Personal Logic Analyzer

Incl. OPTIONS

PM3632

Service manual Edition 2.0

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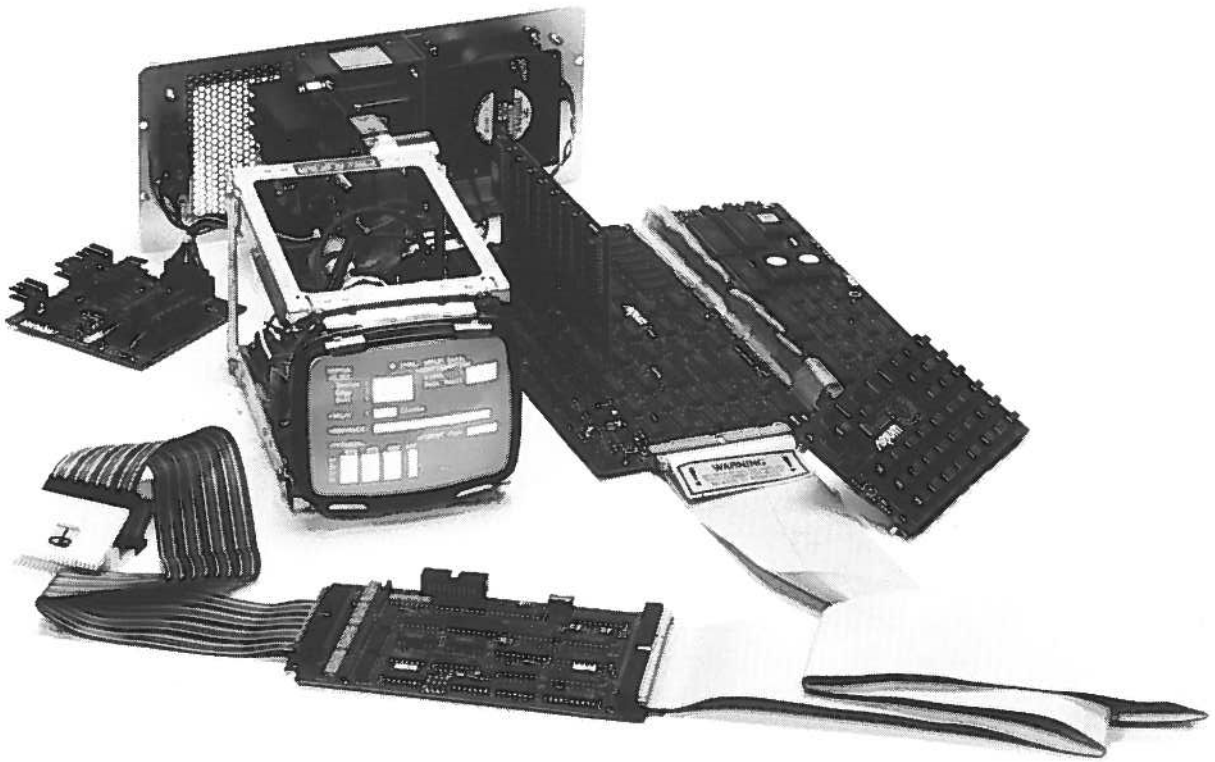

PHILIPS

PHILIPS

This manual (edition 2.0) deals with the PM 3632 and its options, and contains all the information needed for installation, maintenance and service.

Edition 2.0 replaces edition 1.0.
Changes are:
- addition of PM 8870, PM 8874 and PM 8876 microprocessor pods.
- addition of PM8880/80 video output
- addition of chapter 5: disassembly and re-assembly
- addition of chapter 6: troubleshooting

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1. INTRODUCTION

1.1. GENERAL

This maintenance manual is intended to provide reference drawings and circuit descriptions to enable the repair technician to determine how each circuit should behave.
It will not directly locate the fault for every possible symptom, but will instead provide the data and descriptions required to understand normal operation and recognize faults.
Sophisticated diagnostic software and some troubleshooting guidelines however are available to assist the service technician to repair the PM 3632 down to component level (see chapter 5).
This manual assumes a good working knowledge of the PM 3632, and the user should become thoroughly familiar with the PM 3632 setup procedures, operation, and hardware configurations as presented in the PM 3632 Logic Analyzer Operating Manual.

1.2. FEATURES

The PM 3632 Logic Analyzer provides full-featured logic analysis for the debugging and troubleshooting of digital and micro-processor-based products, including complex triggering with state, timing, and (optionally) micro-processor disassembly displays.

Its basic function is to capture (record) the digital data on several signal lines, repetitively, and to do this synchonously or asynchronously with the clock of the system under test. High-speed, asynchronous operation is a powerful aid when solving hardware logic timing problems, while low-speed, synchronous operation is useful for debugging software.

The PM 3632 operates at speeds of up to 100 MHz, at data widths of up to 32 channels, and at a memory depth of up to 8000 samples per channel:

no. of channels	max. sampling rate	memory depth
4	100 MHz (int.clock)	8000
	70 MHz (ext.clock)	8000
8	50 MHz	4000
16	25 MHz	2000
32	12.5 MHz	1000

Data and clock qualifiers can be used, as well as trigger delay of up to 50,000 clocks (Data qualification is available only with 32-channel operation).

The optional ROM Emulator Module (PM 8880/00) enables the software developer to patch the code being traced with the PM 3632.
One or two ROM emulator pods can be connected to the connector at the rear of the unit (in case of two pods, they are daisy chained).
The ROM Emulator Module emulates many popular NMOS PROMs (2716, 2732, 2764 and 27128).
The PM 3632 mainframe is used for editing and controlling transfers to and from the Emulator, but is not involved in the runtime funtions of the Emulator. This leaves all of the normal features of the PM 3632 available for logic analysis during ROM emulation.
The RS232C interface provides for code uploading or downloading.

Further applications for the RS 232C interface are:

- printer for printing a page (state, disassembly and auto sequencing only).
- download or upload data to or from:
  set up memory, data memory, ROM emulator pod.

The optional setup/data memory allows 8 different set ups and 8K of data to be stored in non volatile memory.

An optional video output unit provides a composite video signal for connection to external monitors.

Other options are micro-processor pods with one-clip connection to most popular 8- and 16-bit micro-processors; the resulting disassembly display (if Oisa Rom Board is installed) shows mnemonics for the various instruction and data sequence.

The menus of the PM 3632 can be displayed in two different languages:

english (standard)
french (optional)

The PM 3632 contains a 5-inch, green-screen CRT which displays up to twelve channels of timing diagrams (with labelling) and has cursors for time-measurements. The state display can be formatted and reformatted to achieve almost any conceivable digit combination in several number bases : ASCII, binary, octal, decimal, or hexadecimal.

Four trigger words are available, and can be defined in binary, octal, decimal, or hexadecimal number base. These four words can be combined to form the trigger condition in many different ways. Nineteen trigger sequences are predefined and selectable, and the user may define his own sequence as well. All predefined sequences are available in the 32-channel mode, but these sequences are somewhat more limited in the other modes.

The PM 3632 has been designed for simple set-up and ease of operation. All set-up- and display screens contain complete prompting information which is self-explanatory for most situations.

Standard, the PM 3632 is provided with diagnostic software. Optionally, more extended diagnostic software is available. This software and tools, PM 8891, will help the service technician to repair on component level.

The instrument has been designed and tested according to IEC Publication 348 for class II instruments, and has been supplied in a safe condition. The present Operating Manual contains information and warnings which should be followed by the purchaser to ensure safe operation and to maintain the instrument in a safe condition.

1.3. CONFIGURATIONS

The BASIC PM 3632 consists of a mainframe and one 32 channel logic pod (PM 8860). Other pods that are available are:

- -PM 8862 4 channel fast pod
- -PM 8863 Std. (standard) bus pod
- -PM 8864 ROM emulator pod
- -PM 8865 uP pod: supports 8031, 8032, 8035, 8039, 8040, 8085
- -PM 8866 uP pod: supports 6800, 6802, 6808
- -PM 8867 uP pod: supports 6809/6809E
- -PM 8868 uP pod: supports 6502, 6512, 65C02, 65C102, 65C112
- -PM 8869 uP pod: supports Z80, Z80 A/B/C
- -PM 8870 uP pod: supports NSC 800
- -PM 8874 uP pod: supports 68000, 68010
- -PM 8876 uP pod: supports 8086, 8088

The PM 3632 is connected to the "circuit to test" via one of the above mentioned pods; data and clocks are buffered in the pod, then carried via a 60-conductor ribbon cable to the mainframe, where the data is stored and processed.

This basic unit may be enchanged with a max. of three of four available option cards (installed inside the mainframe).

Available option cards are:

PM 8880/00	ROM emulator module (=PM8880/20+PM8864)
PM 8880/20	RS 232C control card
PM 8880/30	Disa ROM board
PM 8880/40	Setup memory
PM 8880/50	Setup & Data memory

Additional to these option cards, a composite video output unit can be installed in the N.O. service workshops: PM 8880/80

French main software is available as an option: PM 8884/00 (rev. L)
English main software (standard installed) : PM 8883/00 (rev. L)

Some pod connection materials are also commercially available:

- -PM 8882/10 8-ch. probe input set
- -PM 8882/30 24-ch. probe input set
- -PM 8882/50 probe set wire (5 pieces)
- -PM 8882/60 test clip for 40-pin microprocessors

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1.4. SYSTEM SPECIFICATIONS

This specification applies to a PM 3632 Analyzer provided with standard Logic Pod PM 8860, unless otherwise stated.

Properties expressed in numerical values with stated tolerance are guaranteed for ambient temperatures of +5 C.....+40 C unless stated otherwise.
Numerical values without tolerances are typical and represent the characteristics of an average instrument.

This specification is valid after the instrument has been switched-on for at least 15 minutes.

PM 3632 LOGIC ANALYZER

DATA INPUT

Input width	: 4, 8, 16 or 32 bits. The input width is also referred to as number of channels.
Pod inputs	
Sensitivity	: + and -600 mV centered around threshold
Input voltage	: + or -16 V (operating) + or -20 V (absolute rating)
Threshold	: TTL or Variable Variable ranges from +9 V to -9 V.
Input impedance	: 100 kohm//6 pF

DATA RECORDING CLOCK

Internal (asynchronous)	
Rate	: 5 Hz...100 MHz
External (synchronous)	
Data set-up time	: 5 nsec max.
Data hold time	: 1 nsec max.
Clock period	:14 nsec min.
Pulse width	: 7 nsec min.
Clock qualifier	: 1 (external clock only) Qualifier input data same as for the data inputs.
Max. clock rate	: Depending on the recording width, see following list.

Number of Channels	Internal	External
4	100 MHz	70 MHz
8	50 MHz	50 MHz
16	25 MHz	25 MHz
32	12.5 MHz	12.5 MHz

TRIGGERING

Trigger modes	: Sequential or Combinational
Trigger words/events	: Four (4,8 or 32 bit mode) Two (16 bit mode)

Trigger word width : 32 bits maximum (consistent with the number of channels)

Selectable trigger sequences : 19 pre-defined and 1 user-defined.

Predefined : 0...9
A...F
f1...f3
User-defined: f4

The number of trigger sequences being limited by the number of channels, see following list:

Number of Channels	Available Trigger Sequences
4	0, 1, 2, and 3
8	0, 1, 2, and 3
16	0, 1, and 4 (+ user defined)
32	All (incl. user-defined)

Trigger Delay : 0...50,000 clocks

DATA QUALIFICATION (32-bit mode only)

Qualification Modes : State and Combinational

State : Qualification words enable or disable data recording, thus blocks of data to be recorded can be defined.

Combinational : Records only those words which:
1) match qualification words, or
2) don't match qualification words.

MEMORY

Memory depth : Depending on the number of channels

Number of Channels	Recording Depth per Channel
4	8000 samples
8	4000 samples
16	2000 samples
32	1000 samples

LIST DISPLAY MODE

Word list : 14 formatted words

Group columns : 8 max.

Number base : binary, octal, hexadecimal, decimal or ASCII
Repeatable in different number bases and group columns.

Selectable bit groupings for each column.

TIMING DISPLAY MODE

Number of timing lines on the display : 12 max. (any line may be repeated)

Cursors : One main cursor, and one reference cursor.

Magnification (horizontal) : x1 and
x10 (centered around main cursor)

Time measurements
Units : Clock intervals
-Clock periods with external clock
-Time units with internal clock.

Measured time
Without reference cursor: Distance from trigger to cursor
With reference cursor : Distance from reference- to main cursor

DISASSEMBLY DISPLAY MODE

14-line list showing addresses, operands, data, mnemonics and bus activity.

DATA SCROLLING

Continuous (auto repeat).
Absolute instantaneous cursor positioning at trigger.

Timing display mode : Left/right shift, slow or fast

List- and disassembly : Up/down Slow (one sample at a time), or
Fast (one screen at a time)

DISPLAY

5-inch, green phosphor crt

MAINS INPUT

Voltage	: 100V, 110V, 120V, 127V, 200V, 220V, 240V, 250V All +/- 10%
Frequency	: 50 Hz or 60 Hz Jumper selectable
Power consumption	: 170W approx.
Build-in mains fuse	: 2 Amps (delayed) 5x20mm glass tube (1 pc) 10 Amps fuse on power board (1 pc)

PHYSICAL MEASUREMENTS

Size	: Depth 38 cm Width 30 cm Heigth 13 cm
Weigth	: 9.9 kg

ENVIRONMENTAL

Temperature	: 0-40 C operating
Relative humidity	: 5-95%, non-condensing

OPTIONS AND ACCESSORIES

PM 8860 32-CH LOGIC POD

Data input : Refer to PM 3632 system specification

Input PROBE 0-7 (16 wires) : Channel 0...7
External clock
Clock qualifier
Six ground wires

Input PROBE 8-31 (26 wires) : Channel 8...31
Two ground wires

Threshold voltage : TTL = 1.4 V
VAR = -9...+9 V
The threshold voltage can be measured at point 19 to the PROBE 0-7 connector on the Pod. Refer to Fig. 1.1.

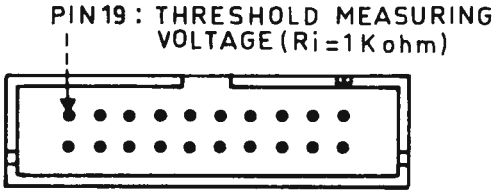

Figure 1.1: Measuring threshold voltage on 32-channel logic pod (8 channel probe set).

PM 8862 4-CH FAST POD

Clock frequency : 100 MHz max. internal clock
75 MHz max. external clock

Threshold : TTL = 1.4 V or,
VAR = -7.9...+7.9 V
The threshold voltage can be measured at the two-pole Molex connector connected to this Pod. The contact at the flat end of this connector is ground potential.

Input voltage : -7.9 V...+7.9 V max.

Sensitivity : + and - 40 mV centered around threshold.

Input impedance : 50 kohm// 6pF

Set-up time : 5 nsec

Hold time : 0.5 nsec

Glitch capture : selectable on/off

Minimum detectable glitch : 40 mV over threshold for 5 nsec.

PM 8863 STANDARD BUS POD

The STANDARD Bus Pod enables to capture bus cycles asynchronously (with the clock from the analyzer), or synchronously (with the external clock).

Modes : STDBUS
STDINT
STD24B

The STANDARD Bus Pod may be inserted into an unoccupied slot on the bus, or it may be used as an extender card.

PM 8864 ROM EMULATOR POD

For Rom Emulation the Analyzer must be provided with:
-PM 8864 Rom Emulator Pod and
-PM 8880/20 RS-232 Communication Card (located inside the Analyzer)

The ROM Emulator emulates one to four Read-Only Memories per Pod, up to a total of 16 Kbytes of memory, and is configurable for 2716, 2732, 2764, or 27128 PROMs.

One or two PM 8864 Pods may be used, for a total of 32 Kbytes of emulation memory. Two Pods can be daisy-chained.
The simulated ROM memory can be uploaded or downloaded, in several popular data transfer formats, to or from other equipment (such as computers/controllers or PROM programmers) via an RS-232C port on the back panel. The memory is displayed on the PM 3632 screen and can be changed directly with front-panel key entries.

PM 8865...8876 MICRO PROCESSOR PODS

These Pods provide one-clip connection to various micro-processors.
These Pods must be used if a disassembler mode has been selected.
The following Pods are currently available:

Pod Type number	Micro-processors supported
PM 8865	Intel 8085,8031,8032,8035,8039 and 8040
PM 8866	Motorola 6800, 6802 and 6808
PM 8867	Motorola 6809, 6809E
PM 8868	Rockwell 6502, 6512, 65C02, 65C102 and 65C112
PM 8869	Zilog Z80, Z80A, Z80B and Z80C
PM 8870	National semiconductor NSC800
PM 8874	Motorola 68000, 68010
PM 8876	Intel 8086, 8088

THRESHOLD : Fixed TTL

PM 8880/00 ROM EMULATOR MODULE

The PM 8880 ROM Emulator Module consists of:

-PM 8864 Rom Emulator Pod
-PM 8880/20 RS-232 Communication Card (located inside the Analyzer)

ROMs supported : 2716, 2732, 2764 and 27128

ROM socket plugs : 4 per Pod

Address bus (all ROMs) : 14 lines, assumed common

Data busses : 2
8-bits each, independent for 8- or 16-bits targets.

Timing :
Tacc : 200 nsec
Tce : 200 nsec
Toe : 70 nsec
Iol : 2.1 mA
Vol : 0.5 V

Data base interface : RS-232 C
Uploads/downloads in hex format

Data editing : From PM 3632 front-panel keys

PM 8880/20 RS-232 CONTROL CARD

Used in conjunction with the Rom Emulator for upload/download of emulation memory.
This unit must be installed inside the analyzer.

Other applications are : Upload/Download system set-up files or reference memory contents, in conjunction with the PM 8880/40/50.
Printer interface for printing a page in STATE, DISASSEMBLY or auto sequence modes.

PM 8880/30 DISA ROM BOARD

This board is required for disassembly of micro-processor programms, and must be located inside the Analyzer.
For each Disassembler a specific Disa Prom must be present on this board.
The Disa Prom is included in delivery with each Micro-processor Pod.
Up to eight different Disa Proms can be located on the Disa Rom board.

PM 8880/40 SET-UP MEMORY

This unit has of a non-volatile memory which can store upto eight complete system set-up files.
Each file can be assigned a 6-character name and a status of "protected" or "unprotected".
Set-up files can be uploaded or downloaded via the PM 8880/20 RS-232 communication Card.
This unit must be located inside the Analyzer.

PM 8880/50 SET-UP AND DATA MEMORY

This unit has of a non-volatile memory which can store upto eight complete system set-up files and one complete data memory (8kx4).
It also has one 8K x 4 RAM to be used as a reference memory (B memory).
The set-up files function as described under "Set-up Memory".
The reference memory can be partitioned into 1, 2, 4, or 8 equal segments which can be saved in non volatile memory.
These saved segments can then be used by the various set-up files, either singly or in the automatic sequence mode. Each saved data segment can be assigned a 6-character name and a status "protected" or "unprotected".
Data segments and setup files can be uploaded or downloaded via the PM 8880/20 RS232C Communication Card.
The unit must be located inside the Analyzer.

1.5 BLOCK DIAGRAM (see fig. 1.2)

1.5.1 GENERAL

This chapter only describes the block diagram of the complete unit, and all its options.
More detailed block diagrams are enclosed in the circuit descriptions of the functional blocks.
As shown in figure 1.2, the PM 3632 logic analyzer has three major functional blocks:

1. a data input pod
2. the PM 3632 mainframe
3. up to three option boards.

To collect data, an input pod must always be connected to the mainframe. The mainframe contains circuitry that collects the data, recognizes trigger conditions and displays the data on the CRT. Optionally, a ROM emulator module (1 or 2 pods) may be added and used concurrently with all other functions.

Data is first buffered in the pod: in some of the pods, it is then registered.
The switching between internal or external clock is done in the pod also.
The data next passes through the input demuliplexer to the data acquisition RAM in the mainframe.
This process continues as long as the unit is active (i.e., the START key has been depressed, but no stop condition has occurred).
Once the recording process has been stopped (via triggering or manually), the data is read from the RAM by the processor and displayed on the CRT in the format selected by the user.

The PM 3632 mainframe consists of a power supply, keyboard, CRT, and the capture board. The capture board handles all basic processing and control functions for the mainframe.

The capture board actually is a pair of snap-apart boards which have been permanently connected via four 25-pin jumper cables.
The larger (lower) card is mounted to the bottom of the box, and contains the input demultiplexer, data RAM, clock generation and dividing and option card interface.
The smaller (upper) card is mounted on the side, and contains the microprocessor and related components, as well as the trigger circuits.

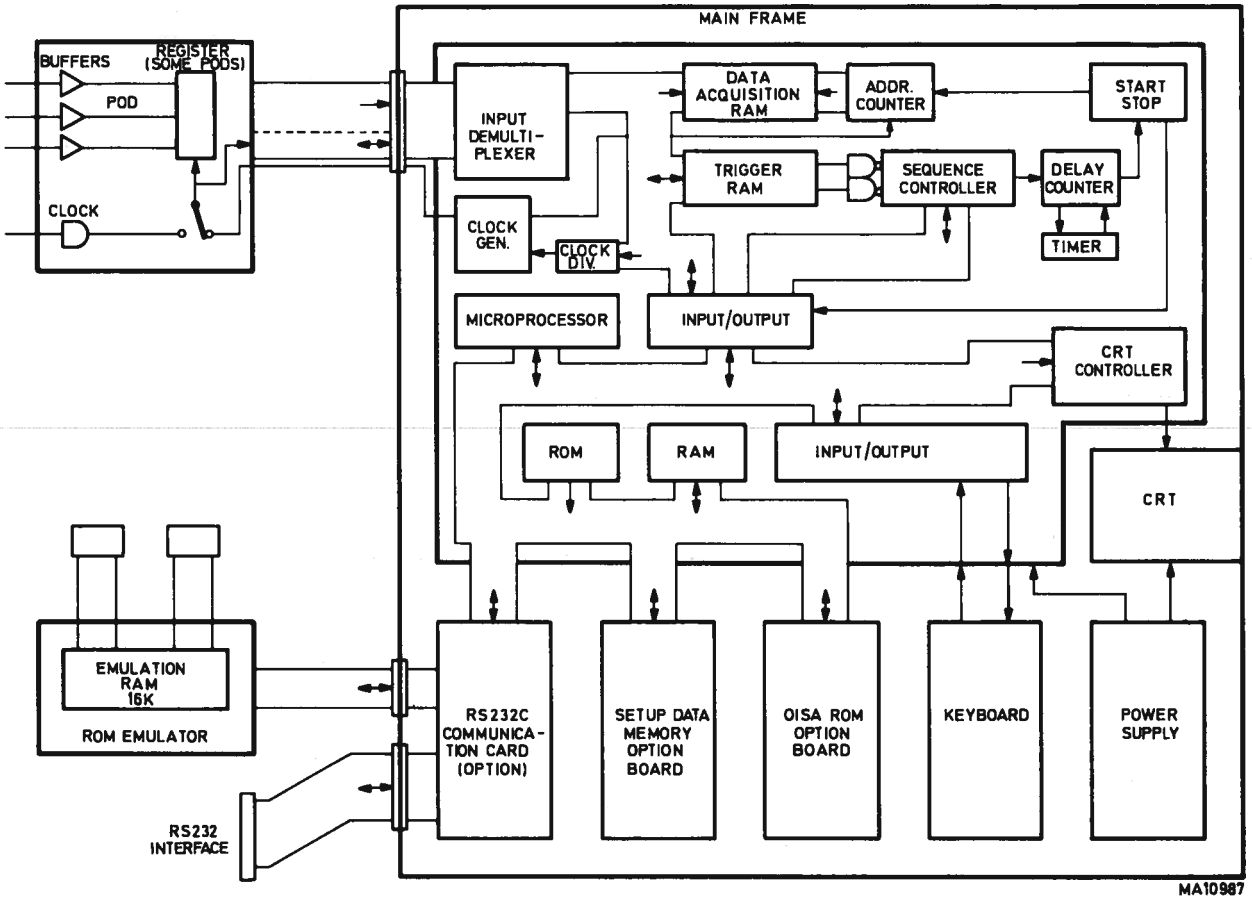

Figure 1.2: PM 3632 block diagram

1.5.2 MAINFRAME

The data signals coming from the pod are processed directly by the input demultiplexing circuitry.
This circuitry operates in one of four input data width: 4, 8, 16 or 32 bits.

In all data width modes, the circuitry's output is 32 bits wide and changes at a maximum rate of 12.5 MHz.

For processing of 4-bit input data, 8 samples are clocked into one 32 bit word, which lowers the word rate by a factor of 8.
This allows the input data to be sampled at 100 MHz, while the output changes at only 12.5 MHz.

Data coming from the input demuliplexer is routed to two major circuit areas: the data acquisition RAM and the trigger RAM.
The data acquisition RAM is normally written into, with each frame of data (a frame in 4-bit mode consists of 8 samples; a frame in 8-bit mode consists of 4 samples, etc.). The exception to this occurs if the data is not qualified by the data qualification circuitry associated with the stop circuitry.

The demultiplexed data is applied to the address pins of the trigger RAM. This RAM is loaded with data which corresponds to the desired trigger action for each input combination of data, applied to the address. The trigger RAM is loaded by the microprocessor before data acquisition is begun and with patterns that depend on the triggerwords defined by the user.

The output of the trigger RAM drives a sequence controller which keeps track of sequential triggering and activates the stop circuitry when the correct sequence of triggerwords has occured in the data stream.
The feedback and output decoding for the sequence controller are accomplished using RAM.

The microprocessor does nothing during data acquisition, except monitor the keyboard and refresh the CRT.
After data acquisition has stopped, it provides data processing and formatting for the operator input functions.
When the START button is depressed, the microprocessor fills the trigger and sequence RAMs with the correct patterns and sets the start/stop logic to begin recording.
The microprocessor also handles auxiliary functions (compare, search, upload, download, etc) and post-data functions (disassembly).

1.5.3 PODS

There are three basic types of data input pods:

1. logic pods
2. microprocessor pods
3. bus pods

All signals to and from the circuit under test are transmitted via a data input pod. The basic purpose of all data input pods is the electrical buffering of the input signals as close as practical to the source; in may cases, the data is also registered in the pod to reduce skew.
All data input pods connect to the PM 3632 via the front-panel connector. Only one data input pod may be connected to the PM 3632 at a time.

Logic Pods

Data, clock, and qualifier signals are first thresholded and high-impedance buffered in the logic pod.
The data and qualifier signals are then clocked into a register, via either an internal or external clock, as selected by the user.
The physical clock switching is done in the pod.

32-Channel Logic Pod (PM 8860)

This pod is part of the standard delivery of the PM 3632.
It functions at word width of up to 32 bits and at speeds of up to 100 MHz (70 MHz with external clock).

4-Channel fast pod (PM 8862)

This pod processes only 4 channels of data at clock speeds of up to 100 MHz. It also detects glitches that occur between two clock samples if commanded to do so from the mainframe.

Microprocessor Pods

There are many types of microprocessor pods; each paricular pod is designed specifically to accomodate one or more particular microprocessors. In all these microprocessor pods, various control signals from the microprocessor are used to develop a clock at the approriate time during each external memory, I/O, or interruptacknowledge cycle. These and other signals are also used to form a status code that identifies the type of microprocessor cycle that has occured (necessary for disassembly). Address demultiplexing is also implemented whenever required.
Address, data and status are then passed up to the mainframe along with the derived clock, if it has been selected.

Bus Pods

A bus pod is functionally almost identical to a microprocessor pod, except it is implemented as an extender board for the particular type of bus.
The only bus that is supported now is the STD (standard) bus (PM 8863).

1.5.4 OPTIONS

Five types of option boards are currently available:

1. The Disa ROM board (provides microprocessor code disassembly).
2. The RS 232C communication card (stand alone or as a part of the ROM emulator module).
3. Setup memory
4. Setup/data memory
5. Composite video output

All these boards are internally installed in the PM 3632 by plugging them into edge connectors on the capture board, which connect them directly to the microprocessor address, data and control busses (except for the video output card). Only three options can be installed at a time (+ video output card). There is no specific connector for any option board; each board may be put into any connector.

Disa ROM board (PM 8880/30)

The Disa ROM board provides disassembly for microprocessor codes.
Upto eight different PROMs may be plugged in at any of the eight sockets at this option board (a 27128 however can only be installed in sockets U5...U8).
It also contains some extra scratch pad RAM.

RS 232C Communication card (PM 8880/20)

The RS 232C communication card contains both, PROM and control circuits to:

1. communicate with the ROM emulator pod(s)
2. upload or download: system setups, reference data (B memory), ROM emulator data.
   Communication is possible with every device or host computer that can communicate in hex format via an RS 232C connection.
3. make a hard copy on a printer of the state list, disassembly list or results of auto sequence (only one page at a time, press f4).

Setup / Setup & data memory (PM 8880/40, PM 8880/50)

The Setup and Setup & data memory options contain EEPROM and UVPROM.
The program stored in UVPROM mechanizes all compare functions and the non volatile storage of setups or data in the EEPROM.
The board layouts of the setup memory option and the Setup data memory option are the same.
The only difference is that the Setup data memory has some extra EEPROMs, some extra RAM and different control software.

Composite video output (PM 8880/80)

This option can be installed in addition to a maximum of 3 option cards. It generates a composite video signal which can be applied to other monitors.

ROM emulator module (PM 8880/00)

The optional ROM emulator module consists of the RS 232C communication card and one ROM emulator pod.
The pod connects to the RS 232C card via the back panel.
This pod contains 16Kbytes RAM configured to emulate popular PROMs. The PM 3632 will accomodate either one pod or two pods used together (which enables you to emulate 16 Kbytes of PROM).
The pods are configured and data is written to them via a serial link (not the RS 232C link!) which is controlled by the RS 232C communication card in the mainframe.

1.6 HARDWARE/SOFTWARE COMPATIBILITY

From the introduction of the PM 3632 and its options, all software releases in the PM 3632 and on each option board fit to each other.
Also each hardware versions of an option board can be used in any PM 3632 in conjunction with any other option board.

NOTE: 1. since the introduction of the 68000/68010 and 8086/8088 microprocessor pods, there is one exception to this statement. These microprocessor pods can only be used succesfully when main software release L (or higher) is installed.

2. For the same software revision, there may be a different indication at the proms. The indication on proms which have not yet the standard prom sticker,may even differ from one instrument to another. The most common indications are listed below. The new standard stickers have the following syntax: M????-?.

Indication of hardware revision, on option boards and PM 3632 capture board:

Capture board	:	920-0530	REV. B
Setup memory	:	920-0587	REV.) no REV indication
Setup Data mmory	:	920-0587	REV.) no REV indication
Disa ROM board	:	920-0545	REV. A
RS 232C communication card	:	920-0552	REV. A

Indication of software revision, at Proms:				Checksum:
Mainframe, english	Software revision	K	; PH K0 and K01 4100	F528 and 16C1
		L	; M4P00-L and M4P01-L	A261 and 5B86
Mainframe, french	Software revision	L	; M4F00-L and M4F01-L	3E88 and 3F5A
Character gen.	Software revision	F	; REV. F, BIGCHR	69DD
		G	; MCH01-G	69D0
Set up memory,	Software revision	B	; REV. B, SM080	A6B7
		B	; MSM00-B	A6B7
Setup Data memory,	Software revision	B	; REV. B, AB032	A5B8
		B	; MAB00-B	A5B8
		C	; MAB00-C	BD0D
RS 232C comm. card,	Software revision	G	; REV. G, ROMEMU	C0BC
		H	; REV. H, ROMEMU	2193
		H	; MRE00-H	2193
PM 8865 disa,	Software revision	E	; REV. E, NDISIN	3787
		E	; MIN00-E	3787
		F	; MIN00-F	EF30
PM 8866 disa,	Software revision	B	; REV. B, OS6800	F91B
		B	; M6800-B	F91B
		C	; M6800-C	FBF8
PM 8867 disa,	Software revision	D	; REV. D, DS6809	35BA
		0	; M6900-0	358A
		E	; M6900-E	25D5
		F	; M6900-F	9F45
PM 8868 disa,	Software revision	C	; REV. C, DS6502	6E17
		C	; M6500-C	6E17
PM 8869 disa,	Software revision	H	; REV. H, Z80	996C
		J	; REV. J, Z80	8638
		J	; MZ800-J	8638
		K	; MZ800-K	F24A
PM 8870 disa,	Software revision	A	; REV. A, NSC800	00A8
		A	; M8N00-A	00A8
PM 8874	Software revision	B	; M6K00-B	2F70
PM 8876	Software revision	A	; M8600-A	E588
Triggerprom for 16-bit disa's, revision		A	; MT600-A	D2F3

Software & hardware revision of the mainframe are indicated in STATUS display: KB (LB)
Software revision K (L)
Hardware revision B (capture board)

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1.7 PROBLEM REPORTS AND CHANGE REQUESTS

In the end of this chapter you find some problem reports and change request forms.

INTRODUCTION

This dual purpose form can be used as either a problem report form or as a change request form, but not for both at the same time.

The form can be used as a problem report only when the equipment does not meet the specifictions detailed in the PM 3632 manuals and when it cannot be repaired through normal service/repair.
Alternatively, the form can be used to describe suggested enchancement or improvements to the equipment as described in the current specification.

NOTE:
Use a separate form for each PROBLEM REPORT or CHANGE REQUEST, thus do not enter more than one subject on a form.

WARNING:

BEFORE FILLING OUT A PROBLEM REPORT OR CHANGE REQUEST, EITHER REMOVE THE THREE LAYERS REQUIRED PER REPORT, OR PLACE A BLOCKING PLATE UNDER THE THIRD LAYER TO ENSURE THAT ONLY THE REQUIRED NUMBER OF DUPLICATES ARE PRODUCED. THESE FORMS ARE CARBON COATED. THEREFORE NO ADDITIONAL CARBON PAPERS ARE REQUIRED.

INSTRUCTIONS FOR COMPLETING

SECTION	REQUIREMENTS
Purpose:	Indicate the type of report with a cross in the appropriate box.
Priority:	Indicate the appropriate priority with a cross in the correct box.
Submitted by:	Fill in full details of the customer's address, because the yellow copy will be used for acknowledgement of reception of the form while using window envelopes. Therefore use, if possible, typewriter or write print letters with ballpoint pen. For the same reason write on the printed lines only as far as they reach. Also do not forget your telephone and telex number!
Description	Give a complete description of the problem or a detailed description of the change requested.
Attached Materials	Do not forget to indicate whether or not you have attached diskettes, listings or other letters. Attachements are very useful for quick responses because it gives details of the problem.
Affected HW/SW	Please give the requested details of (only) the relevant HW/SW configuration when the problem was met. It helps us to judge if an update version of your PM 3632 may be required for solving your Problem/Change Request.
PHILIPS USE ONLY	The boxes indicated in this way are completed in the DTE Supply Centre and therefore restricted for Philips use only. Before returning the yellow copy to the customer the PR or CR number and date of reception are filled out first.

After completing, mail the entire set, top form plus copies to the mailing address listed at the bottom of the form.

NOTES:

NOTES:

2. *MAIN FRAME. CIRCUIT DESCRIPTION*

2.1 GENERAL

This chapter describes the PM 3632 main system.
For an overall understanding of the functioning of all the separate blocks, refer to the block diagram (figure 1.2) first.
A more detailed block diagram is shown in figures 2.1 and 2.2 (microcomputer and analyzer function respectively).
This block diagram will not be explained in detail, but can be used together with the circuit descriptions.

These circuit descriptions contain no unit drawings. All component numbers are printed on the pc board which makes them self-explanatory. How all the pc boards are connected is shown in figure 2.3.
Figure 2.4 shows all the connectors at the capture board and the front panel with all the signal lines that are connected via these connectors.

In all circuit descriptions, a * behind a signal name indicates that it is low active. In the diagrams, the corresponding signalname has a horizontal bar above it.

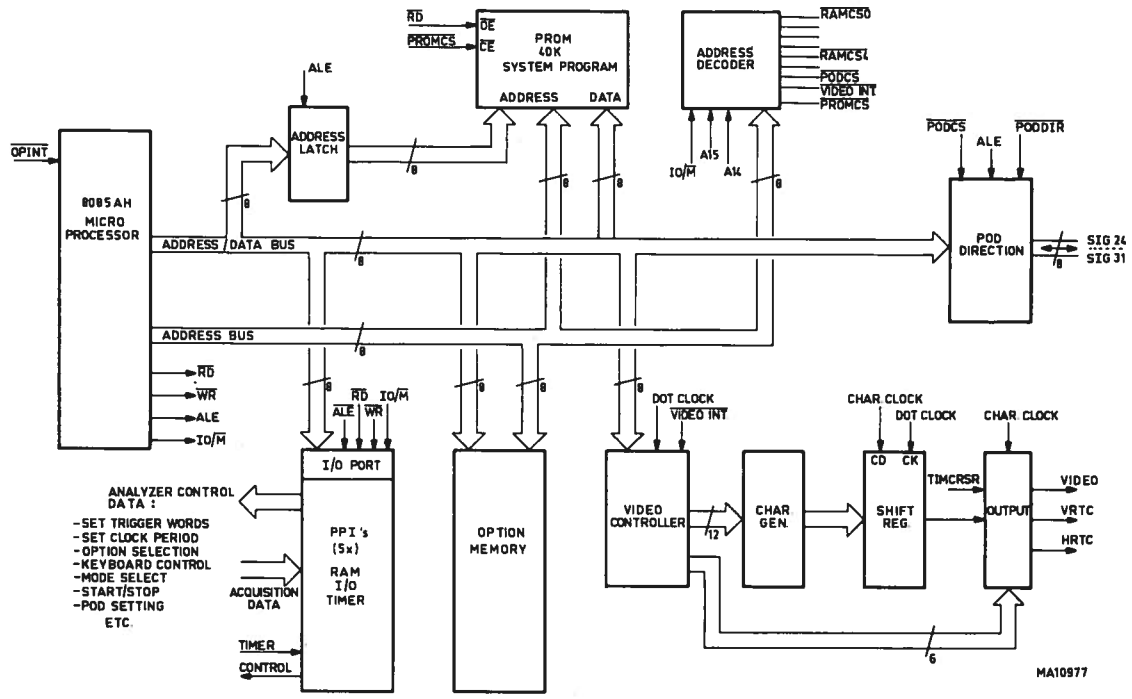


Figure 2.1 : Micro computer, block diagram.

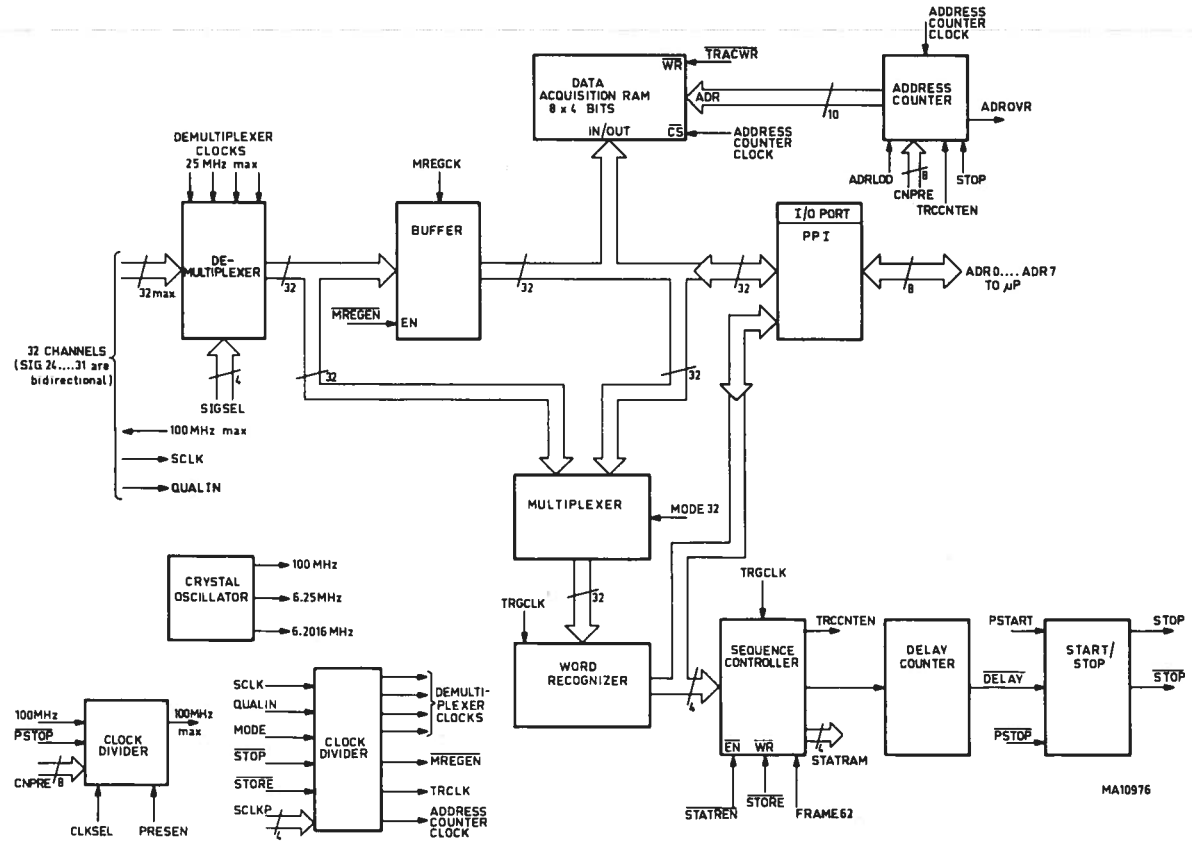


Figure 2.2 : Analyzer functions, block diagram.

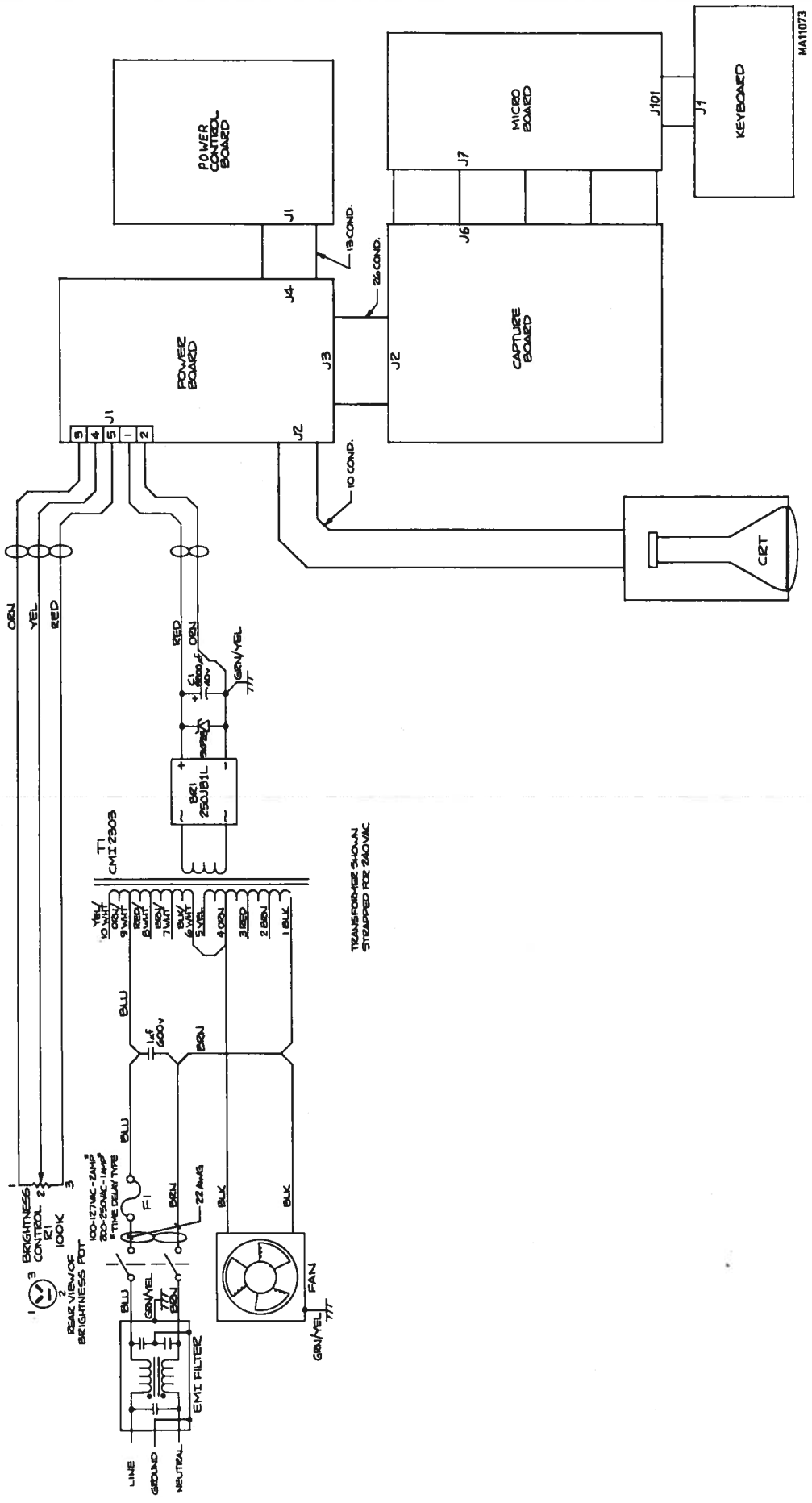


Figure 2.3 : Interconnection between units.

LIST OF SIGNAL NAMES (diagram 1)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM	
6.2016 MHz	Video and uP clock	3	1	
A10	Addressline 10	2	1	
A11	Addressline 11	2	1	
A12	Addressline 12	2	1	
A13	Addressline 13	2	1	
A14	Addressline 14	2	1	
A15	Addressline 15	2	1	
AD0	Address/data line 0	2	1	
AD1	Address/data line 1	2	1	
AD2	Address/data line 2	2	1	
AD3	Address/data line 3	2	1	
AD4	Address/data line 4	2	1	
AD5	Address/data line 5	2	1	
AD6	Address/data line 6	2	1	
AD7	Address/data line 7	2	1	
ADRLDD	Address counter load	2	1	
ALE	Address latch enable	2	1	
BFCLKOUT	Buffered int. sampling clock, out	3	1	
BFPODSEL0	Buffered pod select 0	3	1	
BFPODSEL1	Buffered pod select 1	3	1	
BFPODSEL2	Buffered pod select 2	3	1	
BFPODWRT*	Buffered pod write	3	1	
CNPRE0	Counter preset 0	2	1	
CNPRE1	Counter preset 1	2	1	
CNPRE2	Counter preset 2	2	1	
CNPRE3	Counter preset 3	2	1	
CNPRE4	Counter preset 4	2	1	
CNPRE5	Counter preset 5	2	1	
CNPRE6	Counter preset 6	2	1	
CNPRE7	Counter preset 7	2	1	
DELAY*	Final delay finished	3	1	
DLYCLK	Final delay counter clock	6	1	
EN62*	Enable 62 channel mode	2	1	
FRAME62	62 channel mode, frame indication	5	1	
HRTC	Horizontal retrace	2	1	
IO/M*	Input,output/ memory	2	1	
MODE 4*	4channel mode	2	1	
MODE32*	32 channel mode	2	1	
OP0SEL*	Select option slot 0	3	1	
OP1SEL*	Select option slot 1	3	1	
OP2SEL*	Select option slot 2	3	1	
OPINT*	Option interrupt	21,22,23	1	?
P00CS*	Chip select pod buffer	2	1	
PSTOP*	Pushbutton STOP depressed	2	1	
QUALIN	Qualifier in signal	10,13,16,18 19,20	1	?
RAMCS3*	RAM chip select 3	2	1	
RAMCS4*	RAM chip select 4	2	1	
RD*	Read signal	2	1	
READY	Ready	21,22,23	1	?
RESET OUT	Reset out signal	2	1	
S0	Status line 0	2	1	
S1	Status line 1	2	1	

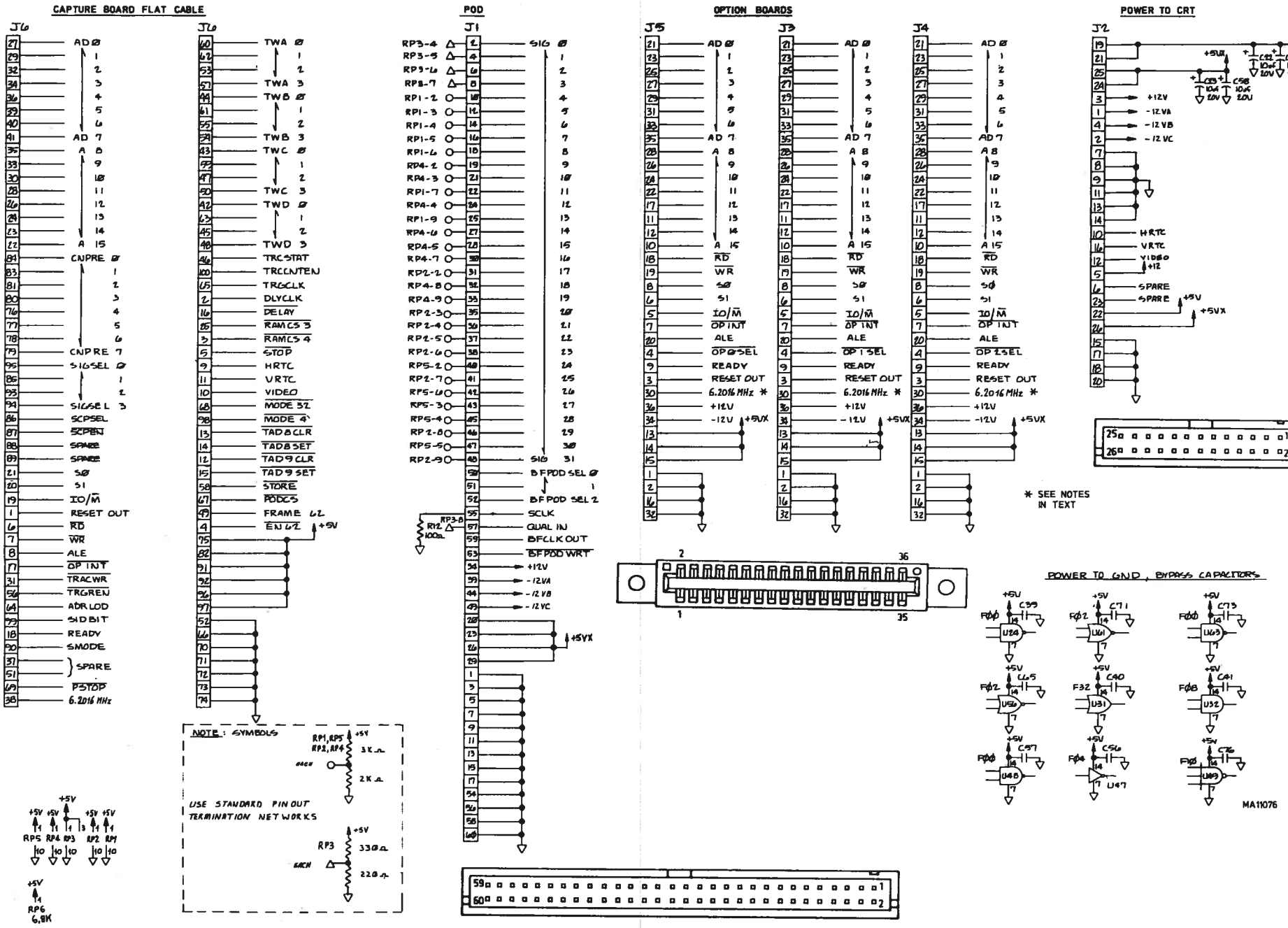
LIST OF SIGNAL NAMES (diagram 1, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM	
SCLK	Selected clock	11,13,16,18 19,20	1	?
SCPEN*	Selected clock pulse enable	2	1	
SCPSEL	Selected clock pulse select	2	1	
SIOBIT	Serial input data, addresscounter	3	1	
SIG 0	Input channel 0	10,12,16,18 19,20	1	?
SIG 1	Input channel 1	10,12,16,18 19,20	1	?
SIG 2	Input channel 2	10,12,16,18 19,20	1	?
SIG 3	Input channel 3	10,12,16,18 19,20	1	?
SIG 4	Input channel 4	10,16,18,19 20	1	?
SIG 5	Input channel 5	10,16,18,19 20	1	?
SIG 6	Input channel 6	10,16,18,19 20	1	?
SIG 7	Input channel 7	10,16,18,19 20	1	?
SIG 8	Input channel 8	10,16,18,19 20	1	?
SIG 9	Input channel 9	10,16,18,19 20	1	?
SIG10	Input channel 10	10,16,18,19 20	1	?
SIG11	Input channel 11	10,16,18,19 20	1	?
SIG12	Input channel 12	10,16,18,19 20	1	?
SIG13	Input channel 13	10,16,18,19 20	1	?
SIG14	Input channel 14	10,16,18,19 20	1	?
SIG15	Input channel 15	10,16,18,19 20	1	?
SIG16	Input channel 16	11,16,18,19 20	1	?
SIG17	Input channel 17	11,16,18,19 20	1	?
SIG18	Input channel 18	11,16,18,19 20	1	?
SIG19	Input channel 19	11,16,18,19 20	1	?
SIG20	Input channel 20	11,16,18,19 20	1	?
SIG21	Input channel 21	11,16,18,19 20	1	?
SIG22	Input channel 22	11,16,18,19 20	1	?
SIG23	Input channel 23	11,16,18,19 20	1	?
SIG24	Input channel 24	3,11,13,16, 18,19,20	1	? BD
SIG25	Input channel 25	3,11,13,16, 18,19,20	1	? BD
SIG26	Input channel 26	3,11,13,16, 18,19,20	1	? BD
SIG27	Input channel 27	3,11,13,16 18,19,20	1	? BD
SIG28	Input channel 28	3,11,13,16, 18,19,20	1	? BD
SIG29	Input channel 29	3,11,13,16 18,19,20	1	? BD
SIG30	Input channel 30	3,11,13,16 18,19,20	1	? BD
SIG31	Input channel 31	3,11,13,16 18,19,20	1	? BD
SIGSEL0	Demultiplexers signal select 0	2	1	

LIST OF SIGNAL NAMES (diagram 1, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM	
SIGSEL1	Demultiplexers signal select 1	2	1	
SIGSEL2	Demultiplexers signal select 2	2	1	
SIGSEL3	Demultiplexers signal select 3	2	1	
SMODE	Select mode	2	1	
STOP	Stop	6	1	
STORE*	Store information	2	1	
TA08CLR*	Address counter, bit 8 clear	2	1	
TA08SET*	Address counter, bit 8 set	2	1	
TA09CLR*	Address counter, bit 9 clear	2	1	
TA09SET*	Address counter, bit 9 set	2	1	
TRACWR*	Data aquisition memory write	2	1	
TRCCNTEN	Address counter enable	6	1	
TRCSTAT	Data qualification trigger switch	6	1	
TRGCLK	Trigger clock	5	1	
TRGREN*	Trigger enable	2	1	
TWA0	Triggerword A, RAM 0	2,5	1	?
TWA1	Triggerword A, RAM 1	2,5	1	?
TWA2	Triggerword A, RAM 2	2,5	1	?
TWA3	Triggerword A, RAM 3	2,5	1	?
TWB0	Triggerword B, RAM 0	2,5	1	?
TWB1	Triggerword B, RAM 1	2,5	1	?
TWB2	Triggerword B, RAM 2	2,5	1	?
TWB3	Triggerword B, RAM 3	2,5	1	?
TWC0	Triggerword C, RAM 0	2,5	1	?
TWC1	Triggerword C, RAM 1	2,5	1	?
TWC2	Triggerword C, RAM 2	2,5	1	?
TWC3	Triggerword C, RAM 3	2,5	1	?
TWD0	Triggerword D, RAM 0	2,5	1	?
TWD1	Triggerword D, RAM 1	2,5	1	?
TWD2	Triggerword D, RAM 2	2,5	1	?
TWD3	Triggerword D, RAM 3	2,5	1	?
VBB		12		
VIDEO	Video signal	2	1	
VRTC	Vertical retrace	2	1	
WR*	Write signal	2	1	

Figure 2.4 : Mainframe connectors (without power supply connectors) (1).



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2.2 CAPTURE BOARD

2.2.1 MICRO COMPUTER (AND USER INTERFACE) + CLOCK GENERATION.

Micro computer and user interface

The basic user interface, including keyboard and CRT handling, is provided by an 8085 NMOS microprocessor.
It and its associated circuits are located on the smaller part of the Capture Board and are illustrated in figure 2.6 and 2.7.
This portion of the machine can be subdivided into several sections:

- *ROM, RAM, and associated decoders which support the program execution.
- *An 8276 (small System CRT Controller) and associated components support the CRT.
- *Several 8155s (PPI's) are used to provide RAM, I/O and timers.

U120 is the 8085-AH main microprocessor (figure 2.6).
Its clock is supplied by a 6.2016 MHz signal produces elsewhere on the board (see clock generation). U101 inverts this clock to drive X2.
C135, R107 and associated diode provide a powerup reset to Pin 36 of the processor.

NOTE: In earlier instruments, the power-up capacitor is slightly too small. This causes sometimes a bad power-up for the uP, due to which the unit stays beeping after switch-on. A small increase (from 10 uF to 22 uF) of this capacitor (C135) will solve this problem. This will cause the unit to beep a little longer after power-up, but the power-up of the microprocessor is ok.
A nicer solution for solving the problem, is changing the power supply. For this, see chapter 2.4.

U101 buffers the interrupt line from the option cards and drives the INTR pin of the microprocessor.
The option card interrupt outputs are "wire-ored" to procedure the input of U101 (refer also to chapter 4).
Pin 7 of the microprocessor (RST 7.5) is driven by the stop logic (U114, see figure 2.14).
Pin 8 (RST 6.5) is driven by the CRT controller and interrupts for each new line of characters (signal 8RDY : Buffer Ready).

The address & data bus outputs from the microprocessor are latched to form the lower address bus by U112 (by means of the ALE pulse).
These lower eight address bits and the next five higher address bits are applied directly to PROM sockets U113 and U121.
Chip selects for these devices are decoded uniquely and directly from the upper addresses by U115 and U117.
The address spaces for these PROMs are indicated on the circuit diagram (refer also to the memory map, figure 2.5).
U103 and the associated gates provide chip selects for the 8155s (PPI's) and the CRT controller (8276).

CRT controller.

The Chip select (CS*) input and the Command/Parameter (C/P*) input of the 8276 are only used to select the CRT controller during initialisation of the video screen. The microprocessor writes the information that defines the video screen into the command and parameter registers directly after power-up.
Inputs Buffer Select (BS*), WR* and RD* are used to fill the video buffer of the 8276 with a new line of characters..

U110, U111, and U133 provide a serial bit stream for the CRT monitor.
Each bit appearing on Pin 13 of U110 is a single dot on the CRT.
U133 outputs ASCII characters along with a row address (LL0-LL3).
1 Addressline (A9) of the character generator is used to divide it into two character sets; one for timing displays (some ASCII characters are replaced by timing characters) and one for other displays (ASCII characters).
These signals are used to address the character generator U111, whose outputs are the bits of one raster row of a character.
These bits are then shifted out by U110 to form the video display (the dot clock is 6.2016 MHz.in units connected to a 50 Hz mains).
A new character row is loaded into the shift register (U110) when signal VIDLOD (VIDEO LOAD, comes from U105) goes low.

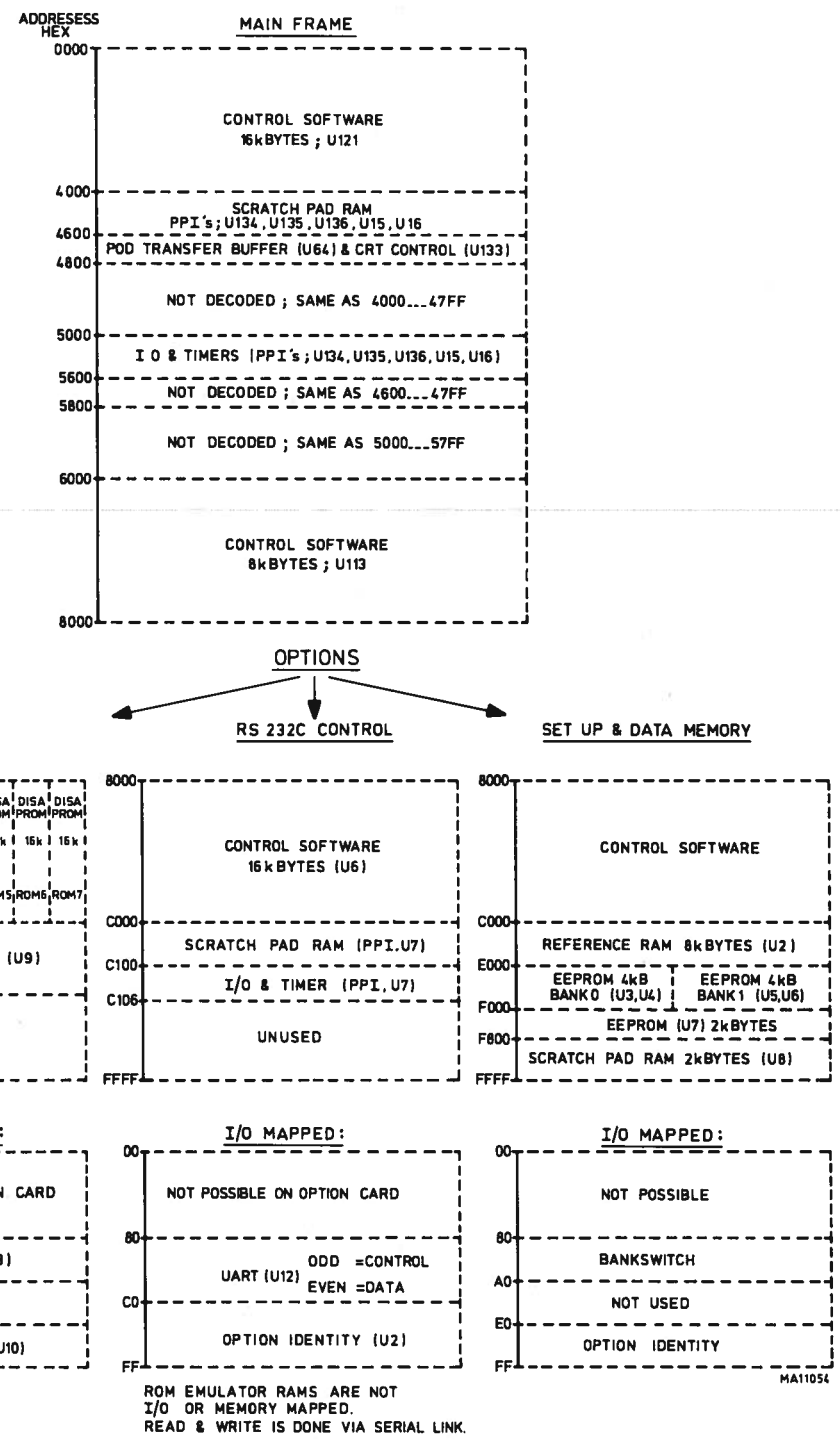


Figure 2.5 : Memory Map.

U119 synchonizes the CRT sync. signals and video attributes from the 8276 with the output of U110.
- VSP (video Suppression) : is used for switching on or off the video signal (blinking cursor).
- RVV (Reverse Video) : inverts the video signal.
- VRTC (Vertical retrace) : vertical synchronisation signal.
- HRTC (Horizontal retrace): horizontal synchronisation signal.
- GPA0, GPA1 (General Purpose Attributes): are used to define the vertical lengths of the cursor (timing display)

U127, Q101, and their associated components form four levels of video, including black.
The three signals-video, vertical sync. (VRTC), and horizontal sync. (HRTC)-- are connected to the CRT monitor.
The 8276 interrupts the microprocessor (BRDY) whenever its internal line buffer is empty.
The microprocessor then fills the buffer with a line of display characters.

U105 is used to derive the character clock (CCCK=VIDLOD) from the 6.2016 MHz dot clock (dot clock is 6.25 MHz for units connected to a 60 MHz. mains).
U105 also drives the cursor generators (Timers in 8155's), for which there are two similar circuits:
  one for the main cursor
  one for the reference cursors (time measurements)

Only the main cursor will be described here.
U125 is clocked to a "one" at the beginning of each line (by means of HRTC), which enables clocks to the timer in U134 via U115. Signal TRACGAT0 and the clock signal coming from U1050B generate four clock pulses in one character.
When the timer expires, U125 will clock to a "zero", again stopping timer clocks.
U114 delays this signal slightly, and U108 decodes the time between these two events as the cursor time (2 dots).
The two cursor signals are mixed at U107 Pin 3.
(The other circuit is similar, but uses two timers so the cursor width can be varied for time measurement displays.)

There are five 8155s on the microprocessor bus; each contains 256 bytes of RAM, a timer circuit, and 22 bits of I/O (see figure 2.7 also).
8155s demultiplex their own address from the processor data bus, and must be provided with the ALE signal.
Signal IO/M* (A12) indicates whether the RAM or the I/O parts are addressed.
Most I/O signals and timers will be described later along with the circuits they are used in.

Pins 29-31 of PPI U136 drive U132, which decodes them for row selects for scanning the keyboard.
The columns on the keyboard matrix are then returned to Pins 1, 2, 5, 37, 38 and 39 of U136 to complete the scan circuit (done in software).
The keyboard is shown in figure 2.8.

Buffer U50 (figure 2.7) is used to read the identity of the connected pod and to write clock and qualifier selection signals to the pod. The direction is controlled by means of signal PODDIR (comes from the microprocessor via PPI U15)
Buffer U64 is used to buffer some control signals for the pod:
  write signal for pod (BFPODWRT)
  pod select signals (BFPODSEL) which determine the pod mode
  internal sampling clock (BFCLKOUT)

These control signals will be described with the pod with which are used.

Clock generation

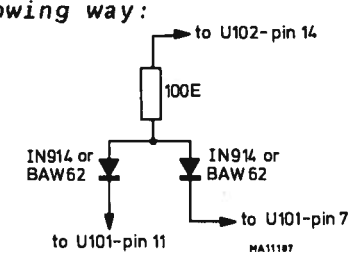
The internal sampling clock (100 MHz) is derived from a 50 MHz oscillator (U55). Transistor Q1 with tuned tank circuit L1, C4 and R3 filter the second hormonic out of this oscillator signal, which is then amplified by transistor Q2.

The 6.2016 MHz clock frequency for the microprocessor is generated by oscillator U23.
This 6.2016 MHz signal is also used as the dot clock for the video interface circuit.

NOTE: 1. For instruments that are connected to a 60 Hz mains, a second oscillator frequency is available (6.25 MHz), derived from the 50 MHz oscillator (via U54). This is to prevent magnetic mains influence on the CRT display. The selection between these two frequencies is done with the jumper near U23 (after the modification described below, this is not jumper selectable anymore!!). A second jumper (near L1) must be changed also to inform the microprocessor if it is a 60 Hz or a 50 Hz mains. The microprocessor can read the position of this jumper via U53. This is necessary for correct initialisation of the video interface (8276).

2. In some instruments, under some circumstances (sometimes after taking-in data with a 68000 microprocessor pod), dots and/or dashes appear random at the screen. This is caused by a bad termination of the 6.2016 MHz clock that goes to the video circuit. If you ever see this appearing, the following modifications have to be done:

- *Cut the track that goes to jumper J6, pin 38 (at the capture board).*
- *This instruction is different for the two different revisions of the capture board.*
  revision C: Cut-off pins of jumper JP2 (near U23).
  Add a wire between pins 2 and 3 of jumper JP2.
  revision B: Put the jumper near U23 in the "60 Hz position" (left).
- *On the solder side, add a wire (as short as possible) between U23-pin 8 and U110-pin 7 (near 8085 microprocessor).*
- *On the solder side, add a wire between U110-pin 1 and U110-pin 8.*
- *On the solder side, connnect a capacitor of 150 pF between pins 7 and 8 of U110.*
- *On the solder side, add a resistor and two diodes to U101/U102 (next to U110), in the following way:*



In instruments with a serial number 1850 or higher, these modifications are done standard.
Whenever you see a PM 3632 in your workshop, you should build-in these modifications.

The frequency of the internal clock (100 MHz) is affected by clock dividers U59, U60, U51 and U52, timer U16 (8155) and multiplexer U53.
These circuits form the internal sampling clock (CLKOUT) that goes to the pod via buffer U64 (BFCLKOUT).
Signal PSTOP takes care of a synchronous start and stop of the internal sampling clock CLKOUT. Signal PSTOP comes from the microprocessor via PPI U134.
The circuits that are used in the different clock ranges are listed in the table on the next page:

CLKOUT:	source:	via:
10ns	100 MHz (U62, U61)	direct, U63
20.....70 ns	100 MHz (U62, U61)	U59, U60, U53, U63
80ns.....9.9 us	20...70ns (U59, U60)	U51, U52, U53, U63
10us.....200 ms	40 ns, 50 ns> >(U51, U52)	Timer U16, U53, U63
	1 us, 12.5us>	

NOTE: U51, U52, U59, U60 are selected components. When changing these, only order the components listed in the spare parts list (see chapter 2.5).

Multiplexer U53 is set used to select the required path for the internal clock signal to form signal CLKOUT. This is done with clock selection signals CLKSEL0 and CLKSEL01 (come from the microprocessor via PPI U16).
Signals CNPRE 0...CNPRE 7 (counter preset) are used to load a certain value in the counters for correct division of the 100 MHz signal. These signals come from the microprocessor via PPI U136.
Signals PRESCAL0...PRESCAL3 (prescale) are used to set the modes for counters U59 and U560 (count up/down, shift left/right, hold) : These signals come from the microprocessor via PPI U16.

The internal sampling clock CLKOUT goes to the pod via buffer U64. In the pod itself the selection is made between internal or external clock. The selected clock comes back as signal SCLK02 (via U45, see figure 2.14) and is connected to U65 that sets the different clock signals for the input demultiplexers (signals SCLKP0...SCLKP3). This setting is done by means of signals SCPSEL (clock pulse select) and SCPEN (clock pulse enable).

LIST OF SIGNAL NAMES (diagram 2)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name. A ? indicates that the source cannot be defined (for example one signal-name can come from different pods, but only one can be connected). A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
6.2016 MHz	Video and uP clock	3	2
A 8	Addressline 8	2	6,21,22,23
A 9	Addressline 9	2	6,21,22,23
A10	Addressline 10	2	1,6,21,22,23
A11	Addressline 11	2	1,6,21,22,23
A12	Addressline 12	2	1,3,6,21,22,23
A13	Addressline 13	2	1,6,21,22,23
A14	Addressline 14	2	1,6,21,22,23
A15	Addressline 15	2	1,6,21,22,23
AD0	Address/data line 0	2	1,3,6,21,22,23 BD
AD1	Address/data line 1	2	1,3,6,21,22,23 BD
AD2	Address/data line 2	2	1,3,6,21,22,23 BD
AD3	Address/data line 3	2	1,3,6,21,22,23 BD
AD4	Address/data line 4	2	1,3,6,21,22,23 BD
AD5	Address/data line 5	2	1,3,6,21,22,23 BD
AD6	Address/data line 6	2	1,3,6,21,22,23 BD
AD7	Address/data line 7	2	1,3,6,21,22,23 BD
ADRLOD	Address counter load	2	1,5,6
ALE	Address latch enable	2	1,6,21,22,23
BPFREQ	Beep frequency	2	2
BRDY	Video buffer ready	2	2
CCLK	Character clock	2	2

LIST OF SIGNAL NAMES (diagram 2, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
CNPRE0	Counter preset 0	2	1,3,5,6
CNPRE1	Counter preset 1	2	1,3,5,6
CNPRE2	Counter preset 2	2	1,3,5,6
CNPRE3	Counter preset 3	2	1,3,5,6
CNPRE4	Counter preset 4	2	1,3,5,6
CNPRE5	Counter preset 5	2	1,3,5,6
CNPRE6	Counter preset 6	2	1,3,5,6
CNPRE7	Counter preset 7	2	1,3,5,6
EN62*	Enable 62 channel mode	2	1,3,5,6
GPA0	General purpose attribute 0	2	2
GPA1	General purpose attribute 1	2	2
HRTC	Horizontal retrace	2	1,6,7,8,9,31
IO/M*	Input,output/ memory	2	1,6,21,22,23
MODE 4*	4channel mode	2	1,5,6
MODE32*	32 channel mode	2	1,5,6
OPINT*	Option interrupt	21,22,23	2 ?
PODCS*	Chip select pod buffer	2	1,3,6
PSTART	Pushbutton START depressed	2	6
PSTOP*	Pushbutton STOP depressed	2	1,3,6
RAMCS0*	RAM chip select 0	2	2
RAMCS1*	RAM chip select 1	2	2
RAMCS2*	RAM chip select 2	2	2
RAMCS3*	RAM chip select 3	2	1,3,6
RAMCS4*	RAM chip select 4	2	1,3,6
RD*	Read signal	2	1,3,6,21,22,23
READY	Ready	21,22,23	2 ?
RESET OUT	Reset out signal	2	1,3,6,21,22,23
S0	Status line 0	2	1,6,21,22,23
S1	Status line 1	2	1,6,21,22,23
SC1	Suppess cursor 1	2	2
SCLKP0	Select clock pulse 0	2	3,5
SCLKP1	Select clock pulse 1	2	3,5
SCLKP2	Select clock pulse 2	2	3,5
SCLKP3	Select clock pulse	2	3,5
SCPEN*	Selected clock pulse enable	2	1,3,5,6
SCPSEL	Selected clock pulse select	2	1,3,6
SIDBIT	Serial input data, addresscounter	3	2
SIGSEL0	Demultiplexers signal select 0	2	1,5,6
SIGSEL1	Demultiplexers signal select 1	2	1,5,6
SIGSEL2	Demultiplexers signal select 2	2	1,5,6
SIGSEL3	Demultiplexers signal select 3	2	1,5,6
SMODE	Select mode	2	1,5,6
STATRAM0	Sequence controller RAM, bit 0	2	6
STATRAM1	Sequence controller RAM, bit 1	2	6
STATRAM2	Sequence controller RAM, bit 2	2	6
STATRAM3	Sequence controller RAM, bit 3	2	6
STATREN*	Sequence controller enable	2	6
STOP	Stop	6	2
STORE*	Store information	2	1,5,6
TA08CLR*	Address counter, bit 8 clear	2	1,5,6
TA08SET*	Address counter, bit 8 set	2	1,5,6
TA09CLR*	Address counter, bit 9 clear	2	1,5,6
TA09SET*	Address counter, bit 9 set	2	1,5,6
TIMCRSR	Timing cursors	2	2
TRACGAT0	Data qualification gate 0	2	2,6
TRACGAT1	Data qualification gate 1	2	2,6
TRACGAT2	Data qualification gate 2	2	2,6
TRACGAT3	Data qaulification gate 3	2	6
TRACTL0	Data qualification control line 0	2	6
TRACTL1	Data qualification control line 0	2	6
TRACWR*	Data aquisition memory write	2	1,5,6
TRGREN*	Trigger enable	2	1,5,6
TWA0	Triggerword A, RAM 0	2	1,6
TWA1	Triggerword A, RAM 1	2	1,6
TWA2	Triggerword A, RAM 2	2	1,6
TWA3	Triggerword A, RAM 3	2	1,6
TWB0	Triggerword B, RAM 0	2	1,6
TWB1	Triggerword B, RAM 1	2	1,6
TWB2	Triggerword B, RAM 2	2	1,6
TWB3	Triggerword B, RAM 3	2	1,6
TWC0	Triggerword C, RAM 0	2	1,6
TWC1	Triggerword C, RAM 1	2	1,6

LIST OF SIGNAL NAMES (diagram 2, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
TWC2	Triggerword C, RAM 2	2	1,6
TWC3	Triggerword C, RAM 3	2	1,6
TWD0	Triggerword D, RAM 0	2	1,6
TWD1	Triggerword D, RAM 1	2	1,6
TWD2	Triggerword D, RAM 2	2	1,6
TWD3	Triggerword D, RAM 3	2	1,6
VIDEO	Video signal	2	1,6,7,8,31
VIDLOAD*	Video load	2	2
VRTC	Vertical retrace	2	1,6,7,8,31
WR*	Write signal	2	1,2,3,6,21,22,23

LIST OF SIGNAL NAMES (diagram 3)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destignation (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
100 MHz	Internal sampling clock source	3	3
6.2016 MHz	Video and uP clock	3	1,2,6,21,22,23
6.25 MHz	Video and uP clock	3	not used
A12	Addressline 12	2	3
AD0	Address/data line 0	2	3 BD
AD1	Address/data line 1	2	3 BD
AD2	Address/data line 2	2	3 BD
AD3	Address/data line 3	2	3 BD
AD4	Address/data line 4	2	3 BD
AD5	Address/data line 5	2	3 BD
AD6	Address/data line 6	2	3 BD
AD7	Address/data line 7	2	3 BD
ADROVR	Address counter overflow	5	3
BFCLKOUT	Buffered int. sampling clock, out	3	1,11,13
BFPODSEL0	Buffered pod select 0	3	1,11,13,16,18,19,20
BFPODSEL1	Buffered pod select 1	3	1,11,16,18,19,20
BFPODSEL2	Buffered pod select 2	3	1,11,16,18,19,20
BFPODWRT*	Buffered pod write	3	1,11,13,16,18,19,20
CLKOUT	Internal sampling clock, out	3	3
CLKSEL0	Internal sampling clock, select 0	3	3
CLKSEL1	Internal sampling clock, select 1	3	3
CNPRE0	Counter preset 0	2	3
CNPRE1	Counter preset 1	2	3
CNPRE2	Counter preset 2	2	3
CNPRE3	Counter preset 3	2	3
CNPRE4	Counter preset 4	2	3
CNPRE5	Counter preset 5	2	3
CNPRE6	Counter preset 6	2	3
CNPRE7	Counter preset 7	2	3
DELAY*	Final delay finished	3	1,6
DLYCLK	Final delay counter clock	6	3
EN62*	Enable 62 channel mode	2	3
OP0SEL*	Select option slot 0	3	1
OP1SEL*	Select option slot 1	3	1
OP2SEL*	Select option slot 2	3	1
OPSEL*	Option select; slot 0,1 or 2	3	21,22,23
POOCS*	Chip select pod buffer	2	3

LIST OF SIGNAL NAMES (diagram 3, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
PODDIR	Pod buffer direction	3	3
POOSEL0	Pod select 0	3	3
PODSEL1	Pod select 1	3	3
POOSEL2	Pod select 2	3	3
PODWRT*	Pod write	3	3
PRESCAL0	Preset sampling clock logic 0	3	3
PRESCAL1	Preset sampling clock logic 1	3	3
PRESCAL2	Preset sampling clock logic 2	3	3
PRESCAL3	Preset sampling clock logic 3	3	3
PSTOP*	Pushbutton STOP depressed	2	3
RAMCS3*	RAM chip select 3	2	3
RAMCS4*	RAM chip select 4	2	3
RD*	Read signal	2	3
RESET OUT	Reset out signal	2	3
SCLK02	Selected clock, phase 2	5	3
SCLKP0	Select clock pulse 0	2	3
SCLKP1	Select clock pulse 1	2	3
SCLKP2	Select clock pulse 2	2	3
SCLKP3	Select clock pulse	2	3
SCPEN*	Selected clock pulse enable	2	3
SCPSEL	Selected clock pulse select	2	3
SIOBIT	Serial input data, addresscounter	3	1,2,6
SIG24	Input channel 24	11,13,16,18 19,20	3 BD
SIG25	Input channel 25	11,13,16,18 19,20	3 BD
SIG26	Input channel 26	11,13,16,18 19,20	3 BD
SIG27	Input channel 27	11,13,16,18 19,20	3 BD
SIG28	Input channel 28	11,13,16,18 19,20	3 BD
SIG29	Input channel 29	11,13,16,18 19,20	3 BD
SIG30	Input channel 30	11,13,16,18 19,20	3 BD
SIG31	Input channel 31	11,13,16,18 19,20	3 BD
TADR8	Address counter bit 8	5	3
TADR9	Address counter bit 9	5	3
TRCD 0	Acquisition data, ch. 0	5	3
TRCD 1	Acquisition data, ch. 1	5	3
TRCD 2	Acquisition data, ch. 2	5	3
TRCD 4	Acquisition data, ch. 4	5	3
TRCD 5	Acquisition data, ch. 5	5	3
TRCD 6	Acquisition data, ch. 6	5	3
TRCD 7	Acquisition data, ch. 7	5	3
TRCD 8	Acquisition data, ch. 8	5	3
TRCD 9	Acquisition data, ch. 9	5	3
TRCD10	Acquisition data, ch. 10	5	3
TRCD11	Acquisition data, ch. 11	5	3
TRCD12	Acquisition data, ch. 12	5	3
TRCD13	Acquisition data, ch. 13	5	3
TRCD14	Acquisition data, ch. 14	5	3
TRCD15	Acquisition data, ch. 15	5	3
TRCD16	Acquisition data, ch. 16	5	3
TRCD17	Acquisition data, ch. 17	5	3
TRCD18	Acquisition data, ch. 18	5	3
TRCD19	Acquisition data, ch. 19	5	3
TRCD20	Acquisition data, ch. 20	5	3
TRCD21	Acquisition data, ch. 21	5	3
TRCD22	Acquisition data, ch. 22	5	3
TRCD23	Acquisition data, ch. 23	5	3
TRCD24	Acquisition data, ch. 24	5	3
TRCD25	Acquisition data, ch. 25	5	3
TRCD26	Acquisition data, ch. 26	5	3
TRCD27	Acquisition data, ch. 27	5	3
TRCD28	Acquisition data, ch. 28	5	3
TRCD29	Acquisition data, ch. 29	5	3
TRCD30	Acquisition data, ch. 30	5	3
TRCD31	Acquisition data, ch. 31	5	3
WR*	Write signal	2	3

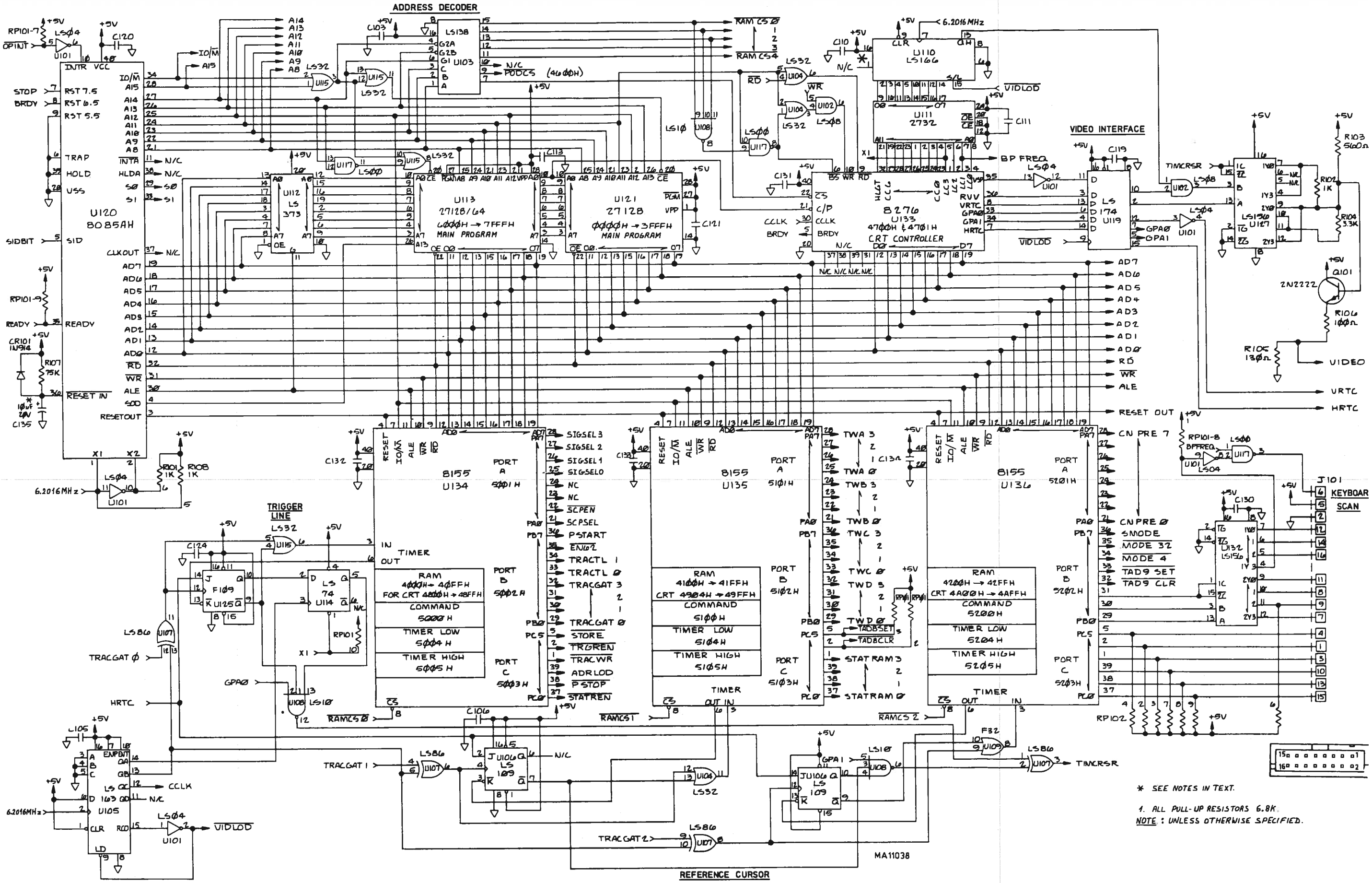


Figure 2.6 : Capture board, microcomputer (2).

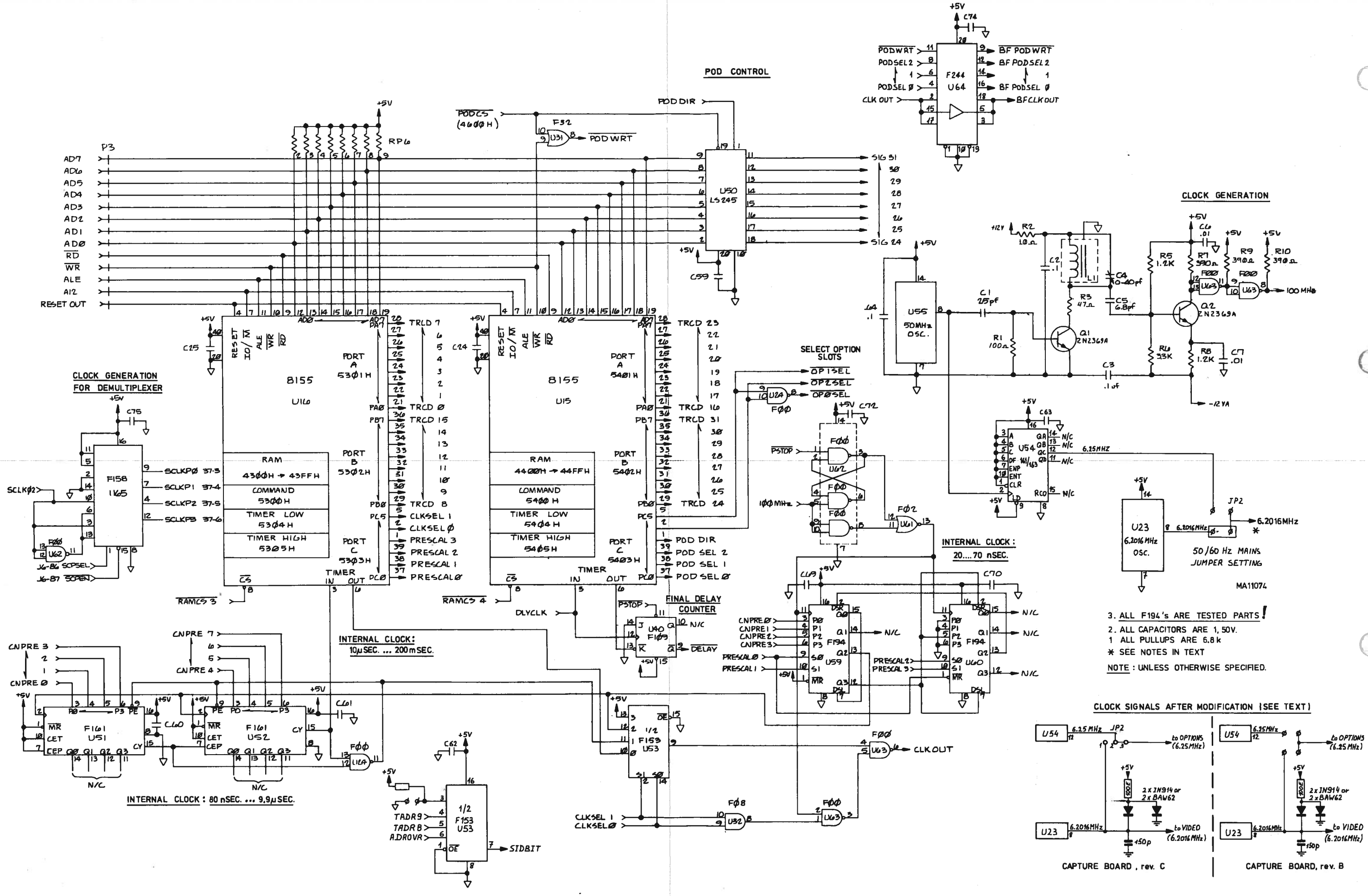


Figure 2.7 : Capture board, microcomputer clock generation (3).

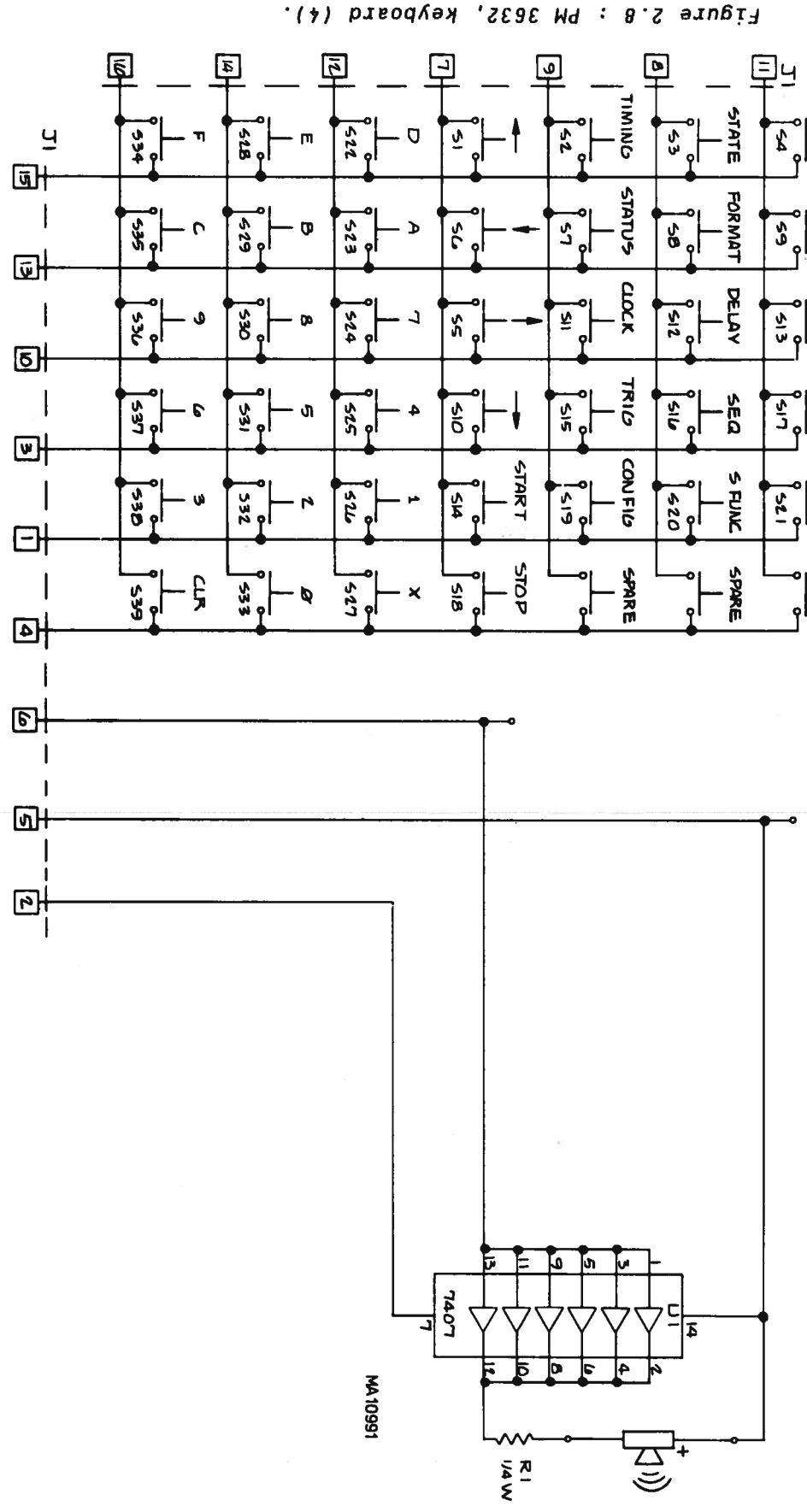


Figure 2.8 : PM 3632, keyboard (4).

2.2.2 INPUT DEMULTIPLEXERS

Data from the pod (SIG0...SIG31) is first processed by the input demultiplexers which organizes it into 32-bit words which can be handled by the PM 3632 cir-circuitry.
Its four modes accept data in word widths of 4, 8, 16, and 32 bits. Input rates in the 4-bit mode are up to 100 MHz. The maximum rate decreases in a binary fashion to 12.5 MHz at 32 bits.

Clocks for the input registers and buffers are developed by U37 and U45 (see upper left part of figure 2.14). U45 operates as a slave, duplicates the signals of U37. This allows driving more loads than U37 could by itself.
SMODE drives Pin 10 of U37-U49; this signal is set by the microprocessor and determines the mode in which U37 operates (load or shift right).
SCLKP 0-3 are also set by the microprocessor and determine the preload of the shift register before its clock is enabled. These signals are also modified by U65 (see figure 2.7) in the 8-bit mode (via signal SCLK02).
SCLK is the clock signal coming from the pod, and can be supplied by the external or internal clock (switching is done in the pod).
Signal QUALIN (qualifier signal from pod) inhibits the clock signals for the demultiplexers as long as the qualifier condition is nut met.
In the 4-bit mode, a pair of adjecent ones is shifted continuously through the the register, providing for four 25 MHz clocks skewed from each other by 90 degrees. In other widths, the outputs are clocked back into the inputs of the register via U65, producing four clocks in one or two phases. These clocks clock the eight 74F399s, as described below (for timing relations of the clock generation, refer also to figure 2.9).

In each of the four modes U13, U14, U21, U22, U29, U30, U38 and U46 register the data directly from the pod.
The modes are controlled with SIGSEL0...SIGSEL3 signal select from the micro-processor.
In the 4-bit mode, the MUX select lines (SIGSEL0...SIGSEL3) are set to cause U14, U22, U30 and U38 to capture the data on lines SIG0...SIG3.
U13, U21, U29 and U46 capture the output of the first registers, and are each clocked at the same time as their predecessor (see also figure 2.9; only the data flow for channel 0 is described).

As an example, U38 is clocked to collect SIG0...SIG3 at every forth sample time. At the same time, U46 is loaded with the output of U38, which is the forth oldest sample.
Every eight samples, this data is loaded into the output register composed of U12, U20, U28 and U43 (by means of signals MREGCK and MREGEN*:12,5 MHz max.)
In 4 bit mode the outputs of U38 and U46 are latched at an intermediate time (4th sample) to insure proper hold time for the ouput registers (signal MODE4*).

In 32-bit and 16-bit mode, all registers are clocked at the same time.
The 16-bit operation is achieved by cascading the pairs, as in 4-bit mode (refer to figures 2.10 and 2.11).
The 8-bit mode is like the 4-bit mode, except the registers are clocked four at a time instead of two at a time (refer to figure 2.12).

For 16-bit microprocessor pods, more than 32 channels are required.
Therefore there is also a 62 bit mode which is for the input demultiplexers the same as the 32 bit mode. In this case bit 31 (signal FRAME 62; is used as control signal for the trigger circuits).
The control signals, for the input demultiplexers, for the different modes are listed in the table in figure 2.14).

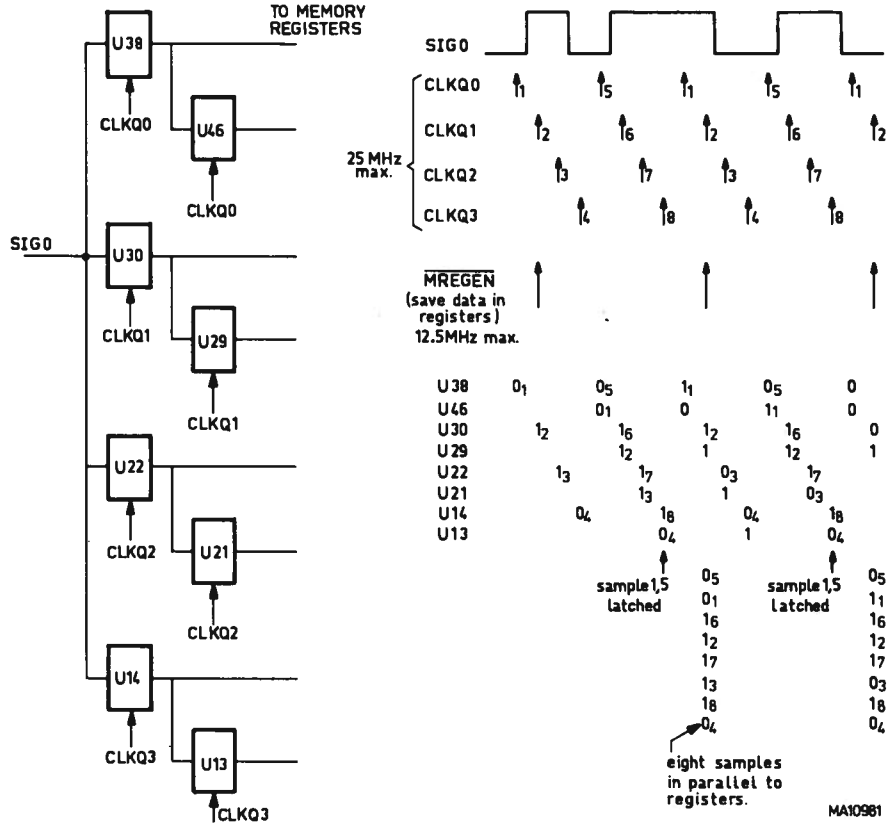


Figure 2.9 : 100 MHz sampling.

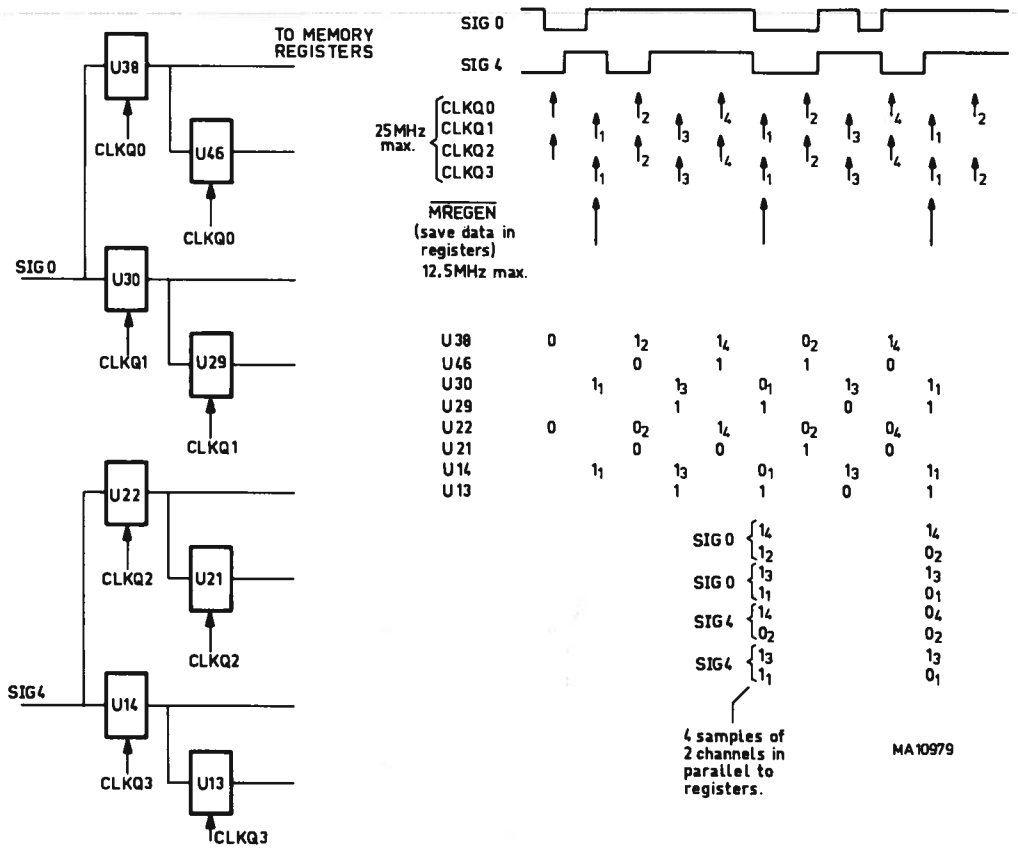


Figure 2.10 : 50 MHz sampling.

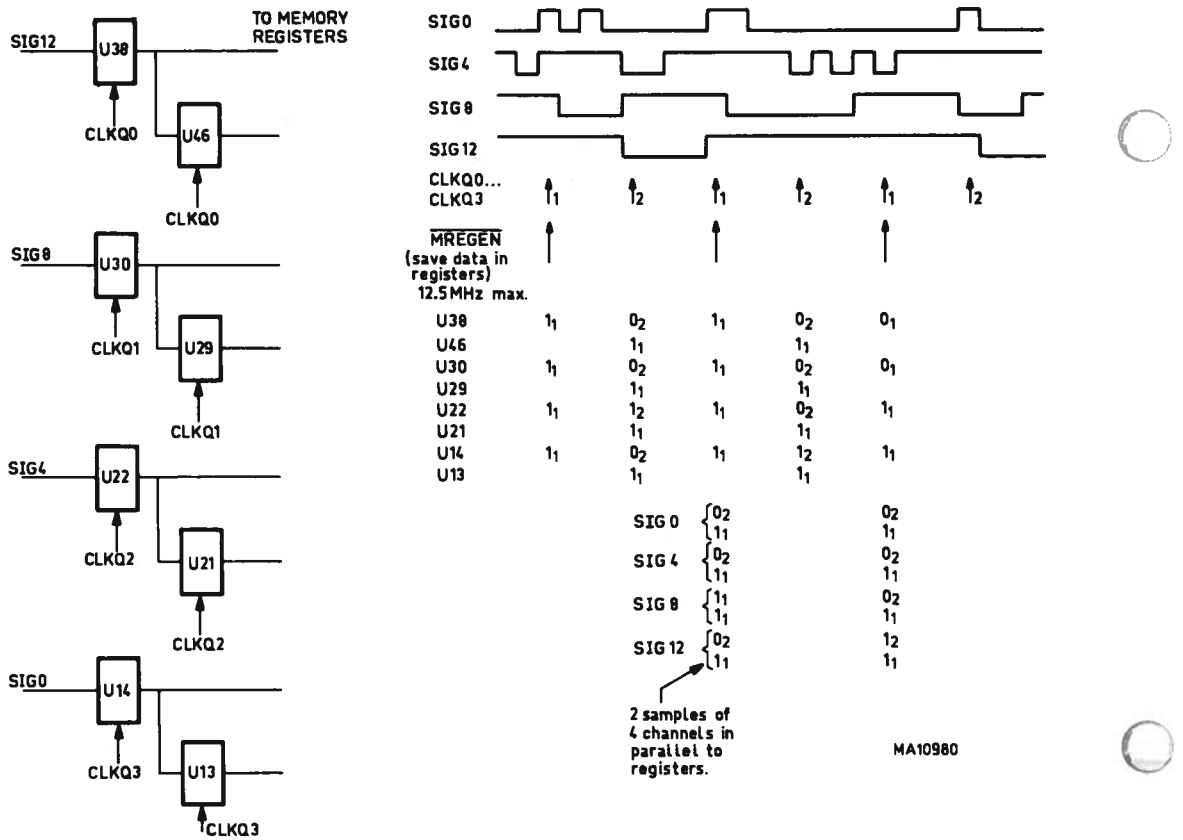
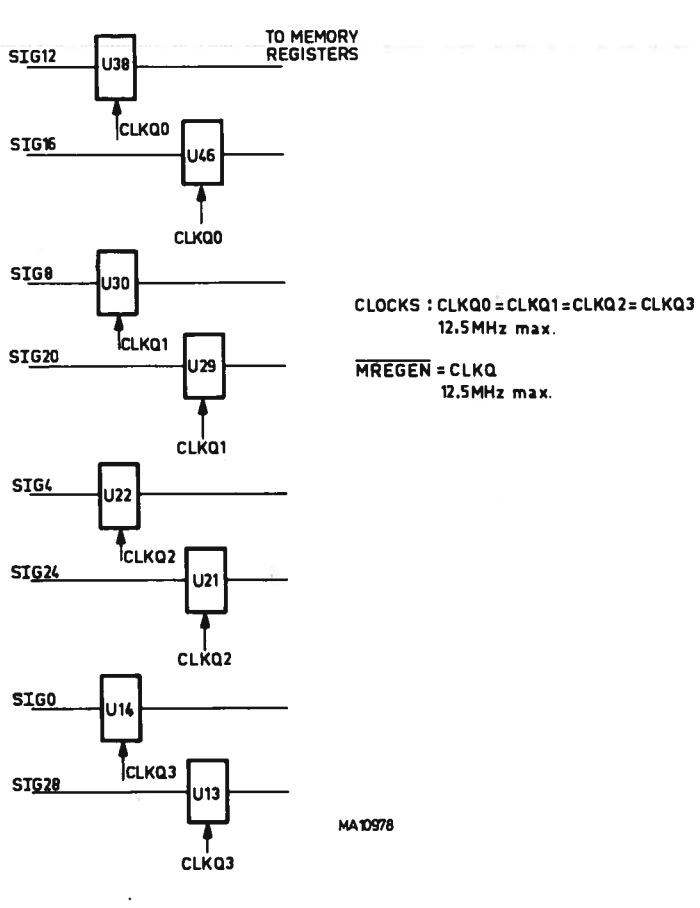


Figure 2.11 : 25 MHz sampling



CLOCKS : CLKQ0 = CLKQ1 = CLKQ2 = CLKQ3
12.5MHz max.

$\overline{\text{MREGEN}}$ = CLKQ
12.5MHz max.

Figure 2.12 : 12.5 MHz sampling

2.2.3 DATA ACQUISITION MEMORIES

U58, U56, and the delay line (U57) form the clock for the data acquisition memory (see figure 2.14). Also the clock for the trigger circuits is generated here (TRGCLK).
U1...U8 form the data acquisition RAMs.
These 4-bit-by-1024-word memories store a total of 32k bits.
U41, U42 (8 address lines) and U39 form the address counter for these RAMs.
Each time a 32-bit record is ready from the input demultiplexers (U43, etc.), U56 (pin 10) clocks this counter and causes a write operation. U40 detects address overflow (signal ADROVR) of the address counter, which does not occur for a small numbers of clocks (those which are less than one memory full).
The overflow only occurs after the trigger condition is fullfilled (signal TRCCNTEN; trace count enable), and the memory is full. Otherwise this counter continues to roll over repetitively until a trigger condition is encountered.
The microprocessor can read signal ADROVR via its serial input (via U53, see figure 2.7); this is necessary for correct data reconstruction.
Signals CNPRE0...CNPRE7 (counter preset) TAD8SET, TAD8CCR, TAD9SET, TAD9CLR and ADRLOD (address load) are used to address the data acquisition RAMs when the microprocessor wants to read the contents of the RAMs after data acquisition has stopped.
The I/O busses TRCD0...TRCD31 from these RAMs are also connected to U15 and U16 (PPIs, see figure 2.7) so that the microprocessor can read out the contents of this RAM.

2.2.4 TRIGGER AND SEQUENCE CIRCUITRY

U9, U17, U25 and U33 are the trigger RAMs (see figure 2.14).
In all modes except 32- and 62-bit, its address lines are driven by the same data as the data lines of the data acquisition RAMs (TRCD0...TRCD31 via MUXes).
In 32-bit and 62-bit mode, these signals are taken directly from the input registers of the input demultiplexer. Signal MODE32 selects the multiplexer inputs (U10, U11 etc).
Only in these two modes data qualification is possible.
The trigger RAM is loaded with the correct pattern by the microprocessor just prior to the start of recording (signal STORE).
If a data sample (used as address lines for the trigger RAMs) corresponds with a selected triggerword, the coresponding outputs of the RAMs will be active.
These outputs are logically "anded" or "ored", as required by U129 and U130 (see figure 2.15).
In 4, 8, 16 and 32 bit modes, only 1/4 of the trigger RAMs is used.
A second quarter is used in 32 bit mode for state qualification: In that case the enable word and disable word are both located at the position of triggerword 0, while TRCSTAT (trigger control state) does the switching between the two quarters (see also figure 2.13).
The second half of the RAMs is used in 62 bit mode.
The 62 bit mode is used when a 16-bit microprocessor pod is connected to the logic analyzer. These pods divide a maximum of 62 input channels in two frames of 31 bits (signal FRAME62 indicates which half is currently in the analyzer).
For triggering on the second half of the 62 bit triggerword, the triggerram is switched-over to the second half (signal FRAME62, see also fig. 2.13).
Signal TRGEN (trigger enable) is used to enable triggering after the correct pattern is loaded in the RAMs.

2.2.5 SEQUENCE CONTROLLER

Sequence controller.

The outputs of U129 and U130 are processed by the sequence controller.
U131 is the input register for this machine, and directly drives U124, the sequence controller RAM.
This RAM is loaded by the microprocessor with a program corresponding to the selected sequence. Its output is registered by U122.
Four lines are used as a feedback to the RAM; These lines indicate the state in which the controller currently is (2 states for initialisation, 13 are left for user defined sequences; state 15 is stop)
U123 decodes the trigger condition state 15 and starts the delay counter composed of U126 and the timer portion of U15 (see figure 2.7). When the delay has expired, U114 is set (stop becomes active which stops the clock generation).
Pressing the STOP pushbutten forces the sequence controller to the stop condition (via U123) via signal PSTOP* (from the microprocessor).

Data qualification.

The state and combinational qualification circuit is formed by U116, U125, U118 and associated components.
Signals TRACGAT0...TRACGAT3 select the words for state or comb. qualification.

Due to the hardware connection (U116), data qualification in 62-bit mode is only possible on the first 31-bit half of the incoming data. This, because in the second half of the data, the triggerrams are also switched-over to the second half.
Allowing data qualification on the second half of the data could result in qualifying one half of the capture data, and disqualifying the other half!
Therefore, only data qualification on the first half is allowed (by the software). Qualification of this half however also qualifies the second. Also disqualification of the first half will disqualify thee second half (signal DF62 holds signal TRCCNTEN stable for two halfs).

Comb. qualification

-only : When the qualified word is found U116 ouputs a "zero" which makes TRCCNTEN (trace counter enable) "zero" via U118. This signal enables the address counter for the data acquisition memories to increment. In this way the qualified word is stored in memory.

-all but: Signal TRCCNTEN will be "zero" (via U118) until a qualified word is found (via U116). This qualified word makes signal TRCCNTEN "high" via U125 and U118. The address counter will not increment now, so the qualified word will be overwritten by the next word.

Signals TRACTL0 and TRACTL1 set multiplexer U118 to input 0 for the "all but mode" or input 1, for the "only" mode.

State qualification

When the enable word is found in the trigger RAMs (stored at the position of word 0) it passes U116 (in the first quarter of these memories).
This causes signal TRCCNTEN to go to "zero" via U118 (input 3). Now the address counter for the data acquisition RAMs is enabled and data will be stored in A memory.

The enable word also toggles JK flip flop U125. Now signal TRCSTAT (trigger control state) switches the trigger RAMs to the second quarter. These RAMs will now start searching for the disable word (stored at the position of word 0). When the disable word is found signal TRCCNTEN will go "high" again which disables the address counter for the data acquisition RAMs.
Signal TRCSTAT switches the trigger RAMs to the first quarter again to search for the enable word again.
Signal LASTGAT is formed via register U122 and is used to hold signal TRCSTAT to the level that it is just set to by the enable or disable word (via U109), until the next qualified word appears.

In 62 bit mode signal OF62 (via U122) holds signal TRCSTAT to the just set level until the next qualified word appears. In this case, state qualification is only possible on the first 31 bit frame of the 62 bit word.

Only qualified words should be able to increment the final delay counter. This is done via U118 output 5 which enables the clock for the delay counter (via U122, U109), however this is done one clockpulse later than the one that belonged to the qualified word. Therefore the last qualified word will not increment the delay counter.
The enabling of a final clockpulse for the delay counter is now done via the feedback of the "enable pin" pin 3 of U137. This enables one more clockpulse (via U118 pin 5); that stops the final delay counter.

2.2.6 OPTION CARD INTERFACE

The three connectors provided on the Capture Board for option expansion are a direct expansion of the microprocessor bus, with the exception of OPINT* and OPSEL* (see figure 2.4, J3, J4 and J5).
OPINT is buffered and applied directly to the interrupt line of the processor.

This signal is "wire-ored".
OP?SEL is the option card select line.
There are three option select lines (?=1, 2, and 3), generated by U15 (see figure 2.7)
Each option card is enabled when its option select line is low; it then provides overlay RAM, ROM, and/or I/O as required (see also figure 2.5; memory map).

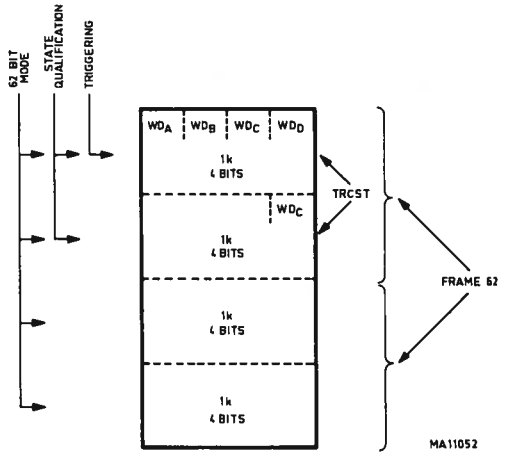


Figure 2.13: Trigger ram.

LIST OF SIGNAL NAMES (diagram 5)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
ADRL00	Address counter load	2	5
ADROVR	Address counter overflow	5	3
CNPRE0	Counter preset 0	2	5
CNPRE1	Counter preset 1	2	5
CNPRE2	Counter preset 2	2	5
CNPRE3	Counter preset 3	2	5
CNPRE4	Counter preset 4	2	5
CNPRE5	Counter preset 5	2	5
CNPRE6	Counter preset 6	2	5
CNPRE7	Counter preset 7	2	5
EN62*	Enable 62 channel mode	2	5
FRAME62	62 channel mode, frame indication	5	1,5,6
M32T 2	32 channel mode, trigger data 2	5	5
M32T 3	32 channel mode, trigger data 3	5	5
M32T 4	32 channel mode, trigger data 4	5	5
M32T 5	32 channel mode, trigger data 5	5	5
M32T 6	32 channel mode, trigger data 6	5	5
M32T 7	32 channel mode, trigger data 7	5	5
M32T 8	32 channel mode, trigger data 8	5	5
M32T 9	32 channel mode, trigger data 9	5	5
M32T 0	32 channel mode, trigger data 0	5	5
M32T 1	32 channel mode, trigger data 1	5	5
M32T10	32 channel mode, trigger data 10	5	5
M32T11	32 channel mode, trigger data 11	5	5
M32T12	32 channel mode, trigger data 12	5	5
M32T13	32 channel mode, trigger data 13	5	5
M32T14	32 channel mode, trigger data 14	5	5
M32T15	32 channel mode, trigger data 15	5	5
M32T16	32 channel mode, trigger data 16	5	5
M32T17	32 channel mode, trigger data 17	5	5
M32T18	32 channel mode, trigger data 18	5	5
M32T19	32 channel mode, trigger data 19	5	5
M32T20	32 channel mode, trigger data 20	5	5
M32T21	32 channel mode, trigger data 21	5	5
M32T22	32 channel mode, trigger data 22	5	5
M32T23	32 channel mode, trigger data 23	5	5
M32T24	32 channel mode, trigger data 24	5	5
M32T25	32 channel mode, trigger data 25	5	5
M32T26	32 channel mode, trigger data 26	5	5
M32T27	32 channel mode, trigger data 27	5	5
M32T28	32 channel mode, trigger data 28	5	5
M32T29	32 channel mode, trigger data 29	5	5
M32T30	32 channel mode, trigger data 30	5	5
M32T31	32 channel mode, trigger data 31	5	5
MODE 4*	4channel mode	2	5
MODE32	32 channel mode	5	5
MODE32*	32 channel mode	2	5
MREGCK	Memory register clock	5	5
MREGEN*	Memory register enable	5	5
QUALIN	Qualifier in signal	10,13,16,18 19,20	5 ?
SCLK	Selected clock	11,13,16,18 19,20	5 ?
SCLK@2	Selected clock, phase 2	5	3

LIST OF SIGNAL NAMES (diagram 5, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM	
SCLKP0	Select clock pulse 0	2	5	
SCLKP1	Select clock pulse 1	2	5	
SCLKP2	Select clock pulse 2	2	5	
SCLKP3	Select clock pulse	2	5	
SCPEN*	Selected clock pulse enable	2	5	
SIG 0	Input channel 0	10,12,16,18 19,20	5	?
SIG 1	Input channel 1	10,12,16,18 19,20	5	?
SIG 2	Input channel 2	10,12,16,18 19,20	5	?
SIG 3	Input channel 3	10,12,16,18 19,20	5	?
SIG 4	Input channel 4	10,16,18,19 20	5	?
SIG 5	Input channel 5	10,16,18,19 20	5	?
SIG 6	Input channel 6	10,16,18,19 20	5	?
SIG 7	Input channel 7	10,16,18,19 20	5	?
SIG 8	Input channel 8	10,16,18,19 20	5	?
SIG 9	Input channel 9	10,16,18,19 20	5	?
SIG10	Input channel 10	10,16,18,19 20	5	?
SIG11	Input channel 11	10,16,18,19 20	5	?
SIG12	Input channel 12	10,16,18,19 20	5	?
SIG13	Input channel 13	10,16,18,19 20	5	?
SIG14	Input channel 14	10,16,18,19 20	5	?
SIG15	Input channel 15	10,16,18,19 20	5	?
SIG16	Input channel 16	11,16,18,19 20	5	?
SIG17	Input channel 17	11,16,18,19 20	5	?
SIG18	Input channel 18	11,16,18,19 20	5	?
SIG19	Input channel 19	11,16,18,19 20	5	?
SIG20	Input channel 20	11,16,18,19 20	5	?
SIG21	Input channel 21	11,16,18,19 20	5	?
SIG22	Input channel 22	11,16,18,19 20	5	?
SIG23	Input channel 23	11,16,18,19 20	5	?
SIG24	Input channel 24	11,13,16,18 19,20	5	? BD
SIG25	Input channel 25	11,13,16,18 19,20	5	? BD
SIG26	Input channel 26	11,13,16,18 19,20	5	? BD
SIG27	Input channel 27	11,13,16,18 19,20	5	? BD
SIG20	Input channel 28	11,13,16,18 19,20	5	? BD
SIG29	Input channel 29	11,13,16,18 19,20	5	? BD
SIG30	Input channel 30	11,13,16,18 19,20	5	? BD
SIG31	Input channel 31	11,13,16,18 19,20	5	? BD
SIGSEL0	Demultiplexers signal select 0	2	5	

LIST OF SIGNAL NAMES (diagram 5, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
SIGSEL1	Demultiplexers signal select 1	2	5
SIGSEL2	Demultiplexers signal select 2	2	5
SIGSEL3	Demultiplexers signal select 3	2	5
SMODE	Select mode	2	5
STOP*	Stop	6	5
STORE*	Store information	2	5
TAD8CLR*	Address counter, bit 8 clear	2	5
TAD8SET*	Address counter, bit 8 set	2	5
TAD9CLR*	Address counter, bit 9 clear	2	5
TAD9SET*	Address counter, bit 9 set	2	5
TADR8	Address counter bit 8	5	3
TADR9	Address counter bit 9	5	3
TRACWR*	Data aquisition memory write	2	5
TRCCNTEN	Address counter enable	6	5
TRCD 0	Acquisition data, ch. 0	5	3
TRCD 1	Acquisition data, ch. 1	5	3
TRCD 2	Acquisition data, ch. 2	5	3
TRCD 4	Acquisition data, ch. 4	5	3
TRCD 5	Acquisition data, ch. 5	5	3
TRCD 6	Acquisition data, ch. 6	5	3
TRCD 7	Acquisition data, ch. 7	5	3
TRCD 8	Acquisition data, ch. 8	5	3
TRCD 9	Acquisition data, ch. 9	5	3
TRCD10	Acquisition data, ch. 10	5	3
TRCD11	Acquisition data, ch. 11	5	3
TRCD12	Acquisition data, ch. 12	5	3
TRCD13	Acquisition data, ch. 13	5	3
TRCD14	Acquisition data, ch. 14	5	3
TRCD15	Acquisition data, ch. 15	5	3
TRCD16	Acquisition data, ch. 16	5	3
TRCD17	Acquisition data, ch. 17	5	3
TRCD18	Acquisition data, ch. 18	5	3
TRCD19	Acquisition data, ch. 19	5	3
TRCD20	Acquisition data, ch. 20	5	3
TRCD21	Acquisition data, ch. 21	5	3
TRCD22	Acquisition data, ch. 22	5	3
TRCD23	Acquisition data, ch. 23	5	3
TRCD24	Acquisition data, ch. 24	5	3
TRCD25	Acquisition data, ch. 25	5	3
TRCD26	Acquisition data, ch. 26	5	3
TRCD27	Acquisition data, ch. 27	5	3
TRCD28	Acquisition data, ch. 28	5	3
TRCD29	Acquisition data, ch. 29	5	3
TRCD30	Acquisition data, ch. 30	5	3
TRCD31	Acquisition data, ch. 31	5	3
TRCSTAT	Data qualification trigger switch	6	5
TRG 4	Trigger data, channel 4	5	5
TRG 5	Trigger data, channel 5	5	5
TRG 6	Trigger data, channel 6	5	5
TRG 7	Trigger data, channel 7	5	5
TRG12	Trigger data, channel 12	5	5
TRG13	Trigger data, channel 13	5	5
TRG14	Trigger data, channel 14	5	5
TRG15	Trigger data, channel 15	5	5
TRG16	Trigger data, channel 16	5	5
TRG17	Trigger data, channel 17	5	5
TRG18	Trigger data, channel 18	5	5
TRG19	Trigger data, channel 19	5	5
TRG24	Trigger data, channel 24	5	5
TRG25	Trigger data, channel 25	5	5
TRG26	Trigger data, channel 26	5	5
TRG27	Trigger data, channel 27	5	5
TRGCLK	Trigger clock	5	1,6
TRGREN*	Trigger enable	2	5
TWA0	Triggerword A, RAM 0	5	1,6
TWA1	Triggerword A, RAM 1	5	1,6
TWA2	Triggerword A, RAM 2	5	1,6
TWA3	Triggerword A, RAM 3	5	1,6
TWB0	Triggerword B, RAM 0	5	1,6

LIST OF SIGNAL NAMES (diagram 5, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
TWB1	Triggerword B, RAM 1	5	1,6
TWB2	Triggerword B, RAM 2	5	1,6
TWB3	Triggerword B, RAM 3	5	1,6
TWC0	Triggerword C, RAM 0	5	1,6
TWC1	Triggerword C, RAM 1	5	1,6
TWC2	Triggerword C, RAM 2	5	1,6
TWC3	Triggerword C, RAM 3	5	1,6
TWD0	Triggerword D, RAM 0	5	1,6
TWD1	Triggerword D, RAM 1	5	1,6
TWD2	Triggerword D, RAM 2	5	1,6
TWD3	Triggerword D, RAM 3	5	1,6

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CLOCK GENERATION FOR DEMULTIPLEXER

DATA STORAGE CLOCK GENERATION

ADDRESS COUNTER

INPUT DEMULTIPLEXER

DATA ACQUISITION RAMS

TRIGGER RAMS

WIDTH	SMODE	SCLK P				SIG SEL				MODE 4	MODE32	ENG2
		3	2	1	0	3	2	1	0			
4	0	1	0	1	0	0	0	0	0	0	1	1
8	0	0	0	1	1	1	1	0	0	1	1	1
16	1	1	1	1	1	0	1	0	1	1	1	1
32	1	1	1	1	1	0	1	1	1	1	0	1
62	1	1	1	1	1	0	1	1	1	1	0	0

Figure 2.14 : Input demultiplexers, data acquisition memories and trigger RAMs (5)

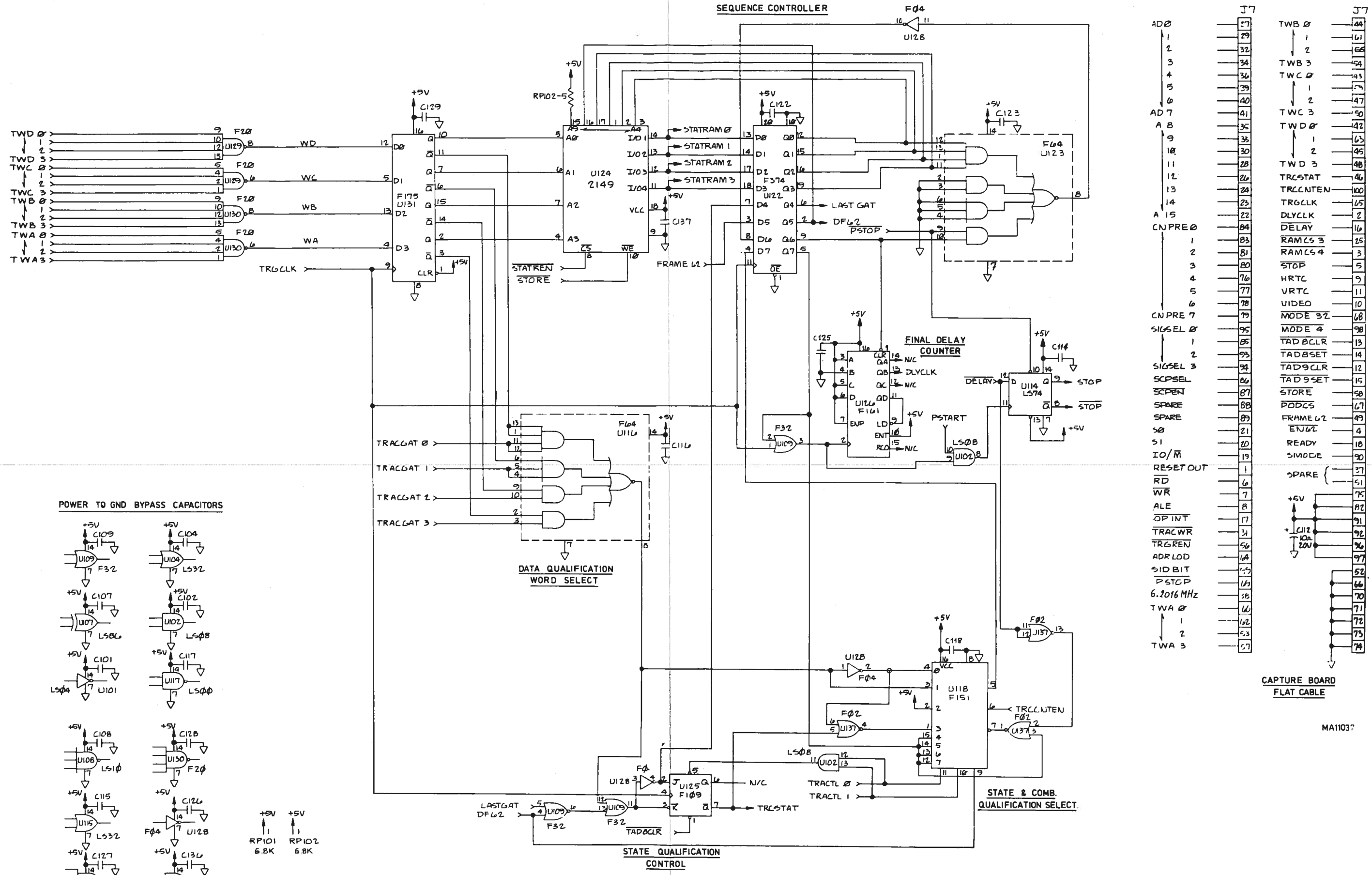


Figure 2.15 : Sequence controller and data qualification circuitry (6)

LIST OF SIGNAL NAMES (diagram 6)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
6.2016 MHz	Video and uP clock	3	6
A 8	Addressline 8	2	6
A 9	Addressline 9	2	6
A10	Addressline 10	2	6
A11	Addressline 11	2	6
A12	Addressline 12	2	6
A13	Addressline 13	2	6
A14	Addressline 14	2	6
A15	Addressline 15	2	6
AD0	Address/data line 0	2	6 BD
AD1	Address/data line 1	2	6 BD
AD2	Address/data line 2	2	6 BD
AD3	Address/data line 3	2	6 BD
AD4	Address/data line 4	2	6 BD
AD5	Address/data line 5	2	6 BD
AD6	Address/data line 6	2	6 BD
AD7	Address/data line 7	2	6 BD
ADRL00	Address counter load	2	6
ALE	Address latch enable	2	6
CNPRE0	Counter preset 0	2	6
CNPRE1	Counter preset 1	2	6
CNPRE2	Counter preset 2	2	6
CNPRE3	Counter preset 3	2	6
CNPRE4	Counter preset 4	2	6
CNPRE5	Counter preset 5	2	6
CNPRE6	Counter preset 6	2	6
CNPRE7	Counter preset 7	2	6
DELAY*	Final delay finished	3	6
DF62	Delayed frame indication	6	6
DLYCLK	Final delay counter clock	6	1,3,6
EN62*	Enable 62 channel mode	2	6
FRAME62	62 channel mode, frame indication	5	6
HRTC	Horizontal retrace	2	6
IO/M*	Input,output/ memory	2	6
LASTGAT	Last captured qualification word	6	6
MODE 4*	4channel mode	2	6
MODE32*	32 channel mode	2	6
OPINT*	Option interrupt	21,22,23	6 ?
PODCS*	Chip select pod buffer	2	6
PSTART	Pushbutton START depressed	2	6
PSTOP*	Pushbutton STOP depressed	2	6
RAMCS3*	RAM chip select 3	2	6
RAMCS4*	RAM chip select 4	2	6
RD*	Read signal	2	6
READY	Ready	21,22,23	6
RESET OUT	Reset out signal	2	6
S0	Status line 0	2	6
S1	Status line 1	2	6
SCPEN*	Selected clock pulse enable	2	6
SCPSEL	Selected clock pulse select	2	6
SIOBIT	Serial input data, addresscounter	3	6
SIGSEL0	Demultiplexers signal select 0	2	6
SIGSEL1	Demultiplexers signal select 1	2	6

LIST OF SIGNAL NAMES (diagram 6, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
SIGSEL2	Demultiplexers signal select 2	2	6
SIGSEL3	Demultiplexers signal select 3	2	6
SMODE	Select mode	2	6
STATRAM0	Sequence controller RAM, bit 0	2	6
STATRAM1	Sequence controller RAM, bit 1	2	6
STATRAM2	Sequence controller RAM, bit 2	2	6
STATRAM3	Sequence controller RAM, bit 3	2	6
STATREN*	Sequence controller enable	2	6
STOP	Stop	6	1,2
STOP*	Stop	6	5,6
STORE*	Store information	2	6
TAD8CLR*	Address counter, bit 8 clear	2	6
TAD8SET*	Address counter, bit 8 set	2	6
TAD9CLR*	Address counter, bit 9 clear	2	6
TAD9SET*	Address counter, bit 9 set	2	6
TRACGAT0	Data qualification gate 0	2	6
TRACGAT1	Data qualification gate 1	2	6
TRACGAT2	Data qualification gate 2	2	6
TRACGAT3	Data qaulification gate 3	2	6
TRACTL0	Data qualification control line 0	2	6
TRACTL1	Data qualification control line 0	2	6
TRACWR*	Data aquisition memory write	2	6
TRCCNTEN	Address counter enable	6	1,5,6
TRCSTAT	Data qualification trigger switch	6	1,5,6
TRGCLK	Trigger clock	5	6
TRGREN*	Trigger enable	2	6
TWA0	Triggerword A, RAM 0	2,5	6 ?
TWA1	Triggerword A, RAM 1	2,5	6 ?
TWA2	Triggerword A, RAM 2	2,5	6 ?
TWA3	Triggerword A, RAM 3	2,5	6 ?
TWB0	Triggerword B, RAM 0	2,5	6 ?
TWB1	Triggerword B, RAM 1	2,5	6 ?
TWB2	Triggerword B, RAM 2	2,5	6 ?
TWB3	Triggerword B, RAM 3	2,5	6 ?
TWC0	Triggerword C, RAM 0	2,5	6 ?
TWC1	Triggerword C, RAM 1	2,5	6 ?
TWC2	Triggerword C, RAM 2	2,5	6 ?
TWC3	Triggerword C, RAM 3	2,5	6 ?
TWD0	Triggerword D, RAM 0	2,5	6 ?
TWD1	Triggerword D, RAM 1	2,5	6 ?
TWD2	Triggerword D, RAM 2	2,5	6 ?
TWD3	Triggerword D, RAM 3	2,5	6 ?
VIDEO	Video signal	2	6
VRTC	Vertical retrace	2	6
WR*	Write signal	2	6

2.3 VIDEO DISPLAY

The video display unit which is used in the PM 3632 is a 5 inch video display unit.
Input signals for the monitor are the HTRC (horizontal retrace), VRTC (vertical retrace) and VIDEO signals.

Because three versions are in the field, three circuit diagrams are enclosed, but it is not recommended to repair this unit because of the low price. Therefore a circuit description in not in this manual.

For those however who want to repair this unit we think these circuit diagrams are self-explanatory (the spare parts list in the back of this chapter contains Philips replacement parts for a few of the semiconductors used in the CRT's).

NOTE: The three different CRT units can be identified as follows:
CRT 1: Manufacturer, KAGA : shorter picture tube: type KT5S831G-OS
CRT 2: Manufacturer, MOTOROLA : longer picture tube (almost reaches the power supply boards): type MD1000-390
CRT 3: Manufacturer, AUDIOTRONIX : short picture tube: type 946-48

LIST OF SIGNAL NAMES (diagram 7)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
HRTC	Horizontal retrace	2	7
VIDEO	Video signal	2	7
VRTC	Vertical retrace	2	7

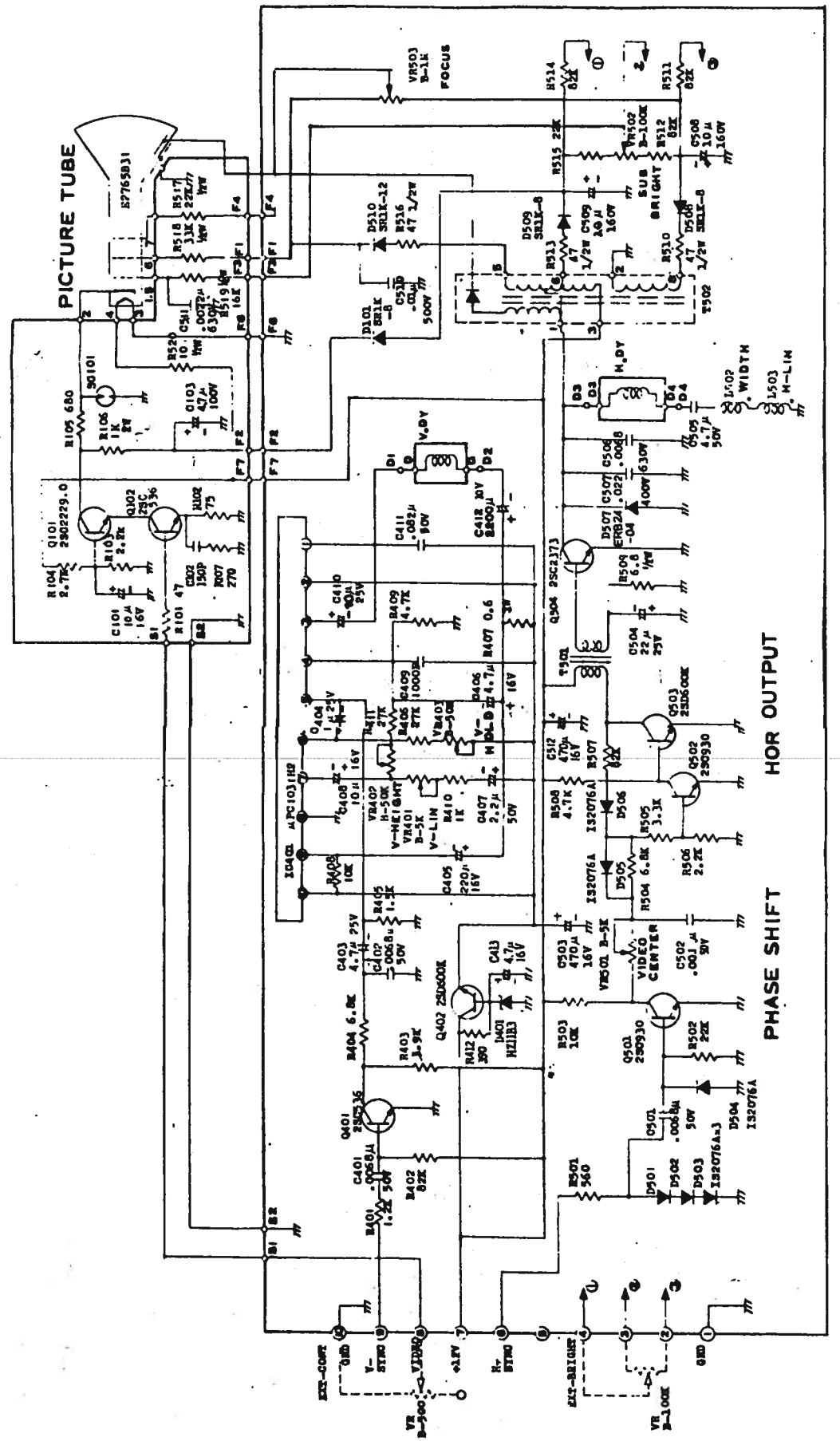


Figure 2.16A : Video display unit 1 (7)

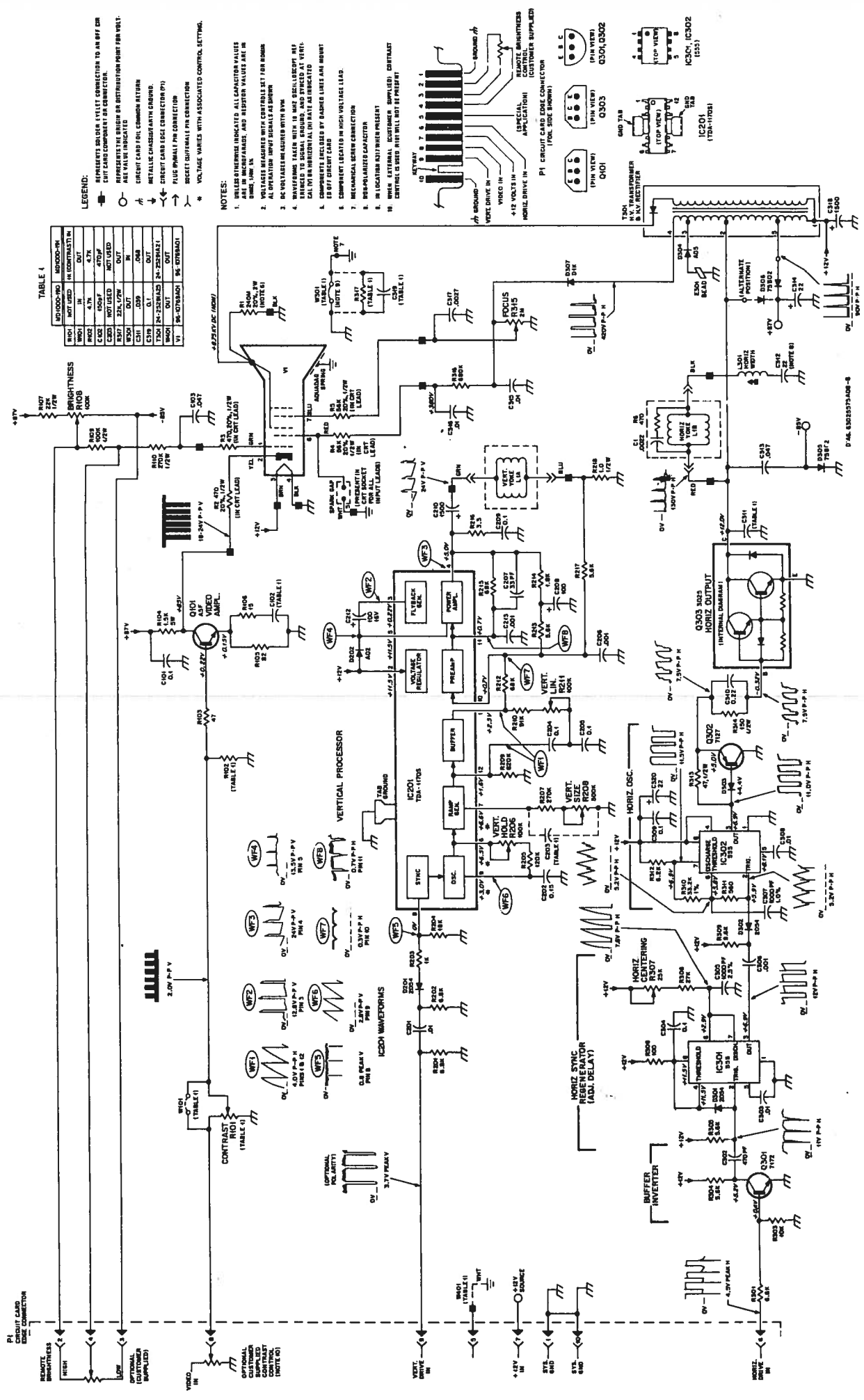


Figure 2.16B : Video display unit 2 (7)

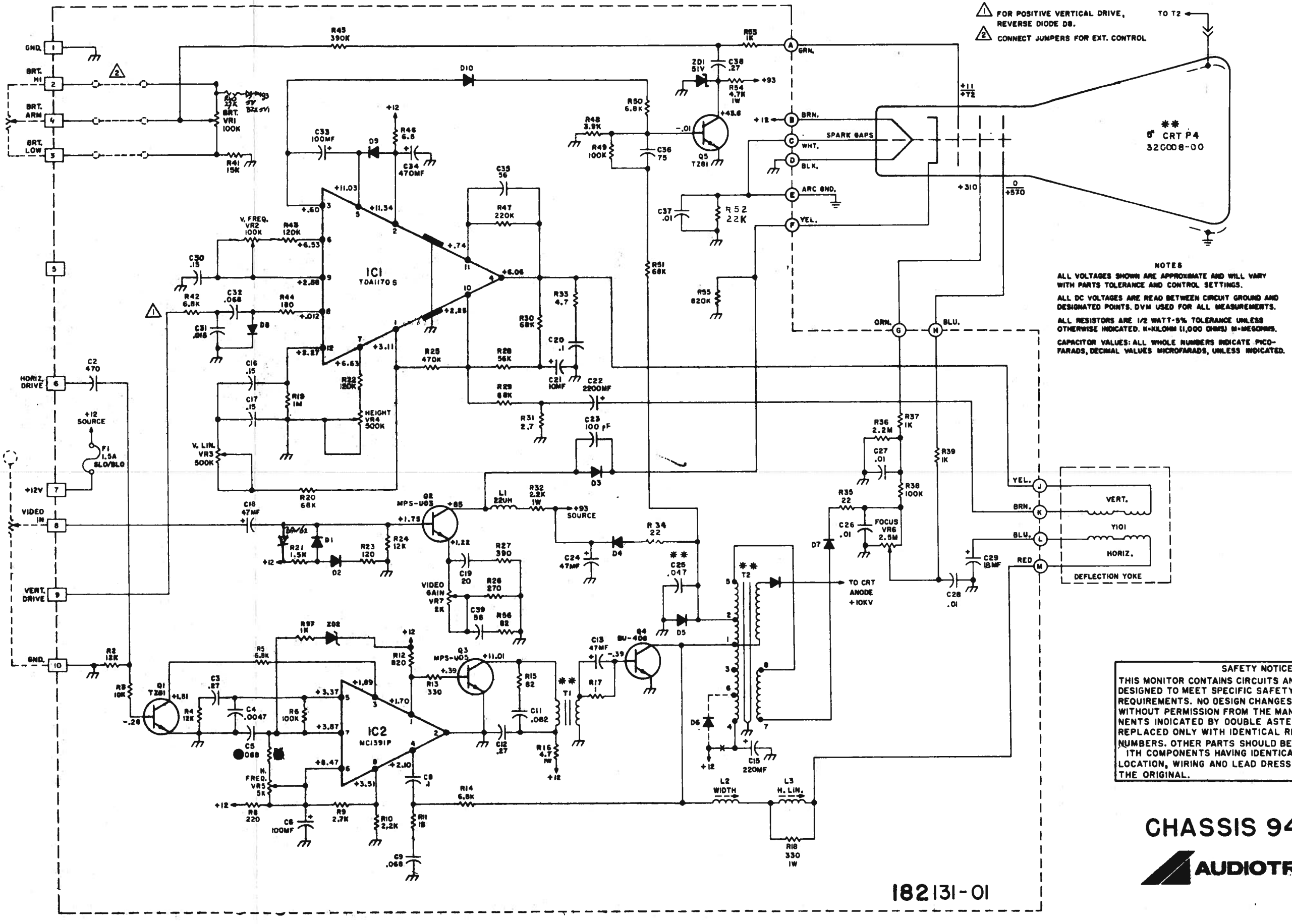


Figure 2.16C : Video display unit 3 (7)

2.4 POWER SUPPLY

How the power supply is configured in the PM 3632 is shown in figure 2.17.
The power supply is suitable for 50 or 60 Hz and for a wide range of supply voltages.
For setting the supply voltage to 220V or 240V, the transformer is fitted with a pair of fastons (for more details, refer to chapter 7).

The power supply is protected in the following ways:

1. overcurrent
2. overvoltage
3. short-circuit
4. overtemperature: results in overcurrent

The mains voltage passes an EMI filter before it passes the switch and the fuse (in 100V...127V range: 2A delayed. in 200V..250V range: 1A delayed).
The output voltage of the transformer passes a rectifier bridge and is then smoothened to form an unregulated voltage of about 21...23 V.
The zener diode in this line is an overvoltage protection, and a "transient killer" for the power supply circuits.

The secondary side of the transformer is then passed to the switched mode power supply.
The output voltage of the power board is regulated by a varying duty cycle which is under control of the power supply control board.
How the power supply is connected to the other boards in the PM 3632 is shown in figure 2.3.

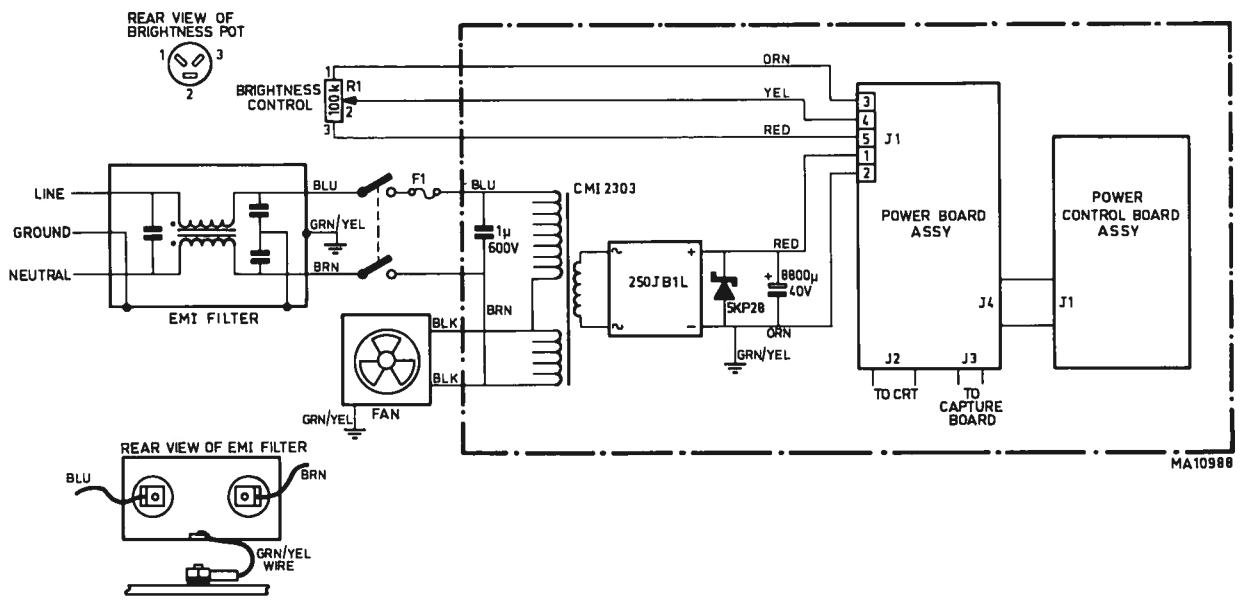


Figure 2.17 : Power supply configuration.

Power board (figure 2.18)

The unregulated voltage comes in at pins 1 (C1+) and 2 (C1-) of connector J1.
This signal passes a 10A fuse and is then distributed to 3 different circuits:

+ 5 V circuit
- 8.5 V circuit
+12 V circuit.

The +5V and -8.5V are switched-mode regulated. The control circuit for these boards is located at the power supply control board.
The output signals of this control board drive power transistors Q3 and Q1.
The +5V circuit consists of:

L3, R8, CR4 : slow-down the collector current increase during switch on.
14, C5 : 15 kHz filter to smoothen the output voltage.
CR7 : limits the output voltage to +6V in case of no load.
CR6, R9, C4 : limits the collector voltage swing during turn-off.

The -8.5V circuit consist of:

L1, R3, CR1 : slow-down the collector current increase during switch on.
L2, C3 : 15 kHz filter to smoothen the output voltage.
CR2, R4, C2 : limits the collector voltage swing during turn-off.

The feedback to the power supply control board is done by means of signals +5CL and -8.5Cl.
The +12V supply is not regulated by means of the power supply control board.
This voltage is directly regulated by a 12V regulator and a coil to supress 15 kHz noise.
To increase the capacity of the +12V regulator, transistor Q5 is added.

Power supply control board (figure 2.19)

The control board consists of three sections:

+ 5 V control (U2)
- 8.5 V control (U3)
-12 V generation (U4)

The +5V and -8.5V control circuits are very similar so only the +5V circuit will be described here.

+5V control.

The control circuit for the +5V supply voltage is an SG3524: a regulating pulse width modulator.
The output of this circuit (pin B: +5V DRV) is a signal which is synchronized with the horizontal retrace signal (HRTC) of the video display unit via a one shot (Q1, Q2).
The pulse width of this signal varies according to a varying +5V output voltage. A lower output voltage increases the duty cycle. A higher output voltage decreases the duty cycle.
This is accomplished via the feedback signal which is applied to operational amplifier U1 (pin2) where it is compared with a reference voltage (formed by the SG3524 itself: pin 16 = +5V).
Diode CR6 affects the duty cycle via pin 10 of the SG3524, but only for transients appearing at the +5V output.
An overcurrent protection is formed by means of operational amplifier U1 (pin8). When the output current becomes too big U1 will affect the duty cycle via pin 4 of the SG3524.
To compensate for noise appearing on the ground, signal SNSRTN (sense return) affects the reference voltage for comparator U1, via R1, C1.

To reduce 50 or 60 Hz noise (coming out of the transformer) the circuit consisting of U1 (pin 7) and associated components also affect the duty cycle, via the feedback input of the SG 3524 (pin 9, signal Vfb-1). Signal ENVF08K comes from the power board.

Diode CR8, capacitor C21 and associated components take care of a slow start by increasing the duty cycle slowly when powering-up the PM 3632.

-12V generation

The -12V is directly derived from the -8.5V supply.
The principle is that two capacitors (C18 and C19) are switched in parallel by means of Q3 and Q4 and then loaded to -8.5 V (VDD).
Then the capacitors are switched in series which results in a -17 V input voltage for the voltage regulator(VR1).
This voltage regulator provides a -12V output voltage which is then smoothened by means of coil L1.

The switching frequency is synchronized with the switching frequency of the other two control circuits.

NOTE: 1. In earlier instruments, the reset for the 8085 microprocessor is not long enough. This, sometimes, causes the instrument to beep constantly after power-up. To avoid this problem, a modification of the power will cause the power supply to start more quickly.

Change C1 from 10 uF into 0.1 uF:
This causes the +5 V to come-up more quickly.

Change C21 from 10 uF into 100 uF:
Changing C1, causes a too quick start of the +5 V on pin 9 of U2. Changing C21 slows down the Vstart voltage increase.

Replace C15 by a resistor (!) of 4.7 Kohm, 1/4 W, 5 %:
For a more reliable start-up of the -12V supply.

Change R36 from 10 Kohm into 3.3 Kohm:
This causes the a 3.8 V voltage at pin 9 of U4, which sets the switching signal to 50% duty cycle.

2. When having problems with the -12 V supply, replace capacitor C15 by a resistor (!) of 4.7 Kohm, 1/4 W, 5 %. This will result in a more reliable start-up of the -12 V supply.

LIST OF SIGNAL NAMES (diagram 8)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
+5CL	+5 V feedback	8	9
+5VDRV	+5 V drive signal	9	8
-8.5CL	-8.5 V feedback	8	9
-8.5VDRV	-8.5 V drive signal	9	8
ENVFDBK	Feedback for 50 Hz suppression	8	9
HRTC	Horizontal retrace	2	8
SNSRTN	Sense return	8	9
VIDEO	Video signal	2	8
VRTC	Vertical retrace	2	8

LIST OF SIGNAL NAMES (diagram 9)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
+5CL	+5 V feedback	8	9
+5VDRV	+5 V drive signal	9	8
-8.5CL	-8.5 V feedback	8	9
-8.5VDRV	-8.5 V drive signal	9	8
ENVFDBK	Feedback for 50 Hz suppression	8	9
HRTC	Horizontal retrace	2	9
SNSRTN	Sense return	8	9
VFB-1	Feedback voltage	9	9
VSTART	Slow start voltage	9	9

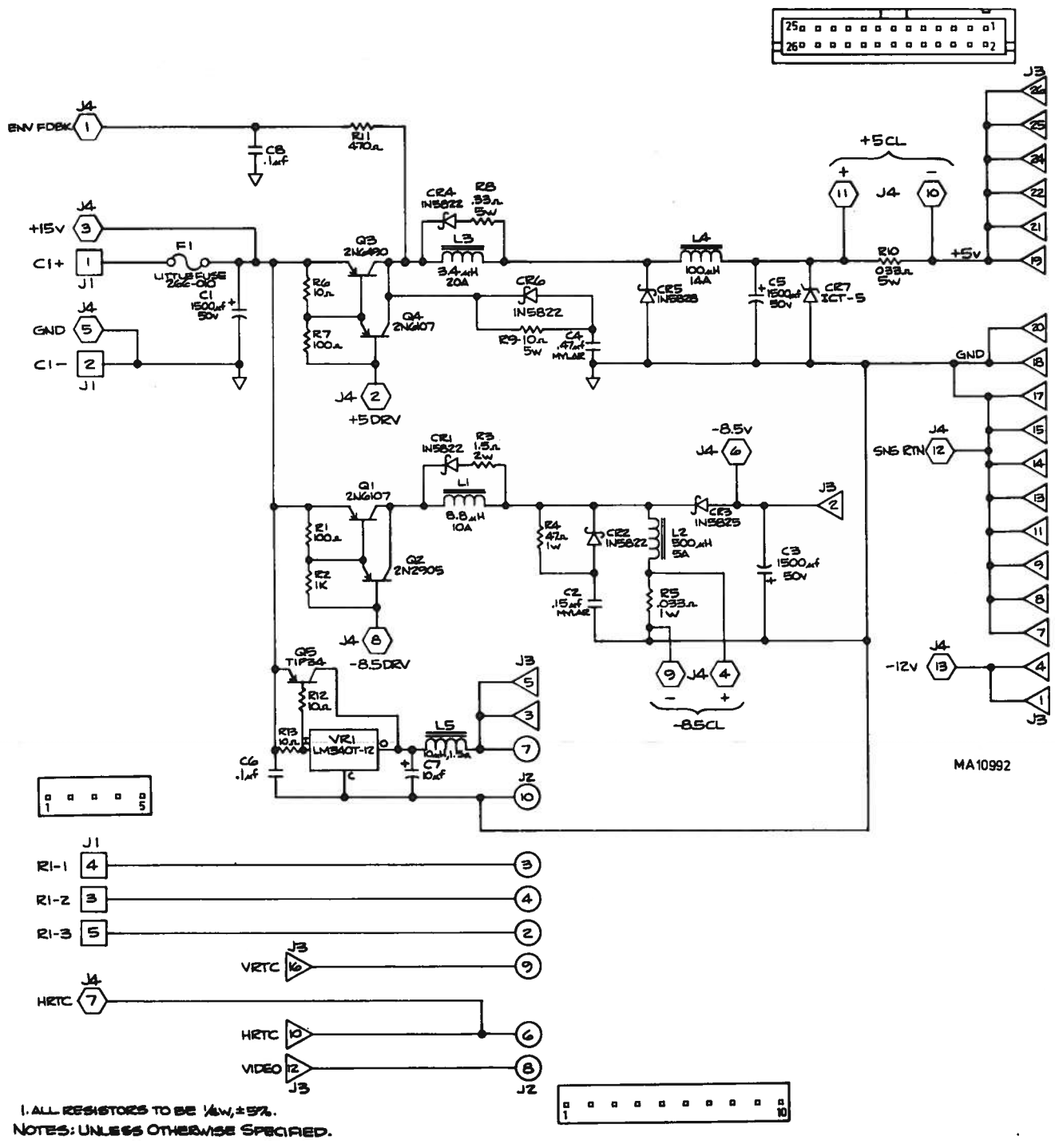
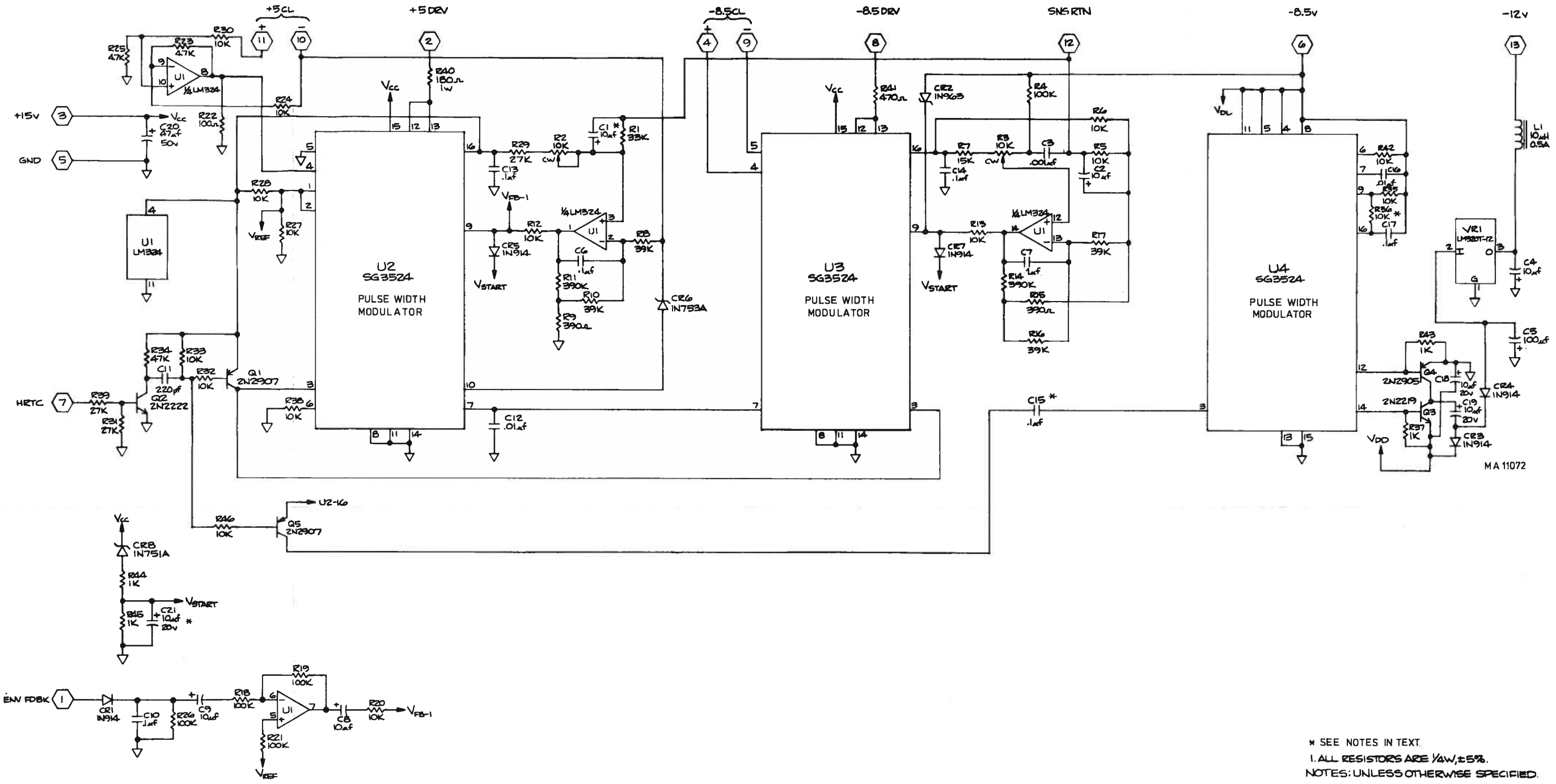


Figure 2.18 : Power supply, power board (8)



* SEE NOTES IN TEXT.

NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL RESISTORS ARE ¼W, ±5%.

Figure 2.19 : Power supply, control board (9)

2.5 PARTS LIST PM 3632, MAINFRAME

This list contains all components of the PM 3632 which are not standard.

Some p.c. boards or units are also available from Concern Service, however none of them is listed as a repairable!

NOTE: When ordering the capture board from Concern Service, you will receive the pc board without software. For ordering PROMs, contact the DTE Supply Centre Service Group.
NEDERLANDSE PHILIPS BEDRIJVEN B.V.
MIG S&I, T&M SERVICE DEPARTMENT DTE
BUILDING TQ V-2
EINDHOVEN

POSITION NUMBER	DESCRIPTION	ORDERING CODE
CAPTURE BOARD:		
Capture board, pc board		5322 219 80608
Integrated circuits:		
U37,45,59,60	74F194 SELECTED	5322 209 82418
U57	DELAY 50NS	5322 209 82417
U117	74LS00	5322 209 84823
U101	74LS04	4822 209 80783
U102	74LS08	5322 209 84995
U108	74LS10	5322 209 84996
U104,115	74LS32	5322 209 85311
U114	74LS74	4822 209 80782
U107	74LS86	5322 209 84997
U106	74LS109	5322 209 86522
U103	74LS138	5322 209 85647
U127,132	74LS156	4822 209 80446
U49	74F10	5322 209 81681
U105	74LS163	5322 209 85863
U110	74LS166	5322 209 86292
U119	74LS174	4822 209 81821
U50	74LS245	5322 209 86225
U112	74LS373	5322 209 86062
U24,48,62,63	74F00	5322 209 81534
U56,61,137	74F02	5322 209 81535
U47,128	74F04	5322 209 81577
U32	74F08	5322 209 81574
U129,30	74F20	5322 209 81537
U31,109	74F32	4822 209 82133
U116,123	74F64	5322 209 81538
U58	74F74	5322 209 81474
U39,40,125	74F109	5322 209 81669
U118	74F151	5322 209 81678
U53	74F153	5322 209 81575

POSITION NUMBER	DESCRIPTION	ORDERING CODE
U51,52,126	74F161	5322 209 82001
U41,42,54	74F163	5322 209 82851
U131	74F175	5322 209 81542
U36,64	74F244	5322 209 81128
U10,11,18,19	74F258	5322 209 81769
U26,27,34,35	74F258	5322 209 81769
U44,122	74F374	5322 209 81909
U13,14,21,22	74F399	5322 209 82852
U29,30,38,46	74F399	5322 209 82852
U1-9,17,25	IC 2149	5322 209 10528
U33,124	IC 2149	5322 209 10528
U120	IC 8085A	5322 209 86035
U15,16,134	IC 8155	5322 209 14563
U135,136	IC 8155	5322 209 14563
U133	IC 8276	5322 209 82849
U12,20,28,43	IC 29826	5322 209 82847
U65	74F158	5322 209 81532
U55	CRYSTAL 50 MHZ	5322 242 71206
U23	CRYSTAL 6.2016 MHZ	5322 242 71205
Semiconductors:		
CR01	1N914B	5322 130 31487
Q101	2N2222	5322 130 40221
Q12	2N2369	5322 130 44047
Various:		
C1	CAPACITOR 27PF	4822 122 30045
C4	VAR. CAP. 0-40 PF 250V	5322 125 50278
C5	CAPACITOR 6.8PF	4822 122 31049
L1	100NH CHOKE	5322 158 10682
RP6,101,102	RES. NETWORK 6K8	5322 111 90834
RP1 ... RP5	RES. NETW. 220E/330E	5322 111 90835
J101	CONNECTOR 16 PIN	5322 265 40453
J2	CONNECTOR 26 PIN	5322 265 51106
J3 ... J5	CONNECTOR 36 PIN	5322 265 61055
J6,7	CONNECTOR 25 PIN	5322 290 80648
J1	CONNECTOR 60 PIN	5322 265 61056

KEYBOARD:

Keyboard, pc board		Not available from C.S.
S1...S39	SWITCHES (CHROME)	5322 273 20207
U1	7407	5322 209 84761
H1	HORN	5322 240 30283
J1	CONNECTOR 16 PIN	5322 265 40453

POSITION NUMBER	DESCRIPTION	ORDERING CODE
POWER SUPPLY, POWER BOARD:		
Power board, pc board		5322 219 80609
Integrated circuits:		
VR1	LM340T-12	4822 209 81019
Semiconductors:		
CR3	1N5825	5322 130 32678
CR5	1N5828	5322 130 32679
Q2	2N2905	5322 130 40021
Q1,4	2N6107	4822 130 40903
Q3	2N6490	5322 130 42507
Q5	TIP 34	5322 130 44334
CR7	TRANSORB.5V 1.5 KW	5322 130 34762
CR1,2,4,6	IN5822	5322 130 32677
Various:		
L5	CHOKE 10UH 1.5A	5322 158 10675
L4	CHOKE 10UH 10A	5322 158 10677
L3	CHOKE 500UH 3.7A	5322 158 10678
L2	CHOKE 3.3UH 20A	5322 158 10679
L1	CHOKE 8.8UH 10A	5322 158 10681
C7	CAPACITOR 10 nF 16V	5322 121 42451
C6, C8	CAPACITOR 0.1 uF 50 V	5322 121 42448
C2	CAPACITOR 0.15 V	5322 121 42449
C4	CAPACITOR 470 nF 100 V	4822 121 41674
C3, C5	CAP. ELCO 1500 uF 25 V	4822 124 40432
C1	CAP. ELCO 1600 uF 40 V	5322 124 41083
R8	RESISTOR 0.33E 5 W	5322 113 60019
J1	CONNECTOR 5 PIN	5322 265 30394
J2	CONNECTOR 10 PIN	5322 265 40452
J4	CONNECTOR 26 PIN	5322 265 51107
F1	LITTLE FUSE 10 A	5322 253 14017
FOR VR1	TO-220 INSULATOR	5322 255 44103
FOR VR1	INSULATING WASHER #4	5322 532 54252
FOR VR1	NYLON NUT	5322 505 10777
FOR VR1	NYLON SCREW	5322 500 10342

POSITION NUMBER	DESCRIPTION	ORDERING CODE
POWER SUPPLY, CONTROL BOARD:		
Control board, pc board		5322 219 80611
Integrated circuits:		
VR1	LM320T-12	5322 209 82848
U2,3,4	SG3524	5322 209 81508
U1	LM324	4822 209 80587
Semiconductors:		
CR8	IN751A	4822 130 34233
CR6	IN753A	4822 130 34167
CR1,3,4,6,7	IN914B	5322 130 31487
Q3	2N2219	5322 130 40496
Q2	2N2222	5322 130 40221
Q4	2N2905	5322 130 40021
Q1,5	2N2907	5322 130 40218
Various:		
L1	CHOKE 10UH 0.5A	5322 158 10676
C11	CAPACITOR 220 pF	5322 122 32573
C12, C16	CAPACITOR 0.01 uF 50V	5322 121 42447
C3,6,10,13	CAPACITOR 0.1 uF 50V	5322 121 42448
C14,15,17	CAPACITOR 0.1 uF 50V	5322 121 42448
C1,2,4,8,9,18,19,21	CAPACITOR 10 uF 20V	5322 124 10508
C20	CAPACITOR 47 uF 63V	4822 124 20733
C5	CAPACITOR 100 uF 25V	4822 124 20701
R41	RESISTOR 470E 1/2 W	4822 116 52224
R40	RESISTOR 180E 1.2 W	4822 116 51095
R2, R3	POTENTIOMETER 10K	5322 101 20721

POWER SUPPLY, 'MAINFRAME PARTS'

Transformer 50/60 Hz	5322 148 80195
Zener diode 5KP28	5322 130 32902
Elco 8800 uF 40 VDC	5322 124 41082
Diode bridge	5322 130 32901
Power switch	5322 277 10846
Fan 115 V	5322 361 10321

POSITION NUMBER	DESCRIPTION	ORDERING CODE

CRT MODULE:

CRT unit (complete)		5322 219 80612

Philips replacements:
The numbers between brackets are the Philips replacement types.

Motorola CRT:		
IC201	TDA-1170S (TDA-1170S)	5322 209 86512
IC301, IC302	555 (NE555N)	4822 209 80775
Kaga CRT:		
Q101	2SC2229.0 (2SC22290)	4822 130 41511
Q102, Q401	2SC536 (2SC536C)	4822 130 41063
Q402, Q503	2SD600K (2SD600)	4822 130 41141
Q501, Q502	2SC930 (2SC930NPD)	4822 130 41597
Q504	2SC2373 (2SC2373L)	4822 130 41566
IC401	uPC1031H2 (UPC1031HA)	4822 209 80528
Audiotronix CRT:		
Q2	MPS-U03 (MPS-U03)	5322 130 44327
Q3	MPS-U05 (MPS-U05)	5322 130 44562
Q4	BU-406 (BU-406)	5322 130 44581
IC1	TDA1170S (TDA1170S)	3222 209 86512

MECHANICAL:

Option card retainer	5322 405 90284
Handle assembly	5322 498 70066
Cabinet bezel, front	5322 447 90448
Cabinet bezel, back	5322 447 90447
CRT bezel	5322 466 60976
Front panel	5322 447 90449
Back panel	5322 447 90451
Fan cover + filter	5322 447 90577
Top cover	5322 447 90578
Bottom cover	5322 447 90579

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NOTES:

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3. PODS. CIRUIT DESCRIPTION

3.1 GENERAL

This chapter describes all the pods which are available for use with the PM 3632.
Almost all pods can be repaired using this description and the diagnostic software (see also chapter 5). These pods, therefore, are not on stock at Concern Service. Spare pods can be ordered as a PM-number.
Exceptions to this, are the 16-bit microprocessor pods (PM 8874 and PM 8876). Only for these two pods, the repair procedure via C.S. can be used.

These descriptions do not include unit drawings, because all the part numbers are printed on the p.c. boards.

Figure 3.1 shows a block diagram of a 32 channel general purpose pod.
Block diagrams for all the other pods look very similar to this one:
some have less channels (4 channel fast pod), some have more clock connections (uP pods). The only exceptions on this are the ROM emulator pod and the 16-bit microprocessor pods. The sections that describe these pods, also contain the block diagrams of them.
Figure 1.2 shows an overall picture of how a pod is connected to the main system.

In all circuit desciptions, a * behind a signal name indicates that it is low active. In the diagrams, the corresponding signal name has a horizontal bar above it.

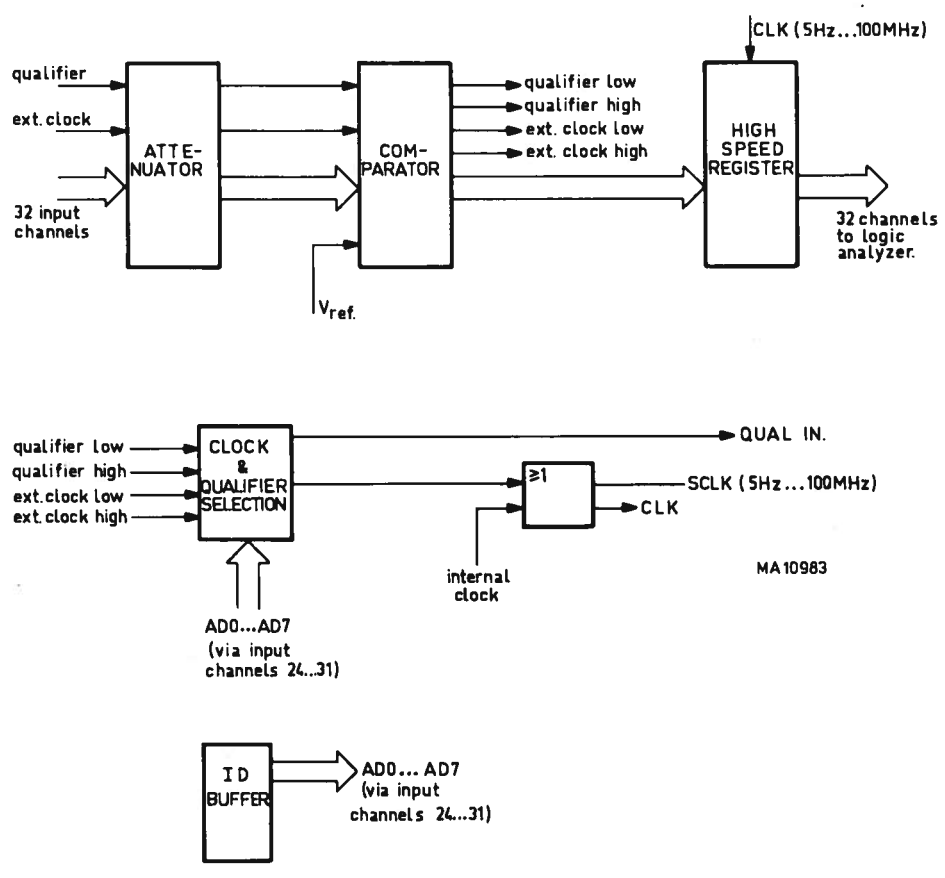


Figure 3.1 : pod block diagram.

Data, clock and qualifier signals are applied to the pod where it passes a (high input impedance) voltage attenuator. After this, the input signals are compared to a reference voltage (Vref), which is generated in the pod itself. The reference voltage is in some cases screwdriver adjustable (not for uP pods). The data is then clocked into a high speed buffer, and clock edges and qualifier levels are selected by the microprocessor in the mainsystem. The selection between internal and external clock is done in the pod also.

For writing control information to the pod (for clock edge and qualifier level), the microprocessor uses datalines 24-31.
Via these datalines, the microprocessor can also read the identity of the pod.

For generating the correct read/write signals and the signal to select int. or ext. clock, the microprocessor uses some control signals which are generated within the mainframe (not shown in the block diagram).

3.2 32 CHANNEL LOGIC POD (see figures 3.2 and 3.3)

The 32 channel logic pod (PM 8860) has 32 data channels, one clock channel and one qualifier channel (refer to figure 3.1 also :block diagram).

All data channels first pass an (high impedance) attenuater and are, after being compared to an internal reference voltage (V ref), registered by the selected clock (clock pulse CLK).
The clock channel is buffered similarly and it, or the clock from the mainframe, is used to clock the data into the register (in the pod,CLK) and to clock the input demultiplexers in the mainframe (clock pulse SCLK).
The qualifier channel is buffered similarly and is passed to the mainframe also (QUALIN).
The microprocessor selects the clock edge and the qualifier level.

For all data channels, the circuits are the same, therefore only channel 0 (probe 0) will be described here.

Data on Probe 0 is applied on pin 2 of P1B by the user connections (see figure 3.2).
RA, RB, CA, RE and CB attenuate this signal for comparison to an identically attenuated reference signal (Vref ; generated in the pod, U30, see below).
U4 performs this comparison, and its output is applied to U2, the input register. This register is clocked by the selected clock(signal CLK; comes from U29).
The buffered signal (SIG0) goes to the input demultiplexers in the mainframe via a shielded flat cable.
The other 31 data channels work in a very similar fashion.

NOTE:

The comparators in channels 0....7 are of the NE 522 type. The other channels (8...31, clock and qualifier) use the faster NE 521 comparator. Although channels 0...7 are used to for higher sampling speeds, the slower comparator is used meet the setup and hold time requirements.

The qualifier signal is processed similarly to the data channels.
Signal QUALIN is passed to the mainframe via the shielded flat cable,

and is active on the high level or low level of the input signal depending on selection signals HIQUAL* and LOQUAL.
CR6 and CR5 provide plus and minus reference voltages, RPI is used to develop 1.4 volts for the TTL reference, and R16 is set by the user to develop the variable threshold voltage.
U30 (pin 10) buffers the selected reference voltage, unless it is overridden by an externally applied low-impedance signal at pin 19 of P1B (8 channel probe set). The selected threshold voltage can also be measured at pin 19 of P1B.
RA and RB attenuate the reference voltage the same number of times as attenuaters in the data channels do. The reference voltage is then buffered to form the final reference at Pin 12 of U30 (V ref). This voltage is then used for a reference for the various comparators.

U17 (see figure 3.3) is the clock comparator and produces both senses of the thresholded clock.
Clock selection and driving are accomplished by enabling the desired sections of U33 or U29.
The clock from the mainframe (BFCLKOUT; buffered clock out) is applied to PIN 8 of U29, while inverted and noninverted versions, of the external clock (HIOUT and LOOUT; from U17) are applied to Pins 2 and 17 of U33.
The selected clock (SCLK) goes up to the mainframe, along with the data.
Clock select signals HICLK* and LOCLK* (low for rising edge or falling edge respectively) are driven from a latch (U21) which is written by the mainframe just prior to beginning to record. Data Lines 24-27 are used for this setup. The data register (U26) outputs are disabled at this time (via signal DATAEN*).
Selection of data qualifier sense is done similarly (via HIQUAL* and LOQUAL).

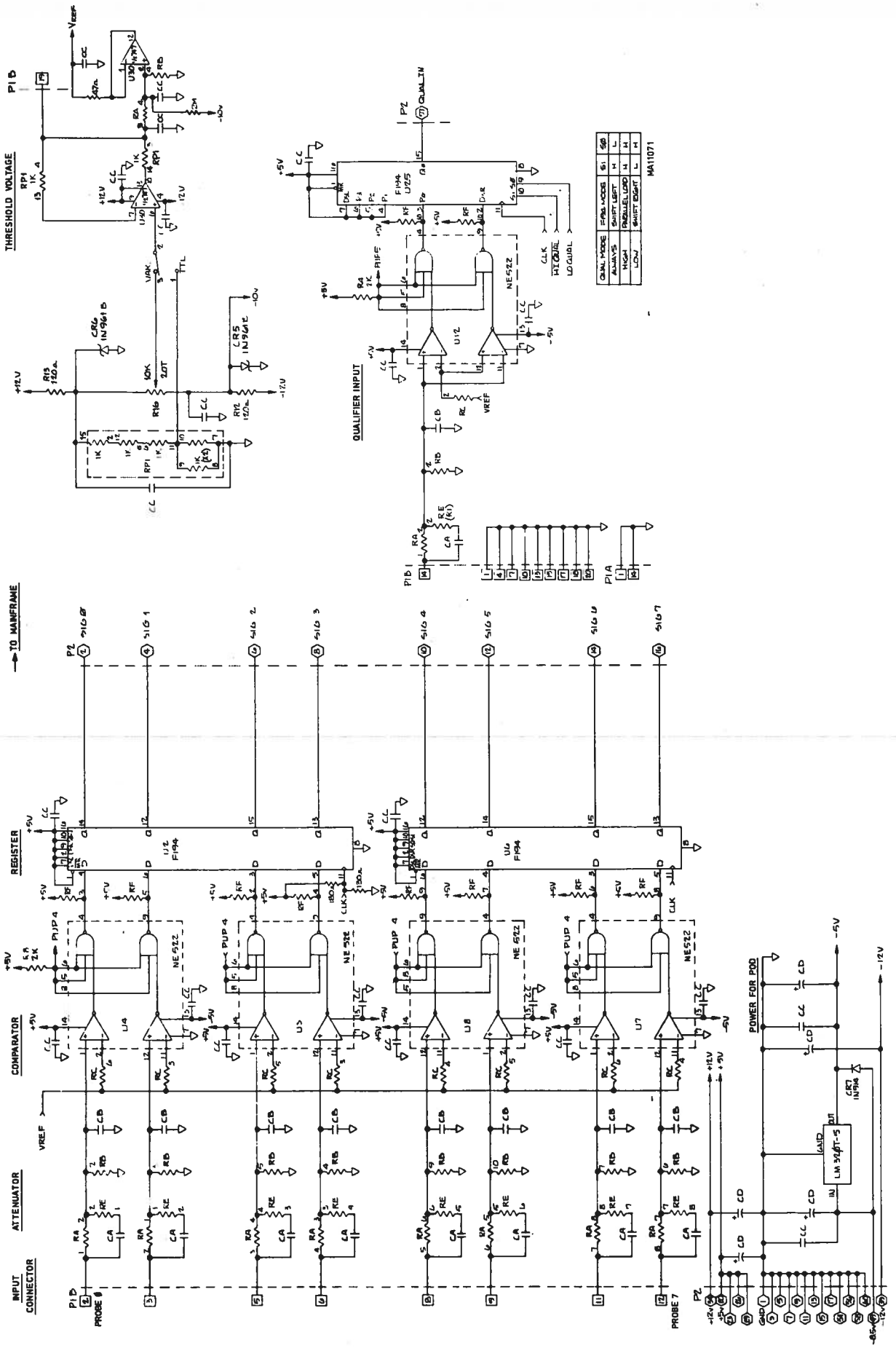
The microprocessor can read the identity of the pod by reading the contents of buffer U18/U22. This is done immediately after power-up.
This identity is read via data channels 24...31.
The data register (U26) outputs are disabled at this time (by signal DATAEN*).

For writing control data to the pod or reading the identity, the microprocessor applies three signals (BFPODSEL0..BFPODSEL2; buffered pod select) and the buffered write signal (BFPODWRT*) to the pod. These signals come from the special pod buffer on the capture board (U50, see figure 2.7).

LIST OF SIGNAL NAMES (diagram 10)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destignation (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
CLK	(selected) clock in pod	11	10
HIQUAL*	Select qualifier high	11	10
LOQUAL	Select qualifier low	11	10
QUALIN	Qualifier in signal	10	1,5
SIG 0	Input channel 0	10	1,5
SIG 1	Input channel 1	10	1,5
SIG 2	Input channel 2	10	1,5
SIG 3	Input channel 3	10	1,5
SIG 4	Input channel 4	10	1,5
SIG 5	Input channel 5	10	1,5
SIG 6	Input channel 6	10	1,5
SIG 7	Input channel 7	10	1,5
SIG 8	Input channel 8	10	1,5
SIG 9	Input channel 9	10	1,5
SIG10	Input channel 10	10	1,5
SIG11	Input channel 11	10	1,5
SIG12	Input channel 12	10	1,5
SIG13	Input channel 13	10	1,5
SIG14	Input channel 14	10	1,5
SIG15	Input channel 15	10	1,5
VREF	Reference voltage (threshold)	10	10,11



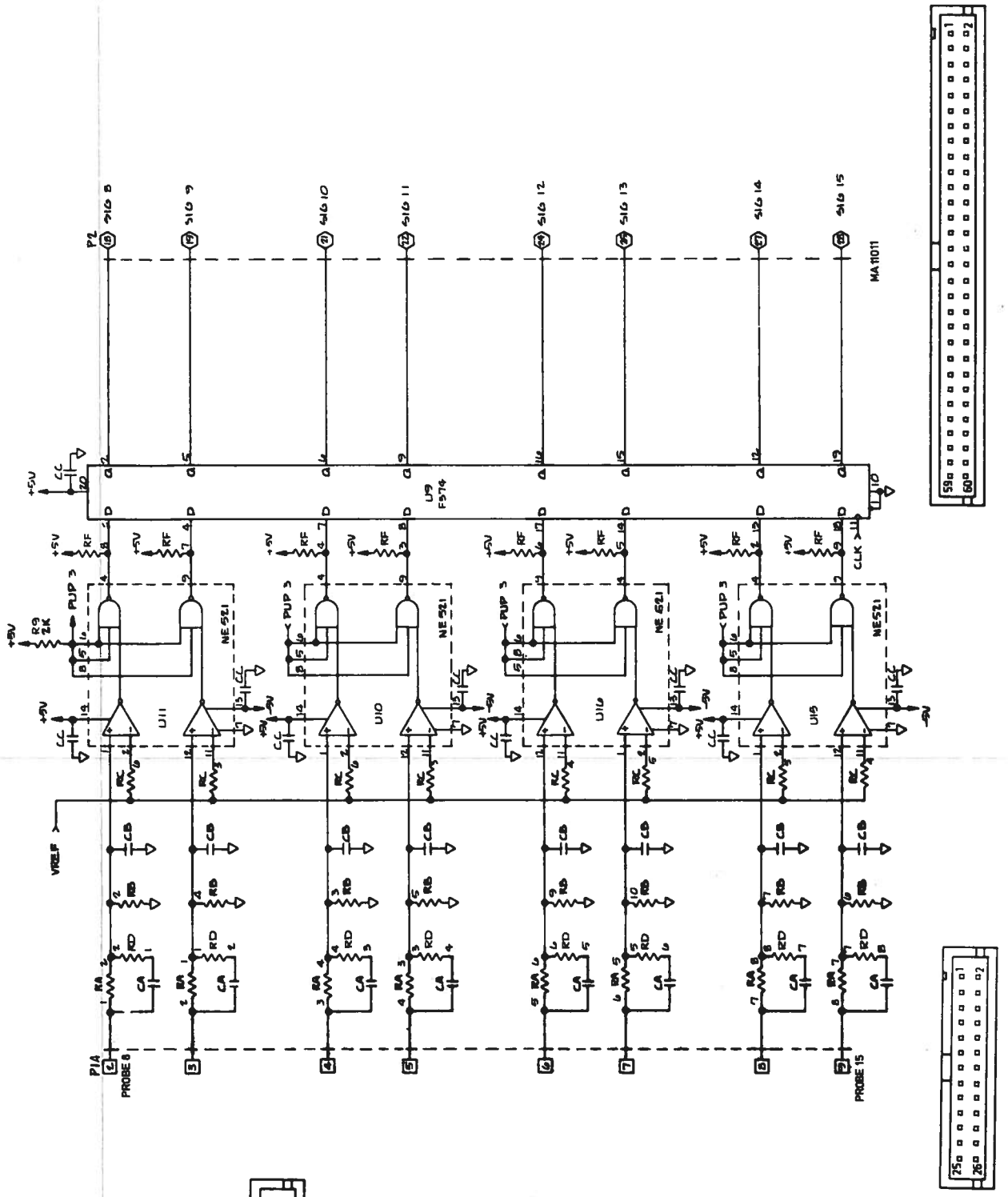
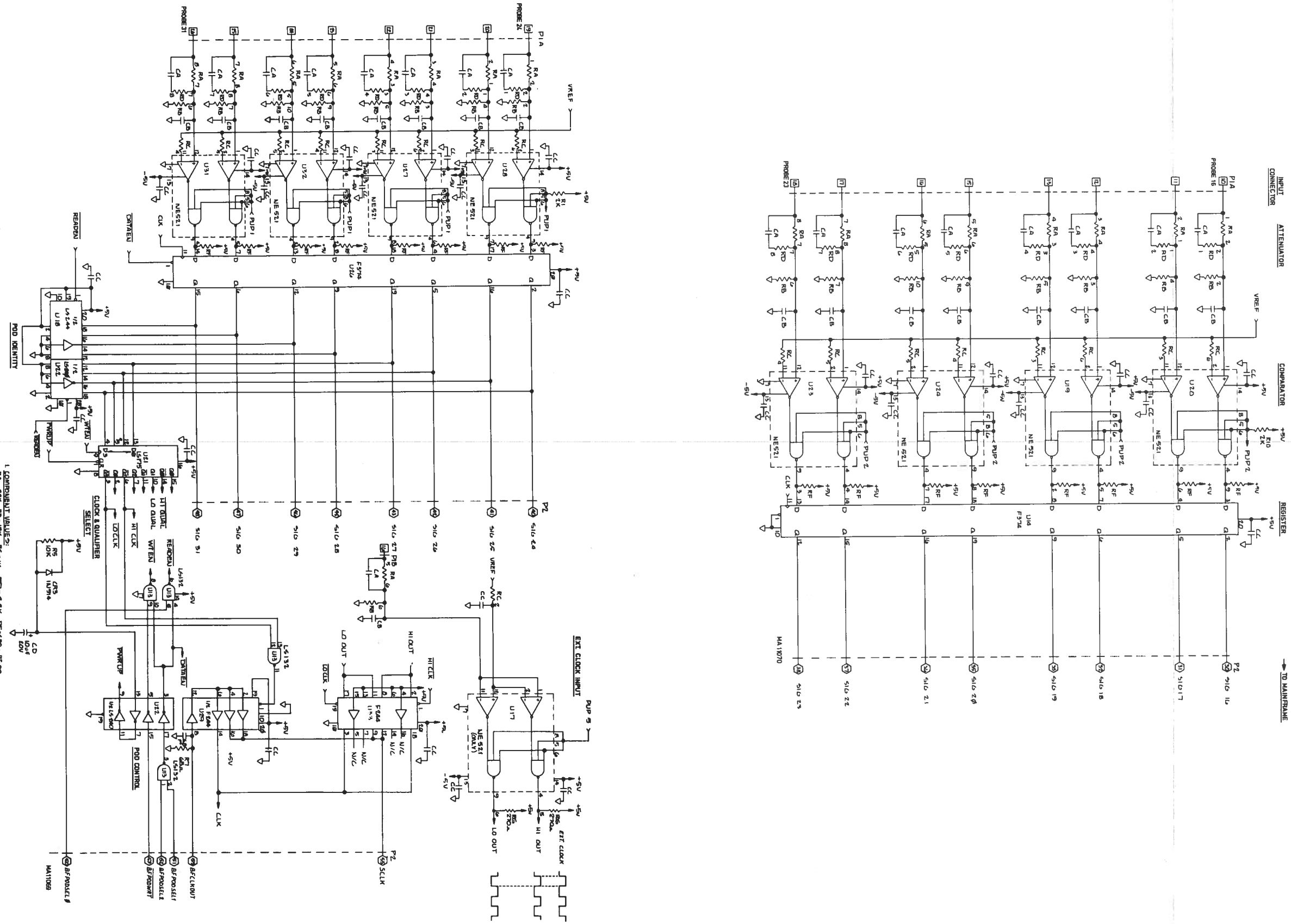


Figure 3.2: 32 channel logic pod; input channels 0...15 (10).

Figure 3.3: 32 channel logic pod; input channels 16...31 (11).



1. COMPONENT VALUE(S) SHOWN ARE: RA = 680Ω, RB = 680Ω, RC = 1K, RD = 2.5K, RE=680Ω, RF=0Ω
CA = 100pF, CB = 47pF, CC = 1nF, 50V, CD = 10uF, 20V

NOTE: UNLESS OTHERWISE SPECIFIED

LIST OF SIGNAL NAMES (diagram 11)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
BFCLKOUT	Buffered int. sampling clock, out	3	11
BFPODSEL0	Buffered pod select 0	3	11
BFPODSEL1	Buffered pod select 1	3	11
BFPODSEL2	Buffered pod select 2	3	11
BFPODWRT*	Buffered pod write	3	11
CLK	(selected) clock in pod	11	10,11
DATAEN*	Enable data register	11	11
HICLK*	Select rising edge ext. clock	11	11
HIOUT	high out (rising edge ext. clock)	11	11
HIQUAL*	Select qualifier high	11	10
LOCLK*	Select falling edge ext. clock	11	11
LOOUT	Low out (falling edge ext. clock)	11	11
LOQUAL	Select qualifier low	11	10
PWRUP*	Power up clear	11	11
READEN*	Enable id buffer read, 32 ch-pod	11	11
SCLK	Selected clock	11	1,5
SIG16	Input channel 16	11	1,5
SIG17	Input channel 17	11	1,5
SIG18	Input channel 18	11	1,5
SIG19	Input channel 19	11	1,5
SIG20	Input channel 20	11	1,5
SIG21	Input channel 21	11	1,5
SIG22	Input channel 22	11	1,5
SIG23	Input channel 23	11	1,5
SIG24	Input channel 24	11	1,3,5 BD
SIG25	Input channel 25	11	1,3,5 BD
SIG26	Input channel 26	11	1,3,5 BD
SIG27	Input channel 27	11	1,3,5 BD
SIG28	Input channel 28	11	1,3,5 BD
SIG29	Input channel 29	11	1,3,5 BD
SIG30	Input channel 30	11	1,3,5 BD
SIG31	Input channel 31	11	1,3,5 BD
VREF	Reference voltage (threshold)	10	11
WTEN*	Enable control buffer write	11	11

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3.3 4 CHANNEL FAST POD [see figures 3.5, 3.6 and 3.6]

The 4 channel fast pod (PM 8862) has 4 data channel, one clock channel and one qualifier channel.
It can be set to a normal capture mode or to a glitch capture mode.

For the block diagram, figure 3.1 can be used, although there are some differences.
All data signals first pass a (high impedance) attenuater.
After being compared with an internal reference voltage (Vref; generated in the pod), the data signals can pass the normal path or the glitch capture path before they are registered by the selected clock (CLK).
The normal mode is exactly the same as the data path in the 32 channel logic pod: after comparison, the data is directly registered.
In the glitch capture mode, the compared input signal is stretched to one sample period and then registred.
The clock signal is buffered similarly to the normal path and it, or the clock from the mainframe, is used to clock the input demultiplexers in the mainframe (clock pulse SCLK).
The qualifier signal is buffered similarly to the normal path and is passed to the mainframe also (signal QUALIN).
The microprocessor selects the clock edge, qualifier level and pod mode.

Because this pod must be very fast, the input circuits are implemented in ECL logic. Therefore, after the input circuits an ECL to TTL converter is necessary to present the correct signal levels to the mainframe.

Power for these ECL circuits is generated in the pod itself, and derived from the main power supply.

WARNING: THIS POD CONTAINS ECL CIRCUITS WHICH CAN DISSIPATE A LARGE AMOUNT OF HEAT. DO NOT USE IT IN ANY POSITION WHICH CAN OBSTRUCT THE NORMAL AIRFLOW AROUND IT.

For all data channels, the circuits are the same, therefore only channel 0 (Probe 0) will be described here.

Data on probe 0 is applied to pin 5 of connector J2 (see figure 3.5) by the user connections. RA1, RB1, CA and CB attenuate this signal for comparison to an identically attenuated reference voltage (Vref; generated in the pod by U13).
U14 performs this comparison and generates both senses of the input signal.
The noninverted sense is applied to the normal data path which only consists of a 2.0 ns delay line (DL3) -which compensates for the delay in the glitch mode- and a data register (U17).
Both senses are also applied to the glitch capture path:

- Positive going glitch (see figure 3.4).
  A low signal drives the clear input of flip-flop U19 high for an instant.
  The output of of U19 (Q) will stay low as long as the input signal is low (via U9). In this stable state, the set input stays low all the time (via U20).
  The output signal of flip-flop U19 is registred in U18 by the selected clock pulse (CLK, internal or external).
  When a positive going glitch appears, the set-input of U19 will go high for an instant via NOR-gate U20. Now register U18 will register a high level which makes the set-input of U19 low again (via NOR-gate U20), and makes the clear input high (via NOR-gate U9).
  Now register U18 will register a low level again (on the next clock pulse, CLK).
  Now the positive going glitch is stretched to one clock period.

- Negative going glitch.
  When the input signal is in a high state, a negative going edge is detected via the clear input of flip-flop U19.
  The rest of the procedure is the same as for a positive going glitch.

The selection between normal mode and glitch mode is done via signal GLITCH* and GLITCH (come from U24).

Then the data signals, either via the normal path or the glitch capture path is applied to an ECL to TTL converter (U16) which generataes the correct signal level for the input demultiplexers.
Buffer U15 drives the signal on the shielded flat cable (SIG0).
The delay (6.0 ns) in front of the ECL to TTL converter compensate for the delay in the clock and qualifier channels.

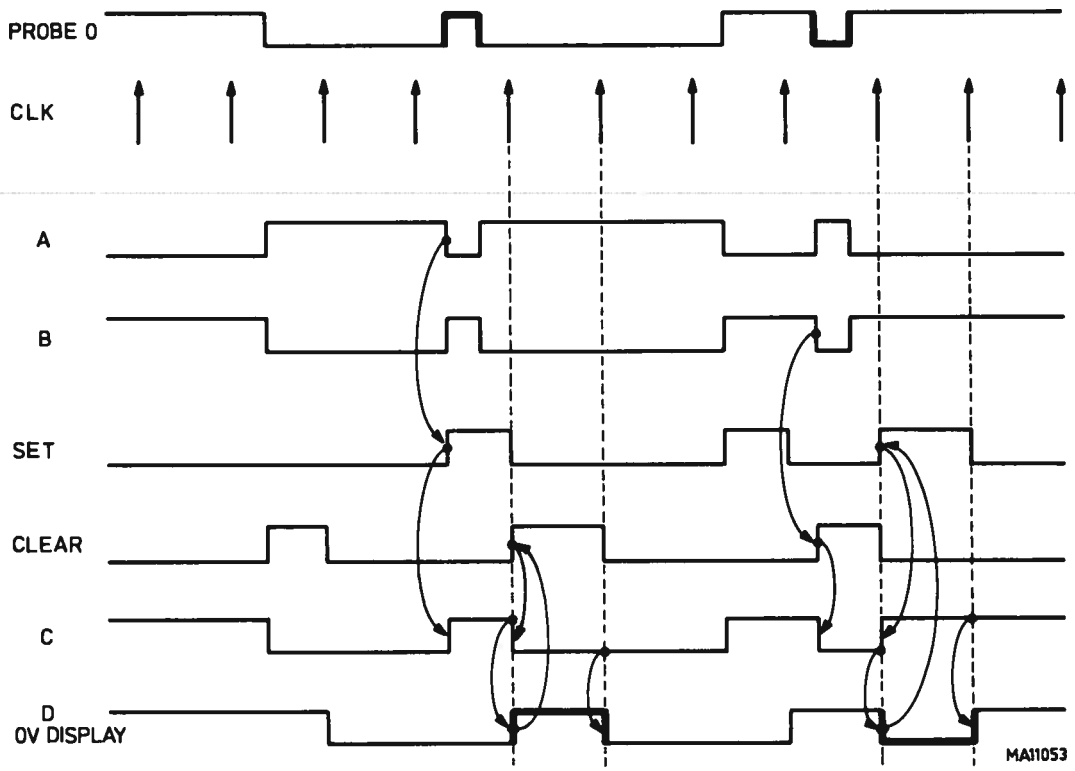

Figure 3.4: Glitch capture, timing diagram.

The qualifier signal is buffered similarly to the data signals (see figure 3.6).
The comparator (U12) also generates both senses of the qualifier signal, which are then delayed by means of flip-flop U8 (compensates for delay in data inputs).
The selection of the active level of the qualifier is done by means of signals HIQUAL, LOQUAL and NOR gates U9.
The output of U9 are wired-ored which means that one of the outputs must be high to make the D-input of U17 and U18 high.
U17 and U18 register the qualifier status before it is converted to TTL and put on the shielded flat cable to the mainframe (signal QUALIN).

The clock signal is buffered similarly to the data and qualifier signals.
Comparate U10 generates both clock senses.
The selection between rising edge or falling edge is done with relais K2, by means of signal LOEXTCLK (low external clock; high for falling edge).
The sense of the clock signal that is not used is shorted to ground via U7 to prevent the occurrence of capacitive coupling in the relais.
Relais K1 selects between the internal sampling clock (BFCLKOUT; buffered clock out, from the mainframe) or the external clock. The switching is done with signal INTCLK* (internal clock).
The clock signal is then converted to TTL level and passed to the mainframe for clocking the input demultiplexers (SCLK).

Timer U11 is used to disable the clock circuit for 4 msec during the settle time of the relais, (via pin 4 of the comparators).
Timer U24 is used to set the qualifier signal (QUALIN) high for another 4 msec after the clock circuit is enabled in order to provide a stable clock signal to to the demultiplexers in the mainframe.

NOTE:
The software in the mainframe doesn't accept the first 8 msec of data after the clock circuit is enabled (this to compensate for the qualifier signal which is higher for 4 msec).
Note that this, in combination an unstable clock as described above, can cause some problems in case of very slow external clock speeds!!

The microprocessor can read the identity of the pod by reading the contents of buffer U3. This is done via data channels 24...31.

For reading the identity, and writing some control information to the pod (clock selection, clock & qualifiers suppression) the microprocessor applies signals BFPODWRT* (buffered pod write) and BFPODSELO (buffered pod select) to the pod. These signals come from buffer U50 in the mainframe (see figure 2.7)

The reference voltage for the comparators is generated via operational amplifiers U13 (see figure 3.6).
Switch S1 selects between the fixed TTL voltage -derived from the +12V supply via R30, R31-, or the variable threshold voltage.
The threshold voltage can be measured at connector J2 (data input connector).

Power for the ECL circuits is generated in the pod itself.
The -5.2V and -4.5V are directly derived from the -12V supply.
U2 is used as a switching control circuit, which runs at a frequency determined by C12 and R18.

Outputs 12,13 provide the switching signal for the output transistors.
The -5.2 V output is fed-back to the control circuit (pin 2) where it is compared with a reference voltage (R28, CR6 andassociated components).
The -2V is derived from the +5 V supply.
U6 is used as a switching control circuit which loads energy into coil L1 when transistor Q2 is switched-on. When Q2 is switched-off coil L1 discharges its energy via CR3 and R15, wich results in a negative voltage (-2 V).
The frequency of the switching is determined by C7 and R17.
The -2 V output voltage is fed-back to the control circuit where it is compared with a reference voltage (derived from pin 16 of U6, +5V).
The difference between the feedback signal and the reference voltage affects the duty cycle of the output signal.

LIST OF SIGNAL NAMES (diagram 12)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
CLK	(selected) clock in pod	13	12
GLITCH	Select non-glitch mode	13	12
GLITCH*	Select glitch mode	13	12
SIG 0	Input channel 0	12	1,5
SIG 1	Input channel 1	12	1,5
SIG 2	Input channel 2	12	1,5
SIG 3	Input channel 3	12	1,5
VBB		12	--
VREF	Reference voltage (threshold)	14	12

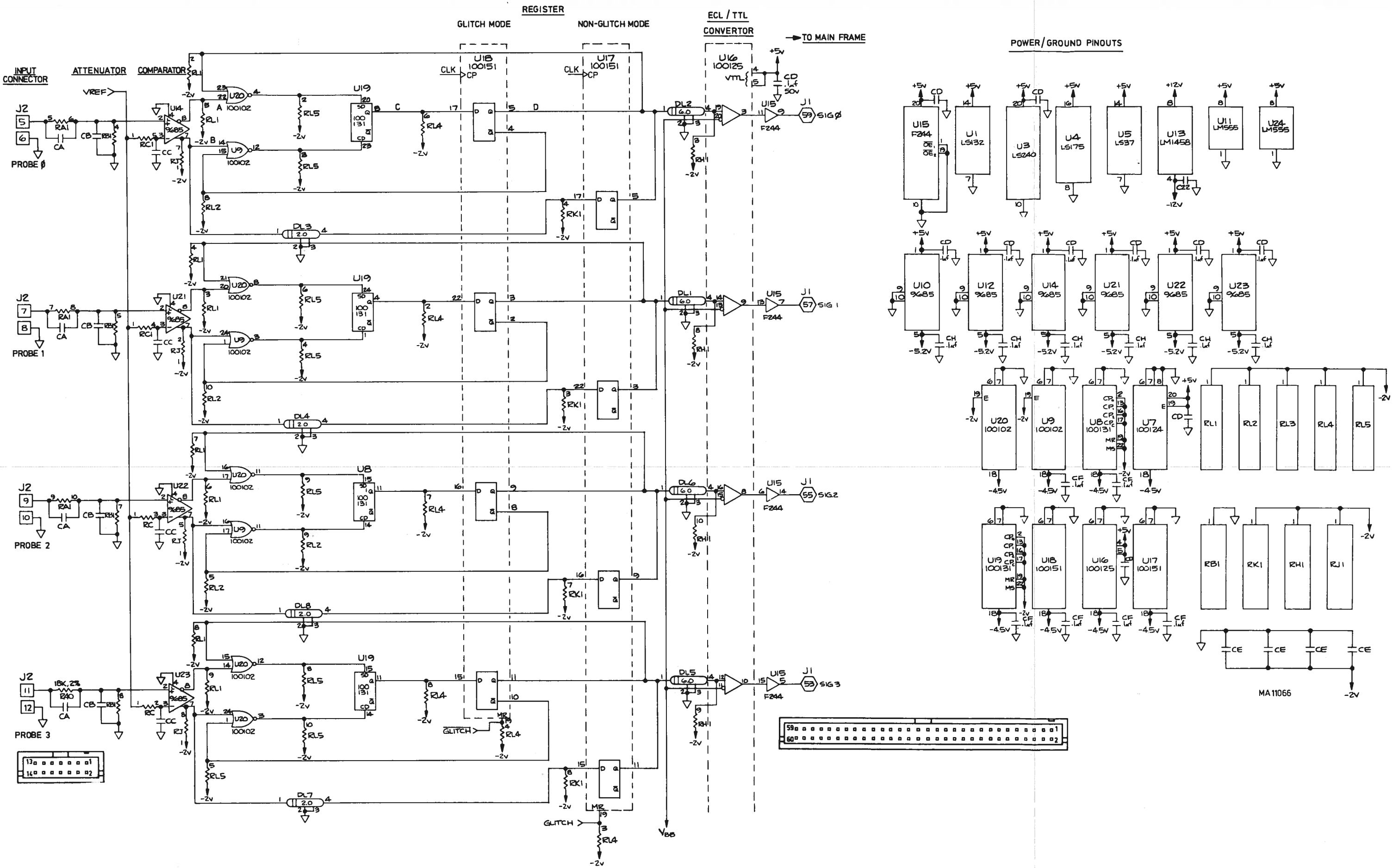

Figure 3.5 : 4 channel fast pod; data channels (12)

Figure 3.6 : 4 channel fast pod; clock & qualifier input, and power supply (13).

LIST OF SIGNAL NAMES (diagram 13)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
BFCLKOUT	Buffered int. sampling clock, out	3	13
BFPODSEL0	Buffered pod select 0	3	13
BFPODWRT*	Buffered pod write	3	13
CLK	(selected) clock in pod	13	12
GLITCH	Select non-glitch mode	13	12,13
GLITCH*	Select glitch mode	13	12,13
INTCLK*	Select int./ext. clock	13	13
LOEXTCLK	Select low/high ext. clock	13	13
QUALIN	Qualifier in signal	13	1,5
SCLK	Selected clock	13	1,5
SIG24	Input channel 24	13	1,3,5 BD
SIG25	Input channel 25	13	1,3,5 BD
SIG26	Input channel 26	13	1,3,5 BD
SIG27	Input channel 27	13	1,3,5 BD
SIG28	Input channel 28	13	1,3,5 BD
SIG29	Input channel 29	13	1,3,5 BD
SIG30	Input channel 30	13	1,3,5 BD
SIG31	Input channel 31	13	1,3,5 BD
VREF	Reference voltage (threshold)	14	13
VSET	Threshold voltage (molex conn.)	13	not used

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3.4 ROM EMULATOR POD (figures 3.7 and 3.8)

The ROM emulator pod can only be used in conjuntion with the RS232C control card. The pod connects to this card via one 15-pole connector (refer also to figure 1.2 : PM 3632 block diagram).
The RS232C control card is used for transferring data from the mainframe to the ROM emulator pod via a serial link (not the RS232C connection!).
It also generates the necessary control signal for the ROM emulator pod.
The RS232C control card is also used for uploading or downloading of data from or to the ROM emulator pod. This is done via the RS232C serial link (in hex format).

The ROM emulator pod can emulate up to 16 K byte of PROM (2716, 2732, 2764, 27128).
Two pods can be daisy chained in which case a total of 32 K bytes of PROM can be emulated.
Each pod contains eight 2K RAMs.

The ROM emulator pod is connected to the RS232C control card via connector P1 (see figure 3.7).
Via this connector, the RS232C C card can pass some control signals to the pod (under control of the microprocessors):

- BCLK (buffered clock): clock signal for filling the input buffers in the pod or for shifting data out of the input buffers to the RS232C control card.
- BCTL0,1 (buffered control lines): set the pod in read write or emulation mode.
- SELECT (pod select) : two lines are used to select one of the two ROM emulator pods.

Via this connector, the RS232C C control card can write data into the RAMs in the pod via a serial link (BDOWN; buffered data down) or read data out of the RAMs via a serial link (SELDAT; selected data (up)).
All signals can go to a second pod also, via connector P2, which can be connected to connector P1 of the second pod also. An exception is the serial data that goes up to the RS232C card, which can be from the first or the second pod.

Write data into the RAMs:
The serial data (1 byte) + addres (2 bytes) come in via line BDDWN (buffered data down) and is clocked into shift register U9, U17 and U18 on clock pulse BCLK (buffered clock). During this, signal RDMOD* (read mode) puts the register in the shift right mode, and signal INTL* (internal mode) enables the outputs.
When the data + addresses are available in parallel, signals IA11, IA12 and IA13 (internal address lines) are decoded to select one of the 8 RAMs (via decoder U8, see figure 3.8) which causes a write of the data to the selected address in the RAM (signals IWE0...IWE7).

Read data out of RAMs:
The serial address 2 bytes is clocked into shift registers U9 and U17 on clock pulse BCLK (buffered clock) via line BDDWN (buffered data down).
Control signals are the same as described above, and signals IA11, IA12 and IA13 are decoded to point out one of the eight RAMs (signals IOE0... IOE7:output enable via U7, see figure 3.8).

After this, the data on that address is loaded into U18 (LD0..LD8) and then shifted out in series on clock pulse BCLK into shift register U11.

Signal ISDAT (internal serial data) goes via U3 (see figure 3.8) to U12 where is is called SELDAT (selected data). SELDAT goes via the RS232C control card to the microprocessor.
In case a second pod is connected, the read-data from this pod (XSDAT) will go via U3 where it is called SELDAT via connector P1 to the RS232C control card.

Pod in emulation mode:
In this mode, the RAM are disconnected from the mainframe and are filled with the necessary data. The RAMs are now under control of the system under test.
For connection to the system under test, four connectors are available, labelled A, B, C and D.
The following table shows which connector can be used in the different modes.

label:	connector:	modes:
A	P3	2716, 2732, 2764, 27128
B	P4	2716, 2732, 27128
C	P5	2716, 2732, 2764
D	P6	2716, 2732

As shown above, a 2716 or 2732 can be plugged-in at any connector.
The target supplies addresslines, data lines, chip enables and output enables to the RAMs in the pod.

2716 in A or B: Only A is described here, because both are very similar.
The adresslines (XA0..XA10) are applied directly (via U24, U25) to both RAMs which are dedicated to connector A (U13 and U14). These buffers are only enabled in the emulation mode via signal EXTL*. When the target activates the chip enable and/or output enable signals (XCE* and XOE*):
1. multiplexers U26, U27 are enabled to transfer data from U13 to P3. This is done via signal XOELO* (via U28, U29). The multiplexer is set in the correct direction by the microprocessor via signal MODE1 (low; see table in figure 3.8).
2. the output enable signals for the RAMs (IOE0 and IOE1) are generated via signal XEN1 which selects RAMs U13, U14 or RAMs U15, U16. Signal XEN1 goes to U2 to generate the correct output enable signals for the RAMs (via U7, see figure 3.8).
XEN1 is always low for 2716 in A. XEN1 is high when 2716 in B is enabled.

2716 in C or D: Only C is described here, because both are very similar (see figure 3.8).
The address lines (XA0...XA10) are applied directly (via U24,U25) to both RAMs, which are dedicated to connector C (U20 and U21).
When the target activates the chip enable and/or output enable signals (via pin 11 and 15 of P5):
1: Buffer U30 is enabled: the data bus of the system under test is connected to the RAM outputs.

2: The output enable signals for the RAMs
(IOE4 an IOE5 are generated via signal
XEN3 which selects either RAMs U20, U21
or RAMs U22, U23. Signal XEN3 goes to U2
to generate the correct output enable
signals for the RAMs (via U7).
XEN3 is always low for 2716 in C. XEN3 is high when
2716 in D is enabled.

2732 in A, B, C or D: This mode of operation is exactly the same as the above described 2716 operation. The only differences is that addressline XA11 is used to make a selection between the upper or the lower 2 K of RAM which is dedicated to each connector.
This selection is done via U7 (see figure 2.9) which generates the correct output enable signals (IOE0...IOE7) for the RAMs.

2764 in A or C: This mode of operation is very similar to the 2716 in A operation.
The difference is that two extra address lines (XA11 and XA12) are used to select one of the 4 RAMs. This is done via the selection circuit U2, U7 and associated components (see figure 3.8).
Signals XEN1 and XEN3 are not used for RAM selection anymore.

27128 in A or B: This mode of operation is very similar to the 2716 in A or B operation.
The difference is that now three extra address lines (XA11, XA12, XA13) are used to select one of the 8 RAMs. This is done via the selection circuit U2, U7 and associated components (see figure 3.8).
Signals XEN1 and XEN3 are not used for RAM selection anymore.
Another difference is that when the data is read out of RAMs U20, U21, U22 or U23, multiplexers U26, U27 (see figure 3.7) are set to a different direction; the data that is now passed to the system under test comes from HD0...HD7.

RAM selection circuitry:

The output enable signals for the RAMs are generatad by U2, U7 and associated components.
This circuitry is controlled by control signal SCTL1, the mode selection (MODE) signals and some address lines from the system under test or the microcomputer in the mainframe (IA11, IA12, IA13 come from U24, U25).
Multiplexer U2 can be set to the 2716/2732 or the 2764/27128 modes, depending on the MODE0 and MODE1.

Mode selection signals:

As shown in the two tables in figure 3.8, the ROM emulator pod can operate in an internal or an emulation mode.
In the internal mode some control signals (SCTL) determine the action that has to be performed (read, write or hold & shift right).

The mode is stored in shift register U4 by clocking a data byte into this register on clock pulses BCLK (buffered clock) via the serial link (BDDWN; buffered data down). This however can only be done when the pod is selected (signal SELECT*).
The MODE signals select registers (U9, U7, U18) and the address buffers (U24, U25) via signals INTL*, EXTL*.
The control signals (BCTL0, BCTL1; come from U12) which drive multiplexer U3 determine which operation can be performed by the pod: read data or write data.

Pod connection errors:
If the pod is connected correctly to the system under test is detected by Q1 and associated components (connector A).
The microprocessor can read (via XSTS0A, XSTS0B; go to shift register U11) if the supply voltage (XPWR0) of the system under test is connected to the correct pin at connector A. If not, the analyzer will display "POD CONNECTION ERRROR" on the screen.
If it is connected in the correct way, FET Q1 will connect system ground to mainframe ground. If the connection is wrong, FET Q1, doesn't make that connection: The message POD CONNECTION ERROR will appear at the screen.

Reading pod identity.
When powering up the PM 3632, the microprocessor reads the identity of the ROM emulator pod by sending data to shift registers U9, U17, U18 via the serial link (BDDWN) on the RS232C control card, and afterwards read the same data back via shift register U11 and the same serial link (SELDAT).

LIST OF SIGNAL NAMES (diagram 14)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
BCLK	Buffered Rom emulator clock	14	14,15
BCTL0	Buffered control line 0	14	15
BCTL1	Buffered control line 1	14	15
BDOWN	Buffered data down	14	14,15
BSELOAT	Buffered serial data up	14	22
CTL0	Control line 0	22	14
CTL1	Control line 1	22	14
DDWN	Data down (to Rom emulator)	22	14
ECLK	Rom emulator clock	22	14
EXTL*	Select external (emulation) mode	15	14
HD0	Rom emulator data 0	15	14 BD
HD1	Rom emulator data 1	15	14 BD
HD2	Rom emulator data 2	15	14 BD
HD3	Rom emulator data 3	15	14 BD
HD4	Rom emulator data 4	15	14 BD
HD5	Rom emulator data 5	15	14 BD
HD6	Rom emulator data 6	15	14 BD
HD7	Rom emulator data 7	15	14 BD
IA 0	Addressline 0 (internal source)	14	15
IA 1	Addressline 1 (internal source)	14	15
IA 2	Addressline 2 (internal source)	14	15
IA 3	Addressline 3 (internal source)	14	15
IA 4	Addressline 4 (internal source)	14	15
IA 5	Addressline 5 (internal source)	14	15
IA 6	Addressline 6 (internal source)	14	15
IA 7	Addressline 7 (internal source)	14	15
IA 8	Addressline 8 (internal source)	14	15
IA 9	Addressline 9 (internal source)	14	15
IA10	Addressline 10 (internal source)	14	15
IA11	Addressline 11 (internal source)	14	15 ?
IA12	Addressline 12 (internal source)	14	15 ?
IA13	Addressline 13 (internal source)	14	14 ?
IA13	Addressline 13 (internal source)	14	14 ?
IA13	Addressline 13 (internal source)	14	15 ?
IOE0*	Output enable, (internal) RAM 0	15	14
IOE1*	Output enable, (internal) RAM 1	15	14
IOE2*	Output enable, (internal) RAM 2	15	14
IOE3*	Output enable, (internal) RAM 3	15	14
ISOAT	(internal) Serial data up	14	15
IWE0*	Write enable, (internal) RAM 0	15	14
IWE1*	Write enable, (internal) RAM 1	15	14
IWE2*	Write enable, (internal) RAM 2	15	14
IWE3*	Write enable, (internal) RAM 3	15	14
LD0	Rom emulator data 0	14	14,15 BD
LD1	Rom emulator data 1	14	14,15 BD
LD2	Rom emulator data 2	14	14,15 BD
LD3	Rom emulator data 3	14	14,15 BD
LD4	Rom emulator data 4	14	14,15 BD
LD5	Rom emulator data 5	14	14,15 BD
LD6	Rom emulator data 6	14	14,15 BD
LD7	Rom emulator data 7	14	14,15 BD
MODE 1	mode 1 select	15	14
ROM00*	Select read mode	15	14

LIST OF SIGNAL NAMES (diagram 14, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
SEL0	Select line 0	22	14
SEL1	Select line 1	22	14
SELDAT	Serial data up (to mainframe)	15	14
SELECT*	Select line	14	15
STSL00*	Load connection test data	15	14
VREF	Reference voltage (threshold)	14	12,13
XA 0	Addressline 0 (external source)	14,15	14 ?
XA 1	Addressline 1 (external source)	14,15	14 ?
XA10	Addressline 10 (external source)	14,15	14 ?
XA11	Addressline 11 (external source)	14,15	14 ?
XA12	Addressline 12 (external source)	14,15	14 ?
XA13	Addressline 13 (external source)	14,15	14 ?
XA 2	Addressline 2 (external source)	14,15	14 ?
XA 3	Addressline 3 (external source)	14,15	14 ?
XA 4	Addressline 4 (external source)	14,15	14 ?
XA 5	Addressline 5 (external source)	14,15	14 ?
XA 6	Addressline 6 (external source)	14,15	14 ?
XA 7	Addressline 7 (external source)	14,15	14 ?
XA 8	Addressline 8 (external source)	14,15	14 ?
XA 9	Addressline 9 (external source)	14,15	14 ?
XCE0*	Chip enable, port A (ext. source)	14	14
XCE1*	Chip enable, port B (ext. source)	14	14
XCOM0	Ground on port A (ext. source)	14	15
XCOM1	Ground on port B (ext. source)	14	15
XEN0	Select RAM for port A (ext.source)	14	not used
XEN1	Select RAM for port B (ext.source)	14	15
XOE0*	Output enable, port A (ext.source)	14	14
XOE1*	Output enable, port B (ext.source)	14	14
XOELO*	Enable multiplexer output	14	14
XPWR0	Power on port A (ext. source)	14	15
XPWR1	Power on port B (ext. source)	14	15
XSDAT	Serial data up (from second pod)	14	15
XSEL	Select multiplexer direction	14	14
XSTS0A	Conection test, port A	15	14
XSTS0B	Conection test, port A	15	14
XSTS1A	Conection test, port B	15	14
XSTS1B	Conection test, port B	15	14
XSTS2A	Conection test, port C	15	14
XSTS2B	Conection test, port C	15	14
XSTS3A	Conection test, port D	15	14
XSTS3B	Conection test, port D	15	14

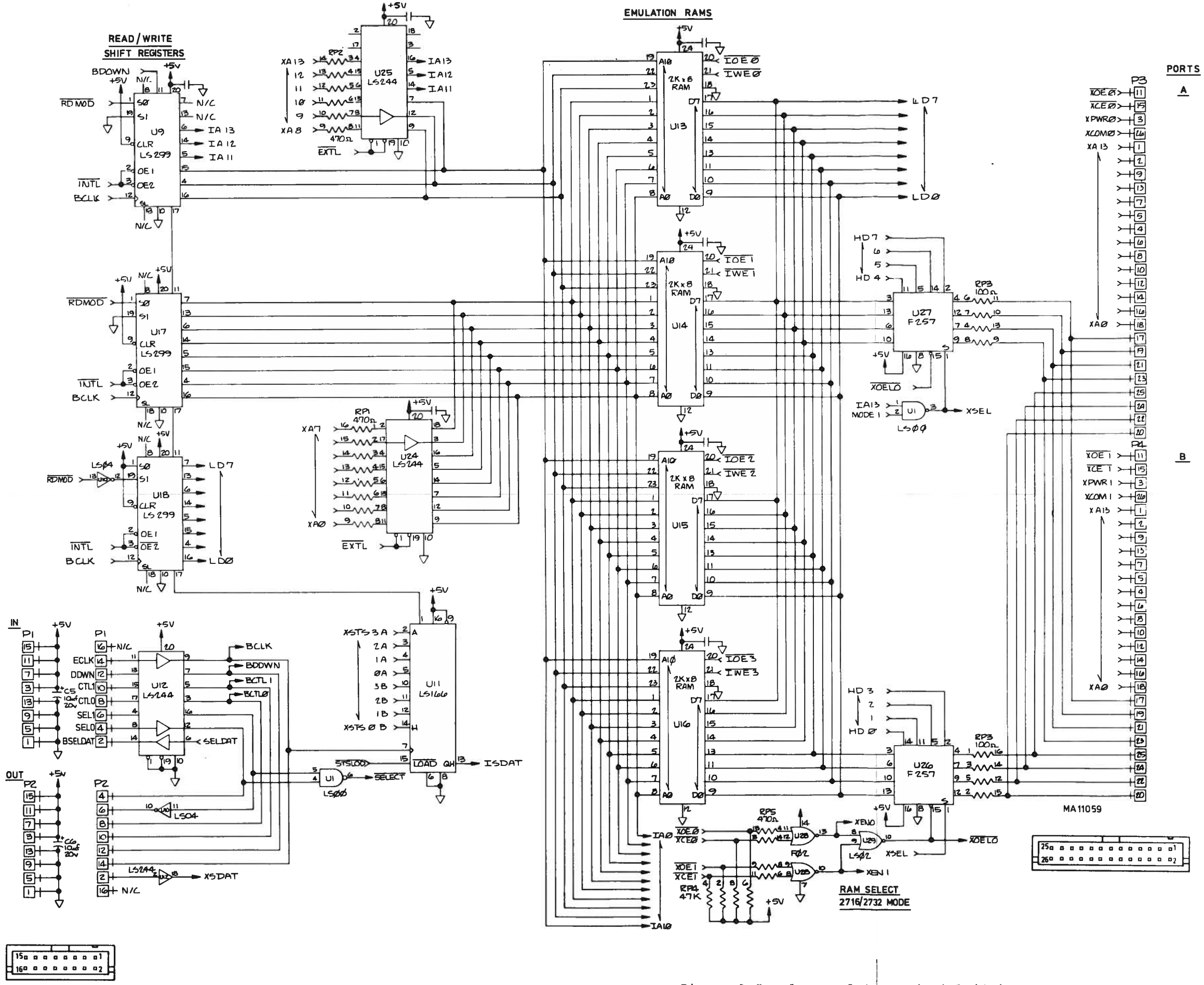
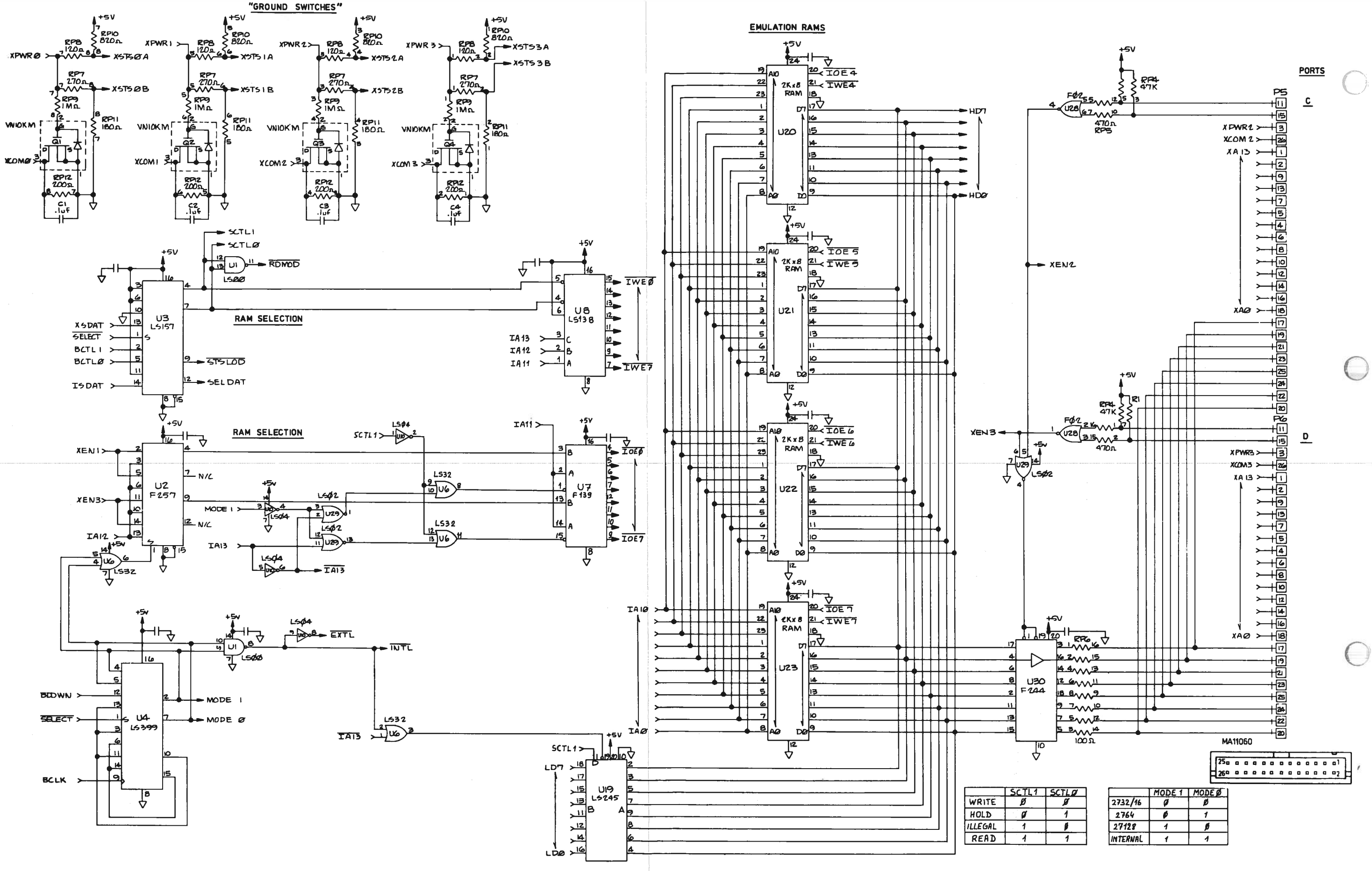


Figure 3.7 : Rom emulator pod; A,B (14)



	SCTL1	SCTL0
WRITE	0	0
HOLD	0	1
ILLEGAL	1	0
READ	1	1

	MODE 1	MODE 0
2732/16	0	0
2764	0	1
27128	1	0
INTERNAL	1	1

Figure 3.8 : Rom emulator pod: C,D (15)

LIST OF SIGNAL NAMES (diagram 15)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
BCLK	Buffered Rom emulator clock	14	15
BCTL0	Buffered control line 0	14	15
BCTL1	Buffered control line 1	14	15
BDDWN	Buffered data down	14	15
EXTL*	Select external (emulation) mode	15	14
HD0	Rom emulator data 0	15	14 BD
HD1	Rom emulator data 1	15	14 BD
HD2	Rom emulator data 2	15	14 BD
HD3	Rom emulator data 3	15	14 BD
HD4	Rom emulator data 4	15	14 BD
HD5	Rom emulator data 5	15	14 BD
HD6	Rom emulator data 6	15	14 BD
HD7	Rom emulator data 7	15	14 BD
IA 0	Addressline 0 (internal source)	14	15
IA 1	Addressline 1 (internal source)	14	15
IA 2	Addressline 2 (internal source)	14	15
IA 3	Addressline 3 (internal source)	14	15
IA 4	Addressline 4 (internal source)	14	15
IA 5	Addressline 5 (internal source)	14	15
IA 6	Addressline 6 (internal source)	14	15
IA 7	Addressline 7 (internal source)	14	15
IA 8	Addressline 8 (internal source)	14	15
IA 9	Addressline 9 (internal source)	14	15
IA10	Addressline 10 (internal source)	14	15
IA11	Addressline 11 (internal source)	14	15 ?
IA12	Addressline 12 (internal source)	14	15 ?
IA13	Addressline 13 (internal source)	14	15 ?
IA13*	Addressline 13 (internal source)	15	15
INTL*	Select internal mode	15	15
IOE0*	Output enable, (internal) RAM 0	15	14
IOE1*	Output enable, (internal) RAM 1	15	14
IOE2*	Output enable, (internal) RAM 2	15	14
IOE3*	Output enable, (internal) RAM 3	15	14
IOE4*	Output enable, (internal) RAM 4	15	15
IOE5*	Output enable, (internal) RAM 5	15	15
IOE6*	Output enable, (internal) RAM 6	15	15
IOE7*	Output enable, (internal) RAM 7	15	15
ISDAT	(internal) Serial data up	14	15
IWE0*	Write enable, (internal) RAM 0	15	14
IWE1*	Write enable, (internal) RAM 1	15	14
IWE2*	Write enable, (internal) RAM 2	15	14
IWE3*	Write enable, (internal) RAM 3	15	14
IWE4*	Write enable, (internal) RAM 4	15	15
IWE5*	Write enable, (internal) RAM 5	15	15
IWE6*	Write enable, (internal) RAM 6	15	15
IWE7*	Write enable, (internal) RAM 7	15	15
LD0	Rom emulator data 0	14	15 BD
LD1	Rom emulator data 1	14	15 BD
LD2	Rom emulator data 2	14	15 BD
LD3	Rom emulator data 3	14	15 BD
LD4	Rom emulator data 4	14	15 BD
LD5	Rom emulator data 5	14	15 BD
LD6	Rom emulator data 6	14	15 BD
LD7	Rom emulator data 7	14	15 BD

LIST OF SIGNAL NAMES (diagram 15)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
MODE 0	mode 0 select	15	not used
MODE 1	mode 1 select	15	14,15
ROMOD*	Select read mode	15	14
SCTL0	Selected control line 0	15	not used
SCTL1	Selected control line 1	15	15
SELDAT	Serial data up (to mainframe)	15	14
SELECT*	Select line	14	15
STSLOO*	Load connection test data	15	14
XA 1	Addressline 1 (external source)	15	14 ?
XA10	Addressline 10 (external source)	15	14 ?
XA11	Addressline 11 (external source)	15	14 ?
XA12	Addressline 12 (external source)	15	14 ?
XA13	Addressline 13 (external source)	15	14 ?
XA 2	Addressline 2 (external source)	15	14 ?
XA 3	Addressline 3 (external source)	15	14 ?
XA 4	Addressline 4 (external source)	15	14 ?
XA 5	Addressline 5 (external source)	15	14 ?
XA 6	Addressline 6 (external source)	15	14 ?
XA 7	Addressline 7 (external source)	15	14 ?
XA 8	Addressline 8 (external source)	15	14 ?
XA 9	Addressline 9 (external source)	15	14 ?
XCOM0	Ground on port A (ext. source)	14	15
XCOM1	Ground on port B (ext. source)	14	15
XCOM2	Ground on port C (ext. source)	15	15
XCOM3	Ground on port D (ext. source)	15	15
XEN1	Select RAM for port B (ext.source)	14	15
XEN2	Select RAM for port C (ext.source)	15	not used
XEN2	Select RAM for port C (ext.source)	15	not used
XEN3	Select RAM for port D (ext.source)	15	15
XEN3	Select RAM for port D (ext.source)	15	15
XPWR0	Power on port A (ext. source)	14	15
XPWR1	Power on port B (ext. source)	14	15
XPWR2	Power on port C (ext. source)	15	15
XPWR3	Power on port D (ext. source)	15	15
XSDAT	Serial data up (from second pod)	14	15
XSTS0A	Conection test, port A	15	14
XSTS0B	Conection test, port A	15	14
XSTS1A	Conection test, port B	15	14
XSTS1B	Conection test, port B	15	14
XSTS2A	Conection test, port C	15	14
XSTS2B	Conection test, port C	15	14
XSTS3A	Conection test, port D	15	14
XSTS3B	Conection test, port D	15	14

3.5 STANDARD BUS POD (see figures 3.9 and 3.10).

The standard bus pod (std bus pod: PM 8863) can be used as an extender card or as a separate plug-in unit for a system running on an Std. bus.

The Std-bus pod behaves itself as a microprocessor pod which means that it makes all the necessary connections to the system under test automatically. Disassembly of the captured data, however, is not possible.

Data (D0...D7) and address lines (A0...A15) from the Std bus are buffered using high impedance buffers (4E, 4D, 4C, see figure 3.9).
The data lines are also latched (2E) to meat set-up and hold time requirements (clock signal DLTCH, derived from the external clock signal EXTCLK and signal INT*; 1A).

Data channels 24...31 (SIG24....SIG31) are used to take-in user defined signals. The user can make his own connections by changing the jumper settings. The default setting is the STDBUS setting (as shown in figures 3.9 and 3.10).
For more details about the different connections, refer to the PM 3632 operating manual.

Data channels 24...31 are also used to read the identity of the pod, by reading the contents of buffer 2C. The uP also reads if the pod is connected correctly (signal X1).
The selection of this buffer is done by means of the BFPODSEL (buffered pod select) signals which come from the mainframe (buffers U50, see figure 2.7).

The selection between internal (BFCLKOUT) or external (EXTCLK) is done in the pod by means of multiplexer 2A. The selection is done by means of signals BFPODSEL0 and BFPODSEL1.
The selected clock (SCLK) is then sent to the mainframe to clock the input demultiplexers.
The external clock (see figure 3.10) is derived from signals AREFRESH*, ARD*, AWR* and AINTAK* which are first compared to a fixed reference voltage and then wired-ored (5C and 5D).

To protect the pod against pod connection errors, FET Q1 (see figure 3.9) only connects ground of the system under test (X3) to ground of the mainframe, only when the power (X1) is at the correct pin of the pod (pin 1 of connecter P1).

LIST OF SIGNAL NAMES (diagram 16)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destignation (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
AS 0	Adress line 0, std-bus	17	16
AS 1	Adress line 1, std-bus	17	16
AS 2	Adress line 2, std-bus	17	16
AS 3	Adress line 3, std-bus	17	16
AS 4	Adress line 4, std-bus	17	16
AS 5	Adress line 5, std-bus	17	16
AS 6	Adress line 6, std-bus	17	16
AS 7	Adress line 7, std-bus	17	16
AS 8	Adress line 8, std-bus	17	16
AS 9	Adress line 9, std-bus	17	16
AS10	Adress line 10, std-bus	17	16
AS11	Adress line 11, std-bus	17	16
AS12	Adress line 12, std-bus	17	16
AS13	Adress line 13, std-bus	17	16
AS14	Adress line 14, std-bus	17	16
AS15	Adress line 15, std-bus	17	16
BFPODSEL0	Buffered pod select 0	3	16
BFPODSEL1	Buffered pod select 1	3	16
BFPODSEL2	Buffered pod select 2	3	16
BFPODWRT*	Buffered pod write	3	16
BUSAK*	Bus acknowledge, std-bus	17	16
CBUSRQ*	Clocked bus request	17	16
CD0	Captured data 0	16	16
CD1	Captured data 1	16	16
CD2	Captured data 2	16	16
CD3	Captured data 3	16	16
CD4	Captured data 4	16	16
CD5	Captured data 5	16	16
CD6	Captured data 6	16	16
CD7	Captured data 7	16	16
CINTRQ*	Clocked int. request	17	16
CIOR	Clocked IO read	17	16
CMMR	Clocked memory read	17	16
CMMR*	Clocked memory read	17	16
CLTCH	Clock data latch	17	16
DS0	Data line 0, std-bus	17	16
DS1	Data line 1, std-bus	17	16
DS2	Data line 2, std-bus	17	16
DS3	Data line 3, std-bus	17	16
DS4	Data line 4, std-bus	17	16
DS5	Data line 5, std-bus	17	16
DS6	Data line 6, std-bus	17	16
DS7	Data line 7, std-bus	17	16
EXTCLK	External clock	17	16
INT*	Select internal clock	16	17
INTAK*	Interrupt acknowledge	17	16
IO/M*EXP	IO/Memory	17	16
MCSYNC*	Master clock sync., std-bus	17	16
MODE 2	mode 2 select	16	16
PC0	Programcounter 0, std-bus	17	16
PC1	Programcounter 1, std-bus	17	16
QUALIN	Qualifier in signal	16	1,5
RD*	Read signal	17	16
READEN	Enable id buffer read	16	16
READEN*	Enable id buffer read	16	16

LIST OF SIGNAL NAMES (diagram 16, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
REFRESH*	Refresh cycle, std-bus	17	16
SCLK	Selected clock	16	1,5
SIG 0	Input channel 0	16	1,5
SIG 1	Input channel 1	16	1,5
SIG 2	Input channel 2	16	1,5
SIG 3	Input channel 3	16	1,5
SIG 5	Input channel 5	16	1,5
SIG 6	Input channel 6	16	1,5
SIG 7	Input channel 7	16	1,5
SIG 8	Input channel 8	16	1,5
SIG 9	Input channel 9	16	1,5
SIG10	Input channel 10	16	1,5
SIG11	Input channel 11	16	1,5
SIG12	Input channel 12	16	1,5
SIG13	Input channel 13	16	1,5
SIG14	Input channel 14	16	1,5
SIG15	Input channel 15	16	1,5
SIG16	Input channel 16	16	1,5
SIG17	Input channel 17	16	1,5
SIG18	Input channel 18	16	1,5
SIG19	Input channel 19	16	1,5
SIG20	Input channel 20	16	1,5
SIG21	Input channel 21	16	1,5
SIG22	Input channel 22	16	1,5
SIG23	Input channel 23	16	1,5
SIG24	Input channel 24	16	1,3,5 BD
SIG25	Input channel 25	16	1,3,5 BD
SIG26	Input channel 26	16	1,3,5 BD
SIG27	Input channel 27	16	1,3,5 BD
SIG28	Input channel 28	16	1,3,5 BD
SIG29	Input channel 29	16	1,3,5 BD
SIG30	Input channel 30	16	1,3,5 BD
SIG31	Input channel 31	16	1,3,5 BD
STATUS0*	Status line 0, std-bus	17	16
STATUS1*	Status line 1, std-bus	17	16
UADREN*	Address latch enable	16	16
WAITRQ*	Wait request, std-bus	17	16
WR*	Write signal	17	16
X1	External power, std-bus	17	16
X3	External ground, std-bus	17	16

LIST OF SIGNAL NAMES (diagram 17)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
AINTAK*	Interrupt ackowledge, std-bus	17	17
ARD*	Read, std-bus	17	17
AREFRESH*	Refresh clock, std bus	17	17
AS 0	Adress line 0, std-bus	17	16
AS 1	Adress line 1, std-bus	17	16
AS 2	Adress line 2, std-bus	17	16

LIST OF SIGNAL NAMES (diagram 17, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
AS 3	Adress line 3, std-bus	17	16
AS 4	Adress line 4, std-bus	17	16
AS 5	Adress line 5, std-bus	17	16
AS 6	Adress line 6, std-bus	17	16
AS 7	Adress line 7, std-bus	17	16
AS 8	Adress line 8, std-bus	17	16
AS 9	Adress line 9, std-bus	17	16
AS10	Adress line 10, std-bus	17	16
AS11	Adress line 11, std-bus	17	16
AS12	Adress line 12, std-bus	17	16
AS13	Adress line 13, std-bus	17	16
AS14	Adress line 14, std-bus	17	16
AS15	Adress line 15, std-bus	17	16
AWR*	Write, std-bus	17	17
BUSAK*	Bus acknowledge, std-bus	17	16
BUSRQ	Bus request, std-bus	17	not used
CBUSRQ*	Clocked bus request	17	16
CINTRQ*	Clocked int. request	17	16
CIOR	Clocked IO read	17	16
CIOR*	Clocked IO read	17	16
CLOCK*	Clock signal, std-bus	17	not used
CMMR	Clocked memory read	17	16
CMMR*	Clocked memory read	17	16
CNTRL*	Control line, std-bus	17	not used
DLTCH	Clock data latch	17	16
DS0	Data line 0, std-bus	17	16
DS1	Data line 1, std-bus	17	16
DS2	Data line 2, std-bus	17	16
DS3	Data line 3, std-bus	17	16
DS4	Data line 4, std-bus	17	16
DS5	Data line 5, std-bus	17	16
DS6	Data line 6, std-bus	17	16
DS7	Data line 7, std-bus	17	16
EXTCLK	External clock	17	16
INT*	Select internal clock	16	17
INTAK*	Interrupt acknowledge	17	16
INTRQ	Interrupt request, std-bus	17	not used
IO/M*EXP	IO/Memory	17	16
IOEXP	Input/output, std-bus	17	17
IORQ*	Input/output request, std-bus	17	17
MCSYNC*	Master clock sync., std-bus	17	16,17
MEMEX	Memory, std-bus	17	17
MEMRQ*	Memory request, std-bus	17	17
NMIRQ*	Request, std-bus	17	not used
PBRESET*	Power board reset, std-bus	17	not used
PC0	Programcounter 0, std-bus	17	16
PC1	Programcounter 1, std-bus	17	16
RD*	Read signal	17	16
REFRESH*	Refresh cycle	17	16
STATUS0*	Status line 0, std-bus	17	16
STATUS1*	Status line 1, std-bus	17	16
SYSRESET*	System reset, std-bus	17	not used
WAITRQ*	Wait request, std-bus	17	16
WR*	Write signal	17	16
X1	External power, std-bus	17	16,17
X3	External ground, std-bus	17	16

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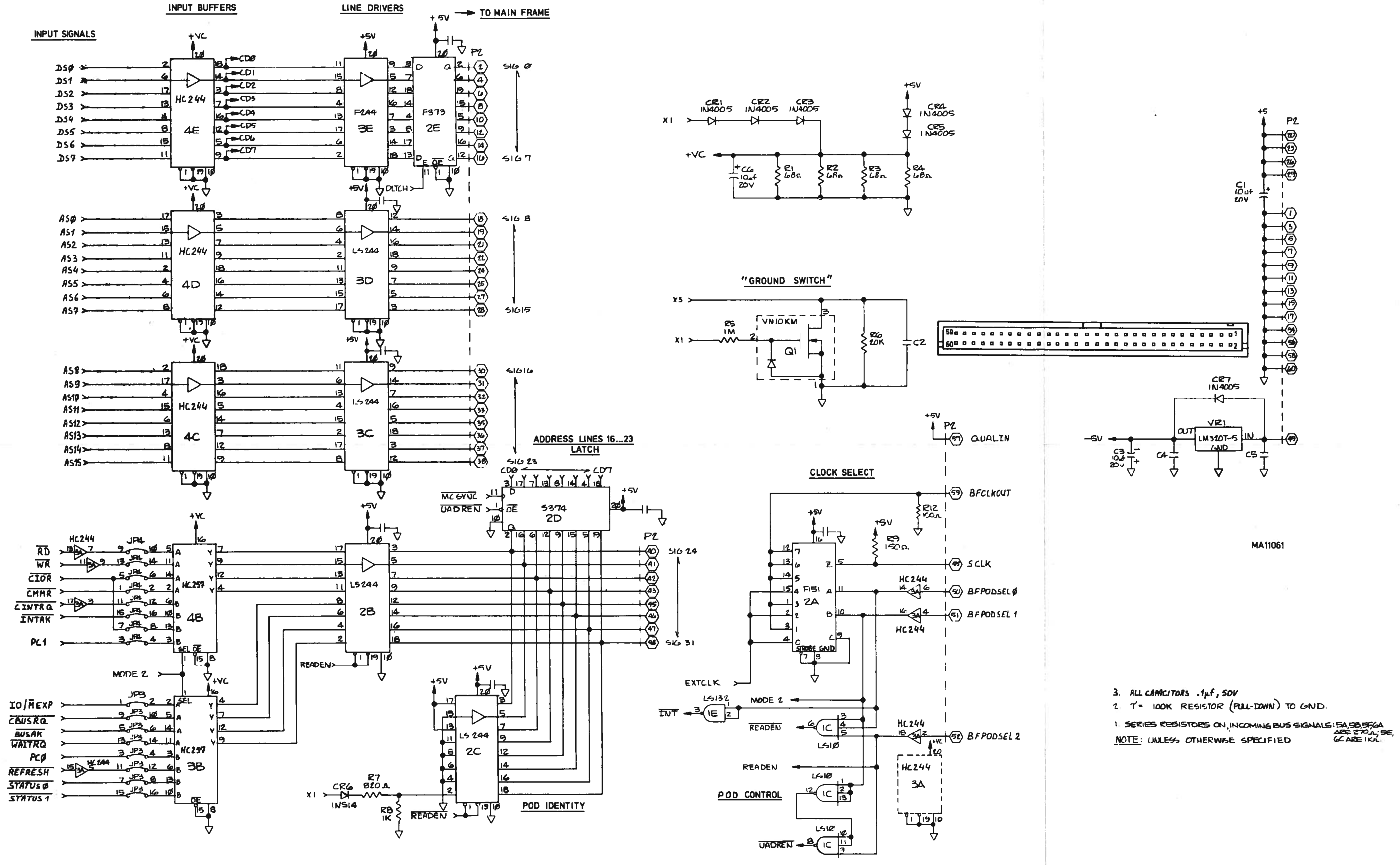

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3. ALL CAPACITORS .1µf, 50V
2. T = 100K RESISTOR (PULL-DOWN) TO GND.
1. SERIES RESISTORS ON INCOMING BUS SIGNALS: 5A, 5B, 5FGA ARE 270Ω; 5E, 6C ARE 1KΩ.

NOTE: UNLESS OTHERWISE SPECIFIED

Figure 3.9 : Std bus pod; input channels (16)

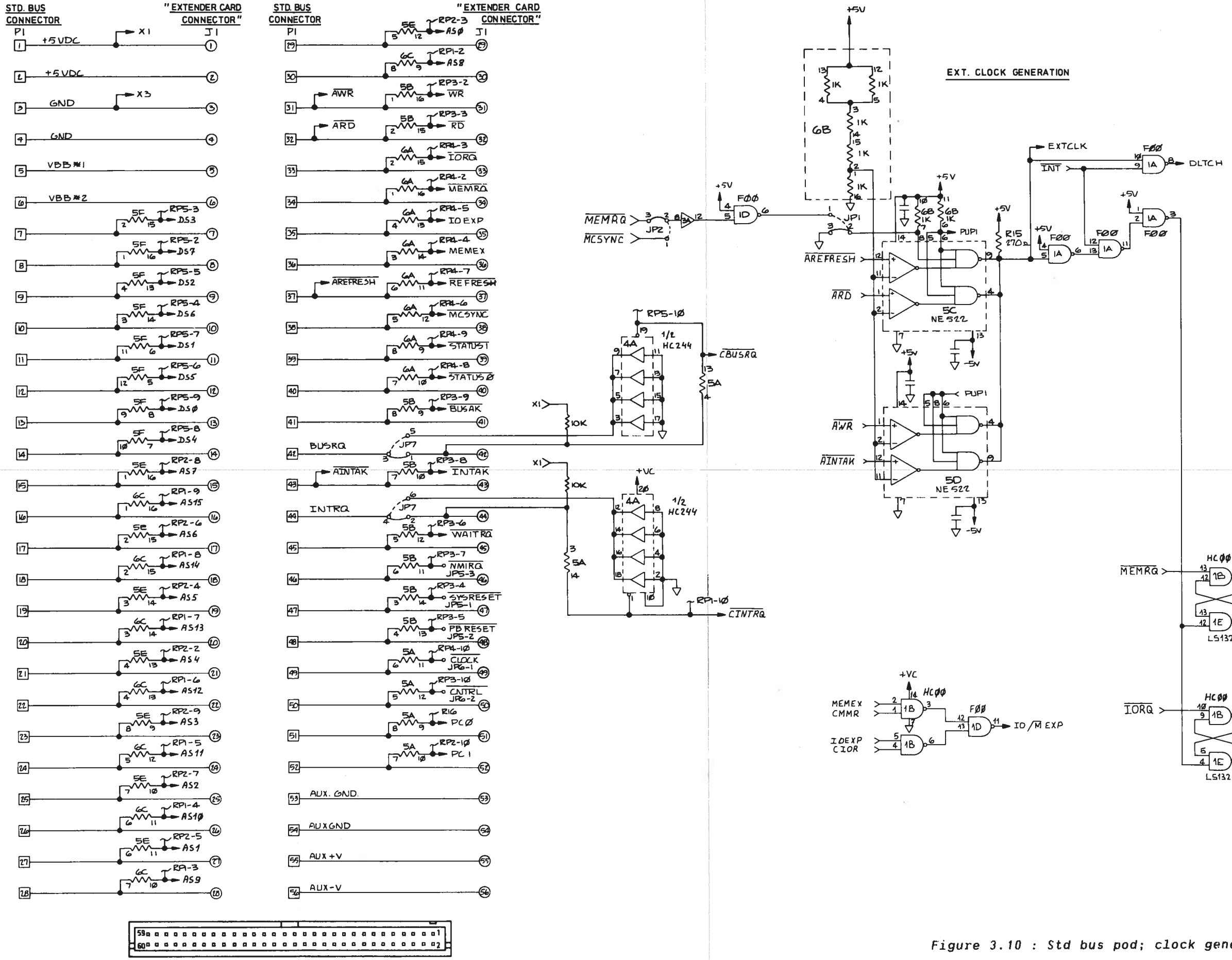


Figure 3.10 : Std bus pod; clock generation and connectors (17)

3.6 DISASSEMBLER PODS.

3.6.1 GENERAL

The disassembler pods, in common, make it possible to make an easy connection to the system under test. This is done via a one clip connection directly on the microprocessor of the system under test.
All the necessary connections are made in the pod itself.

Data lines, address lines, status lines and clock lines are first buffered and sometimes latched before these signals are passed to the input demultiplexers in the mainframe.
The clock signals which are necessary to capture data, addresses and status information are wired-ored and then as one clock signal passed to the mainframe to clock the input demultiplexers.
The selection between internal or external clock is done in the pod under control of the microprocessor (in the mainframe).

Disassembly of the microprocessor instructions is possible only when a Disa Rom board is installed in the mainframe (furnished with the correct disa PROM).

NOTE: for all microprocessor pods, the connector numbering of P2 -the connector via which all the signals are sent to the mainframe- is different than for the other pods!

If: Pm = PM 3632 connector pin
Pp = pod connector pin

Then: Pm = 61-Pp
Pp = 61-Pm

3.6.2 8085, 8048 (FAM.), 8051 (FAM.) MICROPROCESSOR POD (see figure 3.11)

This pod supports the INTEL 8048 family (8035, 8039 and 8040), the 8051 family (8031 and 8032) and the 8085.

Data signals (DATA0...DATA7) from the system under test are first buffered by high impedance multiplexer U10 and U17. In case of connection to one of the 8051 family, the connection to the microprocessor is different: the multiplexers are set to a different direction via signal S51* (select 8051 family).

The lower 8 address lines (ADDR0...ADDR7) are latched in U11, and then passed to the input demultiplexers in the mainframe (SIG0...SIG7 via P2).
The upper 8 address lines (ADDR8...ADDRF) are first buffered by a high impedance buffer (U20), then after buffering in U18 passed to the input demultiplexers in the mainframe (SIG15...SIG23 via P2).

Status information from the microprocessor is passed to the mainframe via the upper half of buffer U14 (SIG24...SIG31).
Which status information is transferred (8085 or 8048/8051), is selected by multiplexer U16 via signal S85*.
The status signals for the 8085 are connected directly to U16 (X29,X33,X34,X38).
The status signals for 8048/8051 are first buffered via U5, U4 (WT5148*, PSEN5148*, RD5148*). In 8085 mode, the ALE* signal clears buffer U4.

U5 makes the selection between 8048/8051 status information (different connections to microprocessor) and the ALE* signal of the 8085 which latches the address signals.

Four spare lines are available for user-defined connections to the system under test. These signals are buffered via U15 before they are transferred to the mainframe.

The selection between internal clock (BFCLKOUT) or external clock and which external clock source, is done under control of the microprocessor by means of signals BFPODSEL0...BFPODSEL2 (buffered pod select) which come from buffer U50 in the mainframe (see figure 2.7).
As an external clock, the microprocessor can select between the 8085 (RD*, WR* and INTACK* via U9-pin 6), the 8051 family (RD*, WR* and PSEN* via U9-pin8) and the 8048 family (RD*, WR*, PSEN*).
All clock signals are combined via NAND gates, which means that when one of them goes low, a clock pulse will be generated for the mainframe.

The microprocessor in the mainframe can read the identity of the pod by reading the contents of buffer U19. This is done via data lines 24...31.
When doing this, buffer U14 is disabled.

To protect the pod against pod connection errors, ground of the system under test is only connected to ground of the mainframe (via FET Q1) when the supply voltage (X40) is at the correct position of the microprocessor clip.
The microprocessor in the mainframe reads this information via buffer U19 and will display POD CONNECTION ERROR if the pod is not connected properly.

WARNING: When using the side probe, do not connect the ground wires! This will cause a short circuit between the drain and source of FET Q1.

MODIFICATIONS:

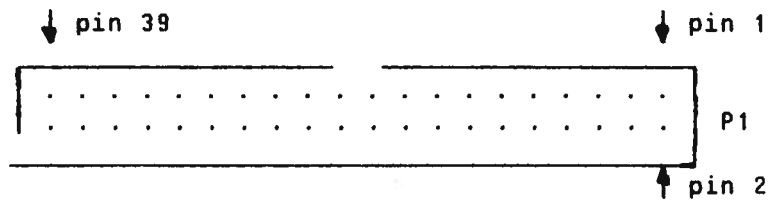
1. In some applications, the target system will not work correctly anymore after connecting a PM 8865 microprocessor pod to it.
   This can be caused by one of the following three problems:
   a. The "high" voltage of the target system is limited to +3 Vdc by the 74HC..... input circuits inside the pod.
   b. Capacitive coupling of microprocessor pins via the flat cable that leads to the pod.
   c. Capacitive loading of the target system by the flat cable that leads to the pod (especially the crystal clock inputs of the uP).

   Therefore the following modifications have to be done in the PM 8865 pod.
   These modifications only have to be done when you have a "revision A" board in the pod (this revision has no revision indicaton at the outside of the pod).
   After these modifications, the pod has board revision B (indicated by a character B engraved behind the serial number, at the outside of the pod).
   Proceed as follows:
   A. The input circuits of the pod have to be changed into 74HCT..... circuits (U17, U10, U5, U20, U9, U6 and U15) in order to raise the "high" voltage of the target.
   B. Diodes CR3 and CR4 are replaced by jumpers, in order to increase the power supply voltage for the 74HCT..... circuits to +5 Vdc.
   C. Resistors R9, R10, R11 and R12 must be removed.
   D. The flat cable + microprocessor clip have to be replaced by a better one. This better cable, alternates ground and signal lines, in order to eleminate cross-talk problems.
      In the new cable, pins 1 ... 7 of the microprocessor are cut at the clip in order to reduce capacitive loading.
   E. Engrave the character "B" behind the serial number, at the back of the pod.

   These modifications, solve problems a and b.

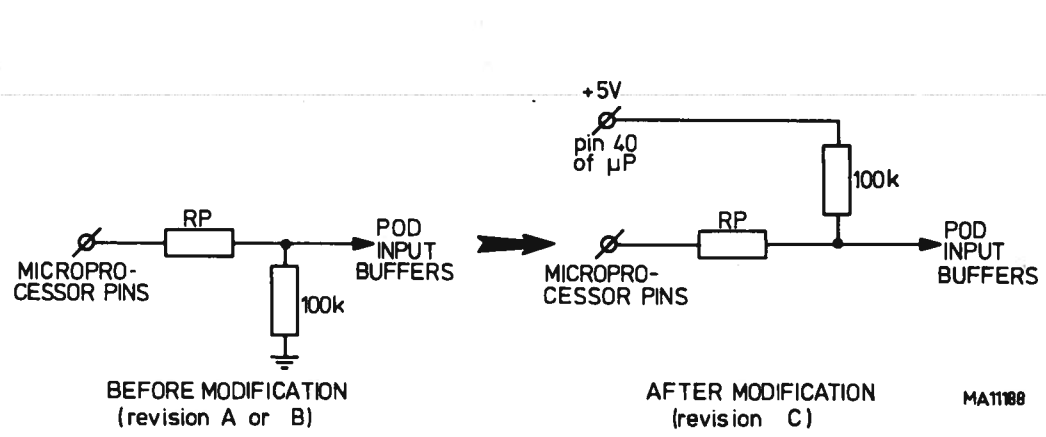
   Some pins of the microprocessor clip are required for one microprocessor type, while being susceptible to capacitive loading problems when using it on another microprocessor type. An example of this is uP pins 18 and 19, which are the clock pins of an 8031 (problem c).
   To solve this problem, you have to "tape" (or insulate otherwise) these pins from the clip, when using it on an 8031 microprocessor.

2. When you want to connect the PM 8865 microprocessor pod to CMOS microprocessors, you have to make the following modifications:
   a. If your pod is not a revision B, first upgrade the pod to the revision B status. For this, see the instructions A ... D above. Do not engrave the character B in the pod box!!!!
   b. Cut the large trace to RP1, pin 1 (component side).
   c. Cut the large trace between U17-pin 8 and R13 (component side only, and **not** under R13!!!).
   d. Cut the large trace between RP8-pin 1 and R21 (solder side).
   e. Cut the large trace that leads to RP3-pin 1 (solder side).
   f. Cut the large trace that leads to RP6-pin 1 (solder side).
   h. Add a wire between the just freed end of R21 and U17-pin 8.
   i. Add a wire between connector P1-pin 39 and RP8-pin 1.
      (pin 1 of connector P1 is marked with a little arrow, see also next page).



j. Add a wire between RP8-pin 1 and RP3-pin 1
k. Add a wire between RP3-pin 1 and RP1-pin 1
l. Add a wire between RP6-pin 1 and near end of R13.
m. If your pod was revision B, engrave a stroke across the character 8 and engrave a character D immediately after the character 8 (at the back of the black pod box).
n. If your pod was revision A, then engrave a character D immediately after the serial number at the back of the black pod box.

After these modifications, the input pull-down resistors of 100 Kohm are changed to pull-up resistors. The pull-up resistors are connected to the +5 V supply of the target system itself (via P1, pin 39) and not to the +5 V supply of the pod (see below).



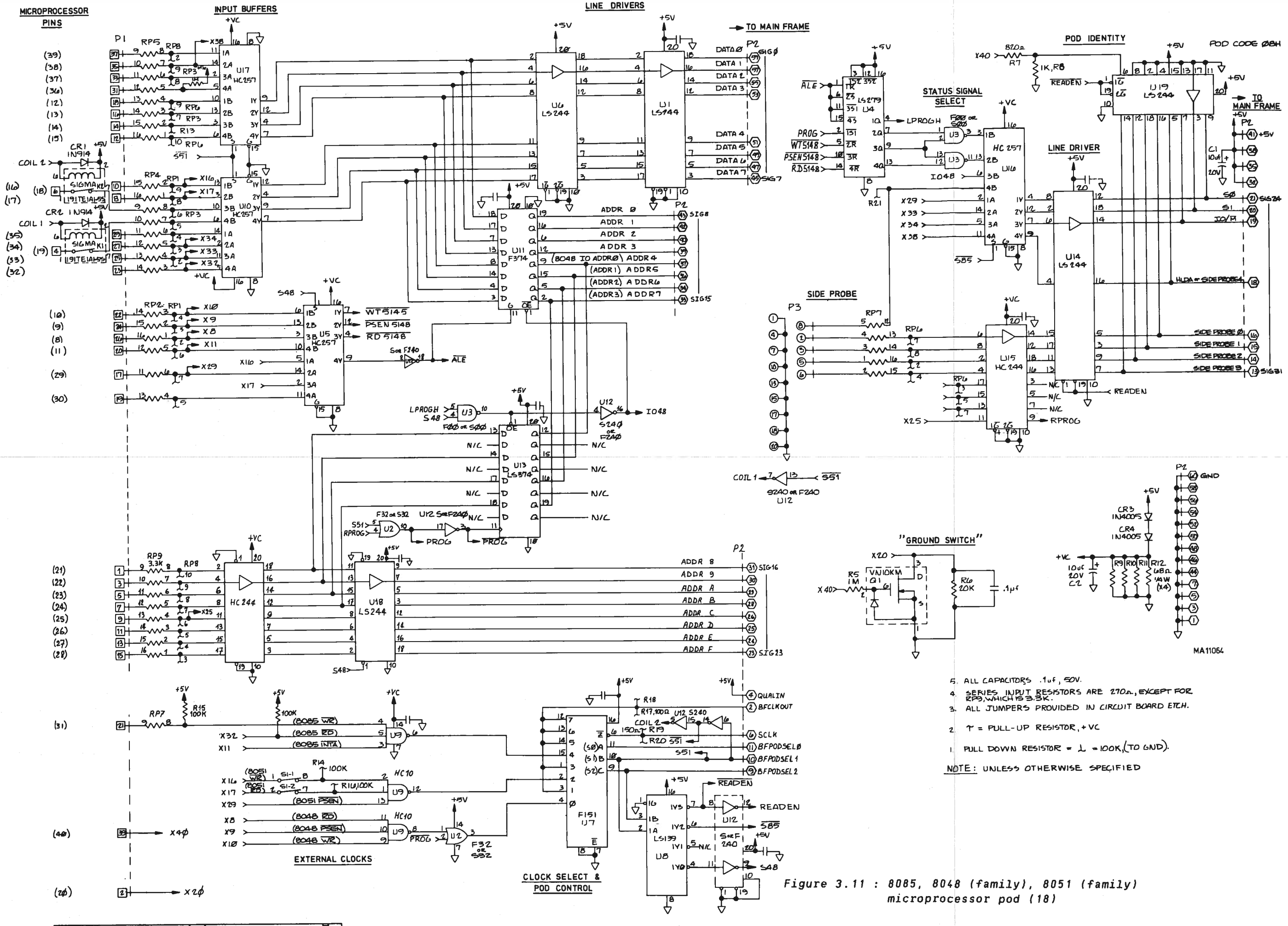
LIST OF SIGNAL NAMES (diagram 18)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destignation (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
ALE*	Address latch enable 8085	18	18
BFPODSEL0	Buffered pod select 0	3	18
BFPODSEL1	Buffered pod select 1	3	18
BFPODSEL2	Buffered pod select 2	3	18
BFPODWRT*	Buffered pod write	3	18
COIL0	Energize coil 0	18	18
COIL1	Energize coil 1	18	18
IO48	Status signal from IO expander	18	18
LPROGH	Buff. output strobe for IO exp.	18	18
PROG	Output strobe for IO expander	18	18
PROG*	Output strobe for IO expander	18	18
PSEN5148*	Program store enable 8051,8048	18	18
QUALIN	Qualifier in signal	18	1,5
RD5148*	Read signal 8051,8048	18	18
READEN	Oisable data buffer for id read	18	18
READEN*	Enable buffer for id read	18	18
RPROG	Output strobe for IO exp. (int.)	18	18
S48	Select 8048 mode	18	18
S51	Select 8051 mode	18	18
S51*	Select 8051 mode	18	18
S85*	Select 8085 mode	18	18
SCLK	Selected clock	18	1,5
SIG 0	Input channel 0	18	1,5
SIG 1	Input channel 1	18	1,5
SIG 2	Input channel 2	18	1,5
SIG 3	Input channel 3	18	1,5
SIG 5	Input channel 5	18	1,5
SIG 6	Input channel 6	18	1,5
SIG 7	Input channel 7	18	1,5
SIG 8	Input channel 8	18	1,5
SIG 9	Input channel 9	18	1,5
SIG10	Input channel 10	18	1,5
SIG11	Input channel 11	18	1,5
SIG12	Input channel 12	18	1,5
SIG13	Input channel 13	18	1,5
SIG14	Input channel 14	18	1,5
SIG15	Input channel 15	18	1,5
SIG16	Input channel 16	18	1,5
SIG17	Input channel 17	18	1,5
SIG18	Input channel 18	18	1,5
SIG19	Input channel 19	18	1,5
SIG20	Input channel 20	18	1,5
SIG21	Input channel 21	18	1,5
SIG22	Input channel 22	18	1,5
SIG23	Input channel 23	18	1,3,5
SIG24	Input channel 24	18	1,3,5 BD
SIG25	Input channel 25	18	1,3,5 BD
SIG26	Input channel 26	18	1,3,5 BD
SIG27	Input channel 27	18	1,3,5 BD
SIG28	Input channel 28	18	1,3,5 BD
SIG29	Input channel 29	18	1,3,5 BD
SIG30	Input channel 30	18	1,3,5 BD
SIG31	Input channel 31	18	1,3,5 BD

LIST OF SIGNAL NAMES (diagram 18, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
WT5148*	Write signal 8051,8048	18	18
X 8	Signal from uP pin 8	18	18
X 9	Signal from uP pin 9	18	18
X10	Signal from uP pin 10	18	18
X11	Signal from uP pin 11	18	18
X16	Signal from uP pin 16	18	18
X17	Signal from uP pin 17	18	18
X20	Signal from uP pin 20	18	18
X25	Signal from uP pin 25	18	18
X29	Signal from uP pin 29	18	18
X32	Signal from uP pin 32	18	18
X33	Signal from uP pin 25	18	18
X34	Signal from uP pin 25	18	18
X38	Signal from uP pin 25	18	18
X40	Signal from uP pin 40	18	18



5. ALL CAPACITORS .1uf, 50V.
4. SERIES INPUT RESISTORS ARE 270Ω., EXCEPT FOR RP9, WHICH IS 3.3K.
3. ALL JUMPERS PROVIDED IN CIRCUIT BOARD ETCH.
2. T = PULL-UP RESISTOR, +VC
1. PULL DOWN RESISTOR = ⊥ = 100K, (TO GND).

NOTE: UNLESS OTHERWISE SPECIFIED

Figure 3.11 : 8085, 8048 (family), 8051 (family) microprocessor pod (18)

3.6.3 6800, 6809 AND 6502 MICROPROCESSOR PODS (see figure 3.12).

These pods support the following microprocessor:
PM 8866 : Motorola 6800, 6802, 6808
PM 8867 : Motorola 6809, 6809E
PM 8868 : Rockwell 6502, 6512, 65C02, 65C102, 65C112.
In this paragraph these pods will be referred to as the 6800, 6809 and 6802 pods respectively.

The reason why they are described here in the same paragraph is, that they are all implemented on the same p.c. board. For the different pods, the p.c. boards are configured slightly differently and switch settings are different. The different switch settings are shown in the tables of figure 3.13.

Data signals (DATA0...DATA7) and the address lines (ADR0...ADR15) are first high impedance-buffered (U9, U13 and U16) and then passed to the input demultiplexers in the mainframe (SIG0...SIG23 via P2).
In case of a 6809 pod, RN4, RN5 and RN6 are in a different position; the input buffer now take in the correct signals from the 6809 microprocessor.

Data inputs 24...27 (SIG24...SIG27) are used to take-in status information from the microprocessor under test (high impedance buffered via U1).
In case of the 6502 pod, switches S1-3 and S1-4 are closed. Now the clock signals (Ø1 and Ø2) of the 6502 microprocessor latch the READY signal via U4. READY is one of the status signals which is necessary for disassembly.
Data inputs 28...31 (SIG28...SIG31) can be used to take-in 4 user defined signals (via P3) or two more status signals and 2 user defined signals when the 6809 pod is used in the 6809E mode (see table in figure 3.9).

The selection for these 4 input channels is done via multiplexer U2 which can be set in two different ways by the microprocessor in the mainframe via BFPODSEL1 (buffered pod select).
Via this multiplexer input buffer U1 is by-passed.
Relais K1 disconnects U2 from the crystal of the 6809 microprocessor when the 6809 pod is used in 6809 mode (selected by BFPODSEL 1, via U12).

Via input channels 24...31, the microprocessor in the mainframe can also read the pod identity by reading the contents of buffer U6.
This code is different for each pod (code 0, code 1). In this case, register U3 is disabled.

The selection between internal clock (BFCLKOUT) or external clock, and which external clock source, is done under control of the microprocessor by means of signals BFPODSEL0 and BFPODSEL2 (U8) which come from buffer U50 in the mainframe (see figure 2.7)
All clock signals are compared to a fixed reference voltage by means of U11 and U7.
As an external clock, the microprocessor of the mainframe can select between clocks from:
6502 : via U11 and U7
6800 : via U11 (pin 4 only) and U7 (pin 9 only)
6809 : via U11 (pin 4 only);
For each pod, jumper settings and switch settings between connector P1 and the comparators are different.
Relais K2 disconnect U11 from the crystal of the 6809 microprocessor when the 6809 pod is used in 6809 mode and connects the crystal to U11 when the pod is used in 6809E mode (selected by BFPODSEL 1, via U12).

To protect the pod against pod connection errors, ground of the system under test (pin 40) is only then connected to ground of the mainframe (via FETQ1) when the supply voltage (pin 26 or pin 28) is at the correct position of the microprocessor clip.
This is detected via voltage follower U5 (pin 12) and comparator U5 (pin 10). The microprocessor in the mainframe reads this information via buffer U6 and will display POD CONNECTION ERROR if the pod is not connected properly.

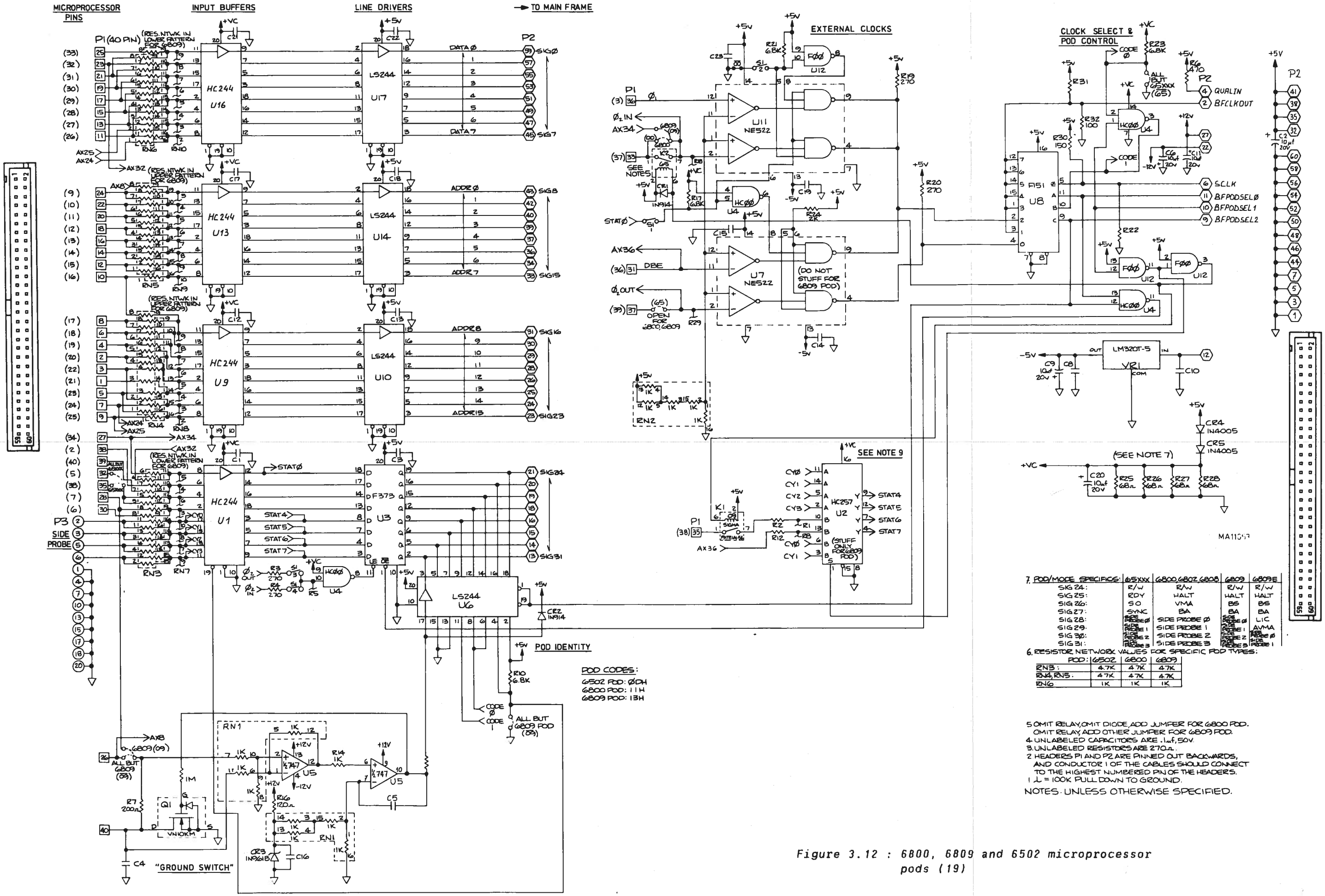
LIST OF SIGNAL NAMES (diagram 19)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
AX 8	Pin 8 of uP clip	19	19
AX24	Pin 24 of uP clip	19	19
AX25	Pin 25 of uP clip	19	19
AX32	Pin 32 of uP clip	19	19
AX34	Pin 34 of uP clip	19	19
AX36	Pin 36 of uP clip	19	19
BFPODSEL0	Buffered pod select 0	3	19
BFPODSEL1	Buffered pod select 1	3	19
BFPODSEL2	Buffered pod select 2	3	19
BFPODWRT*	Buffered pod write	3	19
CODE0	Pod identification code 0	19	19
CODE1	Pod identification code 1	19	19
CY0	Captured spare data 0	19	19
CY1	Captured spare data 1	19	19
CY2	Captured spare data 2	19	19
CY3	Captured spare data 3	19	19
Ø2IN	Ingoing clock signal	19	19
Ø2OUT	Outgoing clock signal	19	19
QUALIN	Qualifier in signal	19	1,5
SCLK	Selected clock	19	1,5
SIG 0	Input channel 0	19	1,5
SIG 1	Input channel 1	19	1,5
SIG 2	Input channel 2	19	1,5
SIG 3	Input channel 3	19	1,5
SIG 5	Input channel 5	19	1,5
SIG 6	Input channel 6	19	1,5
SIG 7	Input channel 7	19	1,5
SIG 8	Input channel 8	19	1,5
SIG 9	Input channel 9	19	1,5
SIG10	Input channel 10	19	1,5
SIG11	Input channel 11	19	1,5
SIG12	Input channel 12	19	1,5
SIG13	Input channel 13	19	1,5
SIG14	Input channel 14	19	1,5
SIG15	Input channel 15	19	1,5
SIG16	Input channel 16	19	1,5
SIG17	Input channel 17	19	1,5
SIG18	Input channel 19	19	1,5
SIG19	Input channel 19	19	1,5
SIG20	Input channel 20	19	1,5
SIG21	Input channel 21	19	1,5

LIST OF SIGNAL NAMES (diagram 19, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
SIG22	Input channel 22	19	1,5
SIG23	Input channel 23	19	1,5
SIG24	Input channel 24	19	1,3,5 BD
SIG25	Input channel 25	19	1,3,5 BD
SIG26	Input channel 26	19	1,3,5 BD
SIG27	Input channel 27	19	1,3,5 BD
SIG28	Input channel 28	19	1,3,5 BD
SIG29	Input channel 29	19	1,3,5 BD
SIG30	Input channel 30	19	1,3,5 BD
SIG31	Input channel 31	19	1,3,5 BD
STAT0	Status line 0	19	19
STAT4	Status line 4	19	19
STAT5	Status line 5	19	19
STAT6	Status line 6	19	19
STAT7	Status line 7	19	19



7. POD/MODE SPECIFICS:

	65XXX	6800, 6802, 6808	6809	6809E
SIG 24:	R/W	R/W	R/W	R/W
SIG 25:	RDY	HALT	HALT	HALT
SIG 26:	SO	VMA	BS	BS
SIG 27:	SYNC	BA	BA	BA
SIG 28:	[illegible]	SIDE PROBE Ø	[illegible]	LIC
SIG 29:	[illegible]	SIDE PROBE 1	[illegible]	AVMA
SIG 30:	[illegible]	SIDE PROBE 2	[illegible]	[illegible]
SIG 31:	[illegible]	SIDE PROBE 3	[illegible]	[illegible]

6. RESISTOR NETWORK VALUES FOR SPECIFIC POD TYPES:

POD:	6502	6800	6809
RN3:	4.7K	4.7K	4.7K
RN4, RN5.	4.7K	4.7K	4.7K
RN6	1K	1K	1K

5. OMIT RELAY, OMIT DIODE, ADD JUMPER FOR 6800 POD.
OMIT RELAY, ADD OTHER JUMPER FOR 6809 POD.
4. UNLABELED CAPACITORS ARE .1uf, 50V.
3. UNLABELED RESISTORS ARE 270Ω.
2. HEADERS P1 AND P2 ARE PINNED OUT BACKWARDS, AND CONDUCTOR 1 OF THE CABLES SHOULD CONNECT TO THE HIGHEST NUMBERED PIN OF THE HEADERS.
1. ⊥ = 100K PULL DOWN TO GROUND.

NOTES: UNLESS OTHERWISE SPECIFIED.

Figure 3.12 : 6800, 6809 and 6502 microprocessor pods (19)

POD/MODE: / SWITCH:	PM 8868			PM 8866		PM 8867
	6502	6512	65C02,65C102,65C112	6800	6802, 6808	6809
S1-1 (6512, 6800 WRITE CLOCK SOURCE)	OPEN	OPEN: S1-2 SELECTS CLOCK FOR WRITES. CLOSED: FALL OF DBE CLOCKS WRITES.	OPEN	OPEN: FALL OF ϕ_2 CLOCKS WRITES. CLOSED: FALL OF DBE CLOCKS WRITES.	OPEN	N/A
S1-2 (6512 READ CLOCK SOURCE)	OPEN	OPEN: FALL OF ϕ_2 CLOCKS READS. CLOSED: RISE OF ϕ_1 CLOCKS READS.	OPEN	N/A	N/A	N/A
S1-3 (6502 RDY SAMPLE TIME).	OPEN: RDY SAMPLED AT CLOCK TIME (FALL OF ϕ_2) CLOSED: RDY SAMPLED AT RISE OF ϕ_2	OPEN	OPEN	N/A	N/A	N/A
S1-4 (6512 RDY SAMPLE TIME).	OPEN	OPEN: RDY SAMPLED AT CLOCK TIME CLOSED: RDY SAMPLED AT RISE OF ϕ_2	OPEN	N/A	N/A	N/A

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RECOMMENDED DEFAULT SETTINGS:

MODE: / SW:	6502	6512	65C02 65C102 65C112	6800	6802 6808
S1-1	OPEN	CLOSED	OPEN	CLOSED	OPEN
S1-2	OPEN	CLOSED	OPEN	OPEN	OPEN
S1-3	CLOSED	OPEN	OPEN	OPEN	OPEN
S1-4	OPEN	CLOSED	OPEN	OPEN	OPEN

Figure 3.13 : 6800, 6809 and 6502 microprocessor pods; switch settings

3.6.4 Z80 MICROPROCESSOR POD (see figure 3.14).

This pod supports the ZILOG Z80 and Z80/A/B/C microprocessor.

Data signals (DATA0...DATA7) and address lines (ADR0...ADR15) are first high impedance-buffered (U3, U5, U9) and then transferred to the input demultiplexers in the mainframe (SIG0...SIG23).
The data signals are also latched (clock pulse DLTCH; data latch) to meet the setup & hold time requirements.

Data inputs 24...27 (SIG24...SIG27) are used to take-in 4 status signals of the Z80. These are necessary for correct disassembly of the microprocessor instructions.
Status signal IOREQ* is latched by means of U10, U17. This latch is cleared immediately after the next external clock pulse (CLTCH; clear latch).
Data inputs 28...31 can be used to take-in user defined signals (via P3).

The microprocessor in the mainframe can read the identity of the pod by reading the contents of buffer U12. This is done via data lines 24...31.
When doing this, buffer U19 is disabled.

The selection between internal clock (BFCLKOUT) and external clock (EXTCLK) is done via U16 by means of signals BFPODSEL0 (buffered pod select), which comes from buffer U50 in the mainframe (see figure 2.7).
The selected clock (SCLK) goes up to the mainframe to clock the input demultiplexers.
Signals BFPODSEL0...BFPODSEL2 are also used to generate the control signals for reading buffer U12.
Signal MODE2 is used to disable the refresh clock (DRFSH;U10) in normal mode in order not to show the refresh cycles on the display.

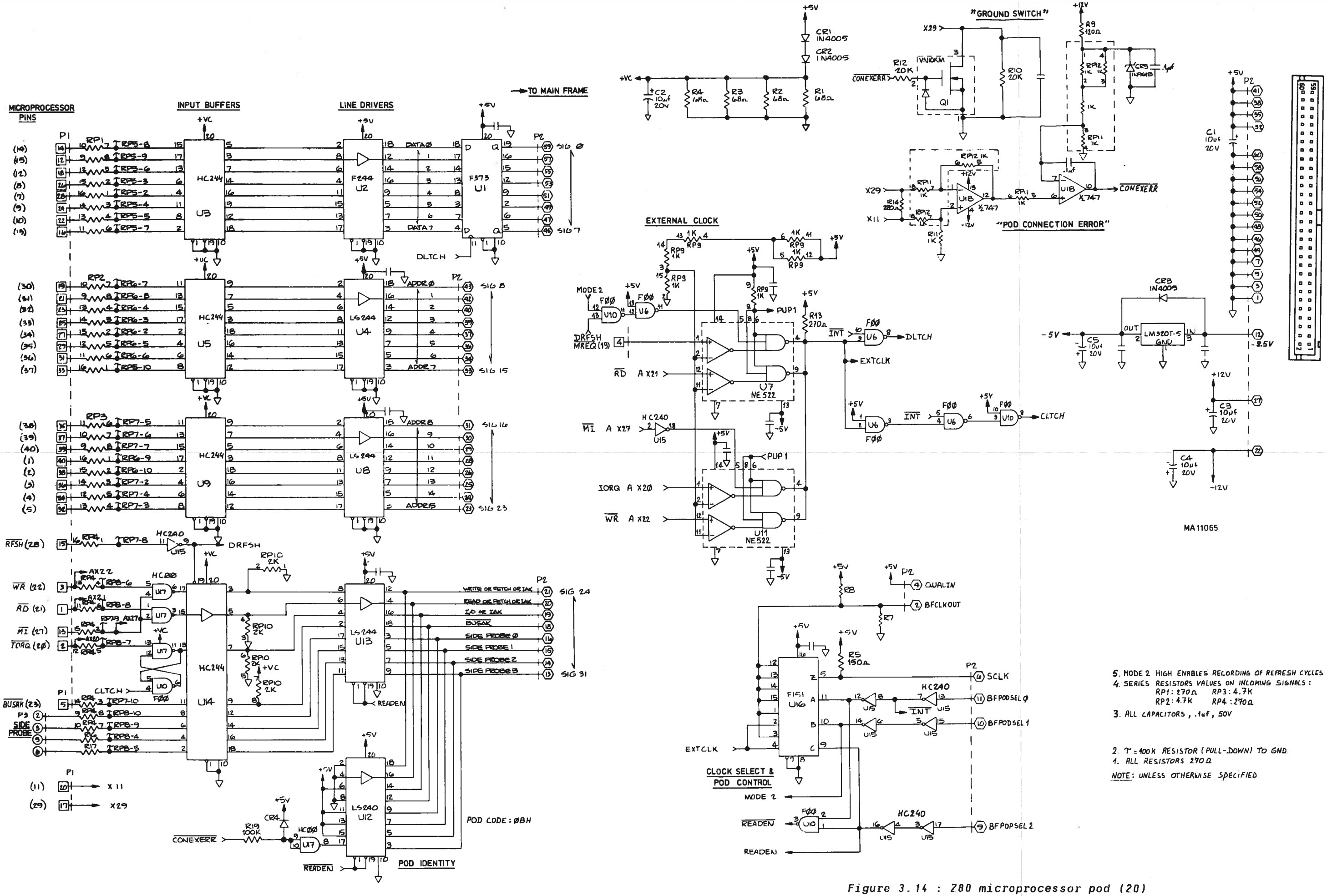
The external clock signals are first compared to a fixed threshold voltage (U7, U11) and then wired-ored to generate the external clock (EXTCLK).
In internal mode (signal INT*; comes from BFPODSEL 1) the generation of clocks for the data latch and IOREQ* latch are stopped.
Signal MODE 2 stops the generation of the refresh clock signal (DRFSH) when the pod is in the normal mode and enables the clock in Z80REF mode.

To protect the pod against pod connection errors, ground of the system under test (X29) is only then connected to ground of the mainframe (via FET Q1) when the supply voltage (X11 of the microprocessor) is at the correct position at the microprocessor clip.
This is detected via U18-pin 12 and comparator U18-pin 10 (CONEXERR*).
The microprocessor in the mainframe reads this information via buffer U12 and will display POD CONNECTION ERROR if the pod is not connected properly.

LIST OF SIGNAL NAMES (diagram 20)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name. A ? indicates that the source cannot be defined (for example one signal-name can come from different pods, but only one can be connected). A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
AX11	Pin 11 of uP clip	20	20
AX20	Pin 20 of uP clip	20	20
AX21	Pin 21 of uP clip	20	20
AX22	Pin 22 of uP clip	20	20
AX29	Pin 29 of uP clip	20	20
BFPODSEL0	Buffered pod select 0	3	20
BFPODSEL1	Buffered pod select 1	3	20
BFPODSEL2	Buffered pod select 2	3	20
BFPODWRT*	Buffered pod write	3	20
CLTCH	Clear latch	20	20
CONEXERR*	Connection error	20	20
CLTCH	Clock for data latch	20	20
DRFSH	Refresh cycle	20	20
EXTCLK	External clock	20	20
INT*	Set to internal clock mode	20	20
IORQ*/AX20	Input/output request	20	20
M1*/AX27	Machine cycle 1	20	20
MODE 2	Set to Z80AEF mode	20	20
MREQ	Memory request	20	20
QUALIN	Qualifier in signal	20	1,5
RD*/AX21	Read signal	20	20
READEN	Disable data buffer for id read	20	20
READEN*	Enable buffer for id read	20	20
SCLK	Selected clock	20	1,5
SIG 0	Input channel 0	20	1,5
SIG 1	Input channel 1	20	1,5
SIG 2	Input channel 2	20	1,5
SIG 3	Input channel 3	20	1,5
SIG 5	Input channel 5	20	1,5
SIG 6	Input channel 6	20	1,5
SIG 7	Input channel 7	20	1,5
SIG 8	Input channel 8	20	1,5
SIG 9	Input channel 9	20	1,5
SIG10	Input channel 10	20	1,5
SIG11	Input channel 11	20	1,5
SIG12	Input channel 12	20	1,5
SIG13	Input channel 13	20	1,5
SIG14	Input channel 14	20	1,5
SIG15	Input channel 15	20	1,5
SIG16	Input channel 16	20	1,5
SIG17	Input channel 17	20	1,5
SIG18	Input channel 20	20	1,5
SIG19	Input channel 20	20	1,5
SIG20	Input channel 20	20	1,5
SIG21	Input channel 21	20	1,5
SIG22	Input channel 22	20	1,5
SIG23	Input channel 23	20	1,5
SIG24	Input channel 24	20	1,3,5 BD
SIG25	Input channel 25	20	1,3,5 BD
SIG26	Input channel 26	20	1,3,5 BD
SIG27	Input channel 27	20	1,3,5 BD
SIG28	Input channel 28	20	1,3,5 BD
SIG29	Input channel 29	20	1,3,5 BD
SIG30	Input channel 30	20	1,3,5 BD
SIG31	Input channel 31	20	1,3,5 BD
WR*/AX22	Write signal	20	20



5. MODE 2 HIGH ENABLES RECORDING OF REFRESH CYCLES
4. SERIES RESISTORS VALUES ON INCOMING SIGNALS :
   RP1 : 270Ω RP3 : 4.7K
   RP2 : 4.7K RP4 : 270Ω
3. ALL CAPACITORS , .1uf , 50V

2. T = 100K RESISTOR (PULL-DOWN) TO GND
1. ALL RESISTORS 270Ω

NOTE : UNLESS OTHERWISE SPECIFIED

Figure 3.14 : Z80 microprocessor pod (20)

3.6.5. NSC800 MICROPROCESSOR POD (see figure 3.15)

This pod supports the NATIONAL SEMICONDUCTOR NSC800 microprocessor.

The multiplexed address and data bus is buffered in input bufferers U1 and U2. The data signals are again buffered by U15, and then latched into U16 (signal DLTCH, comes from clock generation) , before they are passed to the mainframe (SIG0 ... SIG7).
The address signals are clocked into output latch U3 on the ALE pulse, that comes from the microprocessor via U4. The outputs of U3 connect these address lines to the mainframe (SIG8 ... SIG15).
Address lines A8 ... A15 are also buffered first, and then latched before they are sent to the mainframe (SIG16 ... SIG23).

Status information from the microprocessor is passed to the mainframe via the upper half of buffer U7 and U8 (SIG24...SIG27).

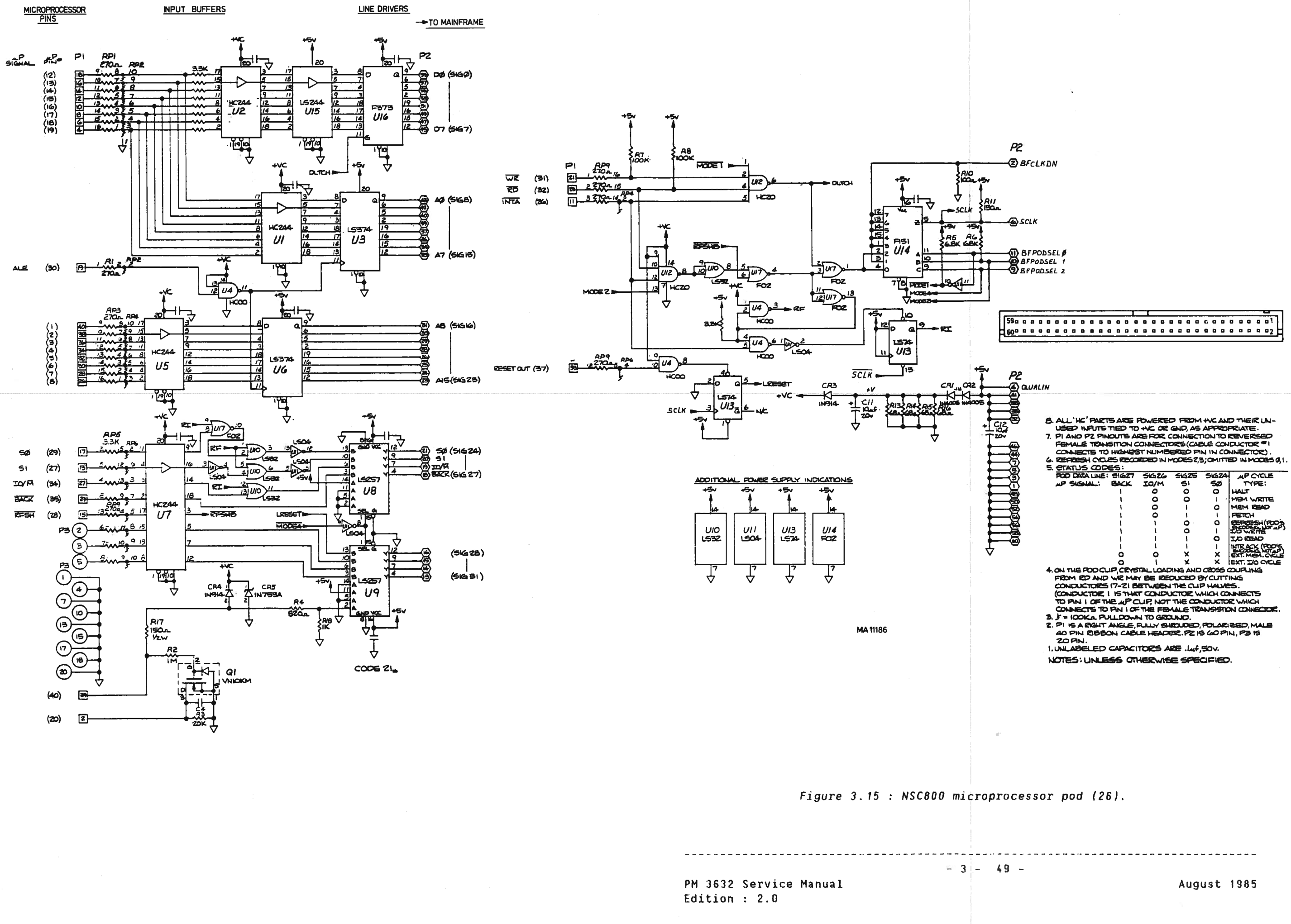
Three spare lines are available for user-defined connections to the system under test. These signals are buffered via the lower half of U7 before they are transferred to the mainframe (SIG29 ... SIG31).

The selection between internal clock (BFCLKOUT) or external clock is done under control of the microprocessor by means of signals BFPODSEL0...BFPODSEL2 (buffered pod select) which come from buffer U50 in the mainframe (see figure 2.7).
As an external clock the RD*, WR*, and INTA* lines are used (signal MODE1*).
In the NSC800 REFESH mode, also the RFSHB (refresh signal) is used as a clock signal. In this mode, also refresh cycles will be recorded in the PM 3632 mainframe (signal MODE2*).
All clock signals are combined via NAND gates (12, U17), which means that when one of them goes low, a clock pulse will be generated for the mainframe.

The microprocessor in the mainframe can read the identity of the pod by reading the contents of the lower halfs of buffers U8 and U9. This is done via signal lines SIG24 ... SIG31.
When doing this, the higher halfs of these buffers are disabled (signal MODE4*).

To protect the pod against pod connection errors, ground of the system under test is only connected to ground of the mainframe (via FET Q1) when the supply voltage (40) is at the correct position of the microprocessor clip. The microprocessor in the mainframe reads this information via buffer U9 and will display POD CONNECTION ERROR if the pod is not connected properly.

WARNING: When using the side probe, do not connect the ground wires! This will cause a short circuit between the drain and source of FET Q1.



8. ALL 'HC' PARTS ARE POWERED FROM +VC AND THEIR UNUSED INPUTS TIED TO +VC OR GND, AS APPROPRIATE.
7. P1 AND P2 PINOUTS ARE FOR CONNECTION TO REVERSED FEMALE TRANSITION CONNECTORS (CABLE CONDUCTOR #1 CONNECTS TO HIGHEST NUMBERED PIN IN CONNECTOR).
6. REFRESH CYCLES RECORDED IN MODES 2,3; OMITTED IN MODES Ø,1.
5. STATUS CODES:

POD DATA LINE:	SIG27	SIG26	SIG25	SIG24	µP CYCLE
µP SIGNAL:	BACK	IO/M	S1	SØ	TYPE:
	1	Ø	Ø	Ø	HALT
	1	Ø	Ø	1	MEM WRITE
	1	Ø	1	Ø	MEM READ
	1	Ø	1	1	FETCH
	1	1	Ø	Ø	REFRESH (POD'S BACK SIGNAL NOT µP)
	1	1	Ø	1	I/O WRITE
	1	1	1	Ø	I/O READ
	1	1	1	1	INTE ACK (POD'S BACK SIGNAL NOT µP)
	Ø	Ø	X	X	EXT. MEM. CYCLE
	Ø	1	X	X	EXT. I/O CYCLE

4. ON THE POD CLIP, CRYSTAL LOADING AND CROSS COUPLING FROM RD AND WR MAY BE REDUCED BY CUTTING CONDUCTORS 17-21 BETWEEN THE CLIP HALVES. (CONDUCTOR 1 IS THAT CONDUCTOR WHICH CONNECTS TO PIN 1 OF THE µP CLIP, NOT THE CONDUCTOR WHICH CONNECTS TO PIN 1 OF THE FEMALE TRANSITION CONNECTOR.
3. $\downarrow$ = 100KΩ PULL DOWN TO GROUND.
2. P1 IS A RIGHT ANGLE, FULLY SHIELDED, POLARISED, MALE 40 PIN RIBBON CABLE HEADER. P2 IS 60 PIN, P3 IS 20 PIN.
1. UNLABELED CAPACITORS ARE .1µf, 50v.

NOTES: UNLESS OTHERWISE SPECIFIED.

Figure 3.15 : NSC800 microprocessor pod (26).

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3.6.6 68000 & 68010 MICROPROCESSOR POD (see figure 3.21 and 3.22)

General

This pod (PM8874) supports the MOTOROLA 68000 and 68010 microprocessors.
Selection between these modes is done by a dip switch in the pod.

The pod has three different modes, which are under software control:

1. transparant mode
   All bus cycles that occur on the bus (also unused prefetches!) are sent to the mainframe. Unused prefetches are not disassembled by the disassembly software.
2. filtered mode
   All bus cycles, except for unused prefetches are sent to the mainframe. This prevents the mainframe to trigger on unused prefetches. Also unused prefetches do not use any memory in the mainframe.
3. jump mode
   Only bus cycles that caused a discontinuity in program flow are sent up to the mainframe.

Because the PM 3632 logic analyzer is only 32 channels wide, and for 68000/68010 support more channels are necessary, the data that is sampled from the bus is divided into two halfs. These two halfs are clocked into the mainframe sequentially. Sig31 indicates whether it is the first or the second half of the captured data (see below).

1st half: sig31 low
addresses (A1 ... A23) + R/W* + BGACK* + FC0...FC2 +
internally generated signals (FETCH*/SOURCE + BYTE + A0)

2nd half: sig31 high
data signals (D0 ... D15) + HALT* + VMA* + BERR* +
IPL0* ...IPL2* (depending on dip switch)

Using the PM 3632 together with a 68000/68010 uP pod affects the working of the mainframe trigger and data qualification circuits (see chapter 2).
For correct triggering, the triggerprom (labelled MT600-?) must always be installed at the PM 8880/30 disa board.
Also for correct operation of the mainframe together with this pod, main software revision L (or higher) must be installed.

The three different modes in which the pod can operate will be described in this paragraph separately. All three modes will be explained using the block diagram first.

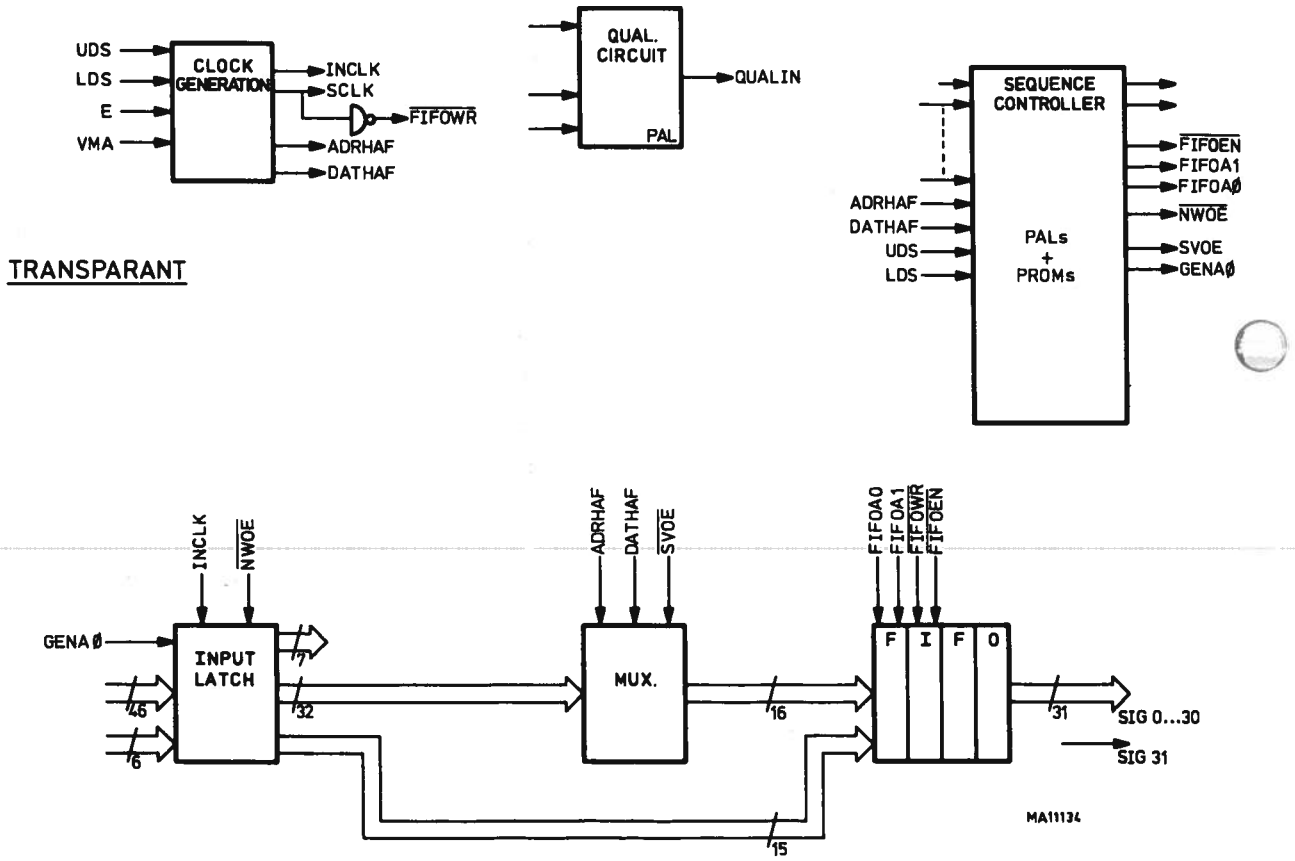


Figure 3.16: 68000/68010 uP pod block diagram (transparent mode).

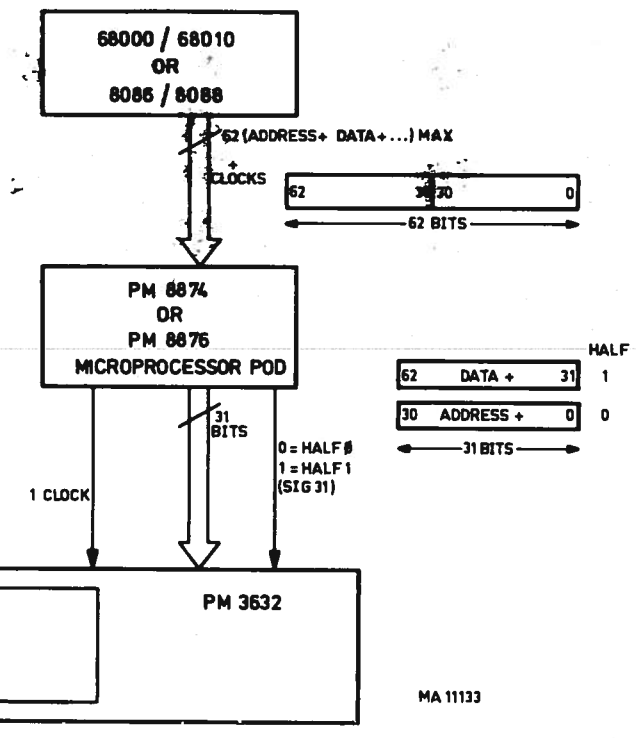
Block diagrams

-Transparent mode (see figure 3.16)

In the transparent mode, all bus cycles of the 68000/68010 microprocessors have to be transferred to the PM 3632 mainframe.

All the bus signals (52 lines), are clocked into the input latches on a clock pulse INCLK (comes from clock generation).
Addressline A0 which is not available on the 68000/68010 busses is generated inside the pod (GENA0).

After the data is latched into these input latches, this information has to be separeted into two halfs. This is because the PM 3632 mainframe can only handle 32 channels at a time (see picture below).



This division into two halfs is done by means of a multiplexer.
This multiplexer divides 32 channels into two halfs of 16 each.
the two halfs are clocked through the multiplexer on signals ADRHAF and DATHAF.
The other lines go to the mainframe together with each half, but are only once displayed at the state screen.

Both halfs pass a First-In First-Out memory (FIFO) before they are passed to the mainframe (SIG0 ... SIG30). SIG31 indicates which half is the address half (first) or the data half (second).
The address lines and enable pulse for the FIFO are generated by the sequence controller in the pod.
The write signal is generated by the clock generation circuitry.
In transparent mode, the FIFO is only one sample deep (because all cycles have to be transferred to the mainframe).

The following clock signals are generated by the clock generation circuitry:

- INCLK clocks information from the microprocessor busses into the input latches.
- SCLK Clocks 31 channels into the PM 3632 mainframe.
- ADRHAF Clocks the first half of information (addresses) through the multiplexer.
- DATHAF Clocks the second half of information (data) through the multiplexer.
- FIFOWR* writes information into the FIFO.

All these signals are generated from the following signals:

- UDS (Upper data strobe) and LDS (Lower data strobe) which generate these clock signals for all 68000/68010 bus cycles.
- E and VMA (Valid memory address) which generate these clock signals when the 6800/68010 communicates with a 6800 peripheral.

The clock signal that goes to the mainframe (SCLK) has to be qualified via signal QUALIN. In transparent mode, this signal is always high because all bus cycles have to be transferred to the mainframe.

In all modes, there is a sequence controller that controls everything that happens in the pod.
Input signals for this circuit are not all drawn, because they are not all used in this mode.
The sequence controller generates the following signals:

- FIFO address and enable lines (FIFOA0, FIFOA1, FIFOEN*).
- Output enable signals for input latches and multiplexer (NWOE*, SVOE).
- Address line A0 (GENA0).

-**Filtered mode** (see figure 3.17)

For this block diagram description, first read the transparent mode description.

In filtered mode, the pod works partly the same as in transparent mode. In order to disqualify unused prefetches, and thus not transfer them to the mainframe, the following special things are done:

1. Data bus cycle patterns are decoded. This makes it possible for a sequence controller to check if a sampled cycle pattern matches a known cycle pattern. If not, this sequence controller checks if there was an instruction prefetched which was not used.
   Under some circumstances, the pod may not be able to synchronize on these patterns correctly, which results in prefetches being removed (this can happen in a tight loop with no writes).
   Also a processor RESET will result in a los of synchronisation.
   Refer to the operating manual section for more details.
2. The lenght of the fifo is now 4 samples.
   This makes it possible for the sequence controller to decide whether the instructions in the fifo are really executed or not.

Conventions:

1. The 68000/68010 uP prefetch words. When a word is prefetched, it may be a part of an instruction which is not executed.
   When an instruction is prefetched but not used, it is not allowed to be transferred to the mainframe. Data and IACK (interrupt acknowledge) cycles must always be transferred to the mainframe.
2. When the 68000 or 68010 do a retry on a certain cycle (HALT* and BERR* are both low), then the cycle which is retried must not be captured a second time, because it was already captured once.
3. Cycles following the BG* (bus grant) are not sent up to the mainframe. These are cycles which are not performed by the 68000 or 68010, but for example by another uP (or DMA). In transparent mode these cycles are transferred to the mainframe!
4. Unremoved prefetches:
   - Three instructions (CHK, DIV and TRAPV) and the TRACE exception generate exceptions in a way that makes it difficult to remove all prefetches; in fact, it is sometimes impossible to know whether one or two prefetches need to be removed.
     In these cases only one prefetched word (the last) is removed.
   - Address and Bus Error exceptions do not have unused prefetches, but a cycle may be deleted anyway.
   - Another ambiguous circumstance occurs when the processor executes a single-word conditional branch around a one-word instruction that makes no data accesses. In this case it is sometimes impossible to tell if the one-word instruction is executed or not. In that case, in the disassembly display the one-word instruction will be marked with a ?. Refer to the operating manual section for more details.

In filtered mode, the datalines from the microprocessor, which are latched into the input latches, are passed to the sequence controller (NWD0 ... NWD15, new data).
The pattern that occurs on the databus is decoded in the sequence controller. After being decoded, it is compared to known patterns, stored in the sequence controller (PROM).
If the sequence controller can not match the patterns, then there must have been a prefetch or exception.

Data and address lines that go to the multiplexer circuit are also passed to a second row of latches. Information is clocked into these latches on SVCLK. This clock pulse is generated by the clock generation circuit, and is enabled by the sequence controller (signal SVCKEN).

When the sequence controller can not match a cycle pattern, then it will compare the address in the second row of latches (SVA, saved address) to the address in the input latches (NWA, new adress) + an offset (ALUCRY or SVD, saved data).
The result of this compare (CMPHI*) makes clear to the sequence controller if there was a discontinuity after the prefetched word or not.
If there was a discontinuity, then the prefetch was not excecuted and must not be transferred to the mainframe.
In some cases, the sequence controller has to activate a second compare in order to decide if the prefetch was excecuted ot not (result is signal CMPLO*).
Which offset it takes in the compare, and if it does a second compare or not, depends on the cycle pattern on the bus. Lines CT0,1,2 reflect which compare will be done.

If the sequence controller comes to the conclusion that a prefetch was not excecuted, then it will disqualify this cycle at the moment it will be transferred to the mainframe (via signal DISQUAL*).

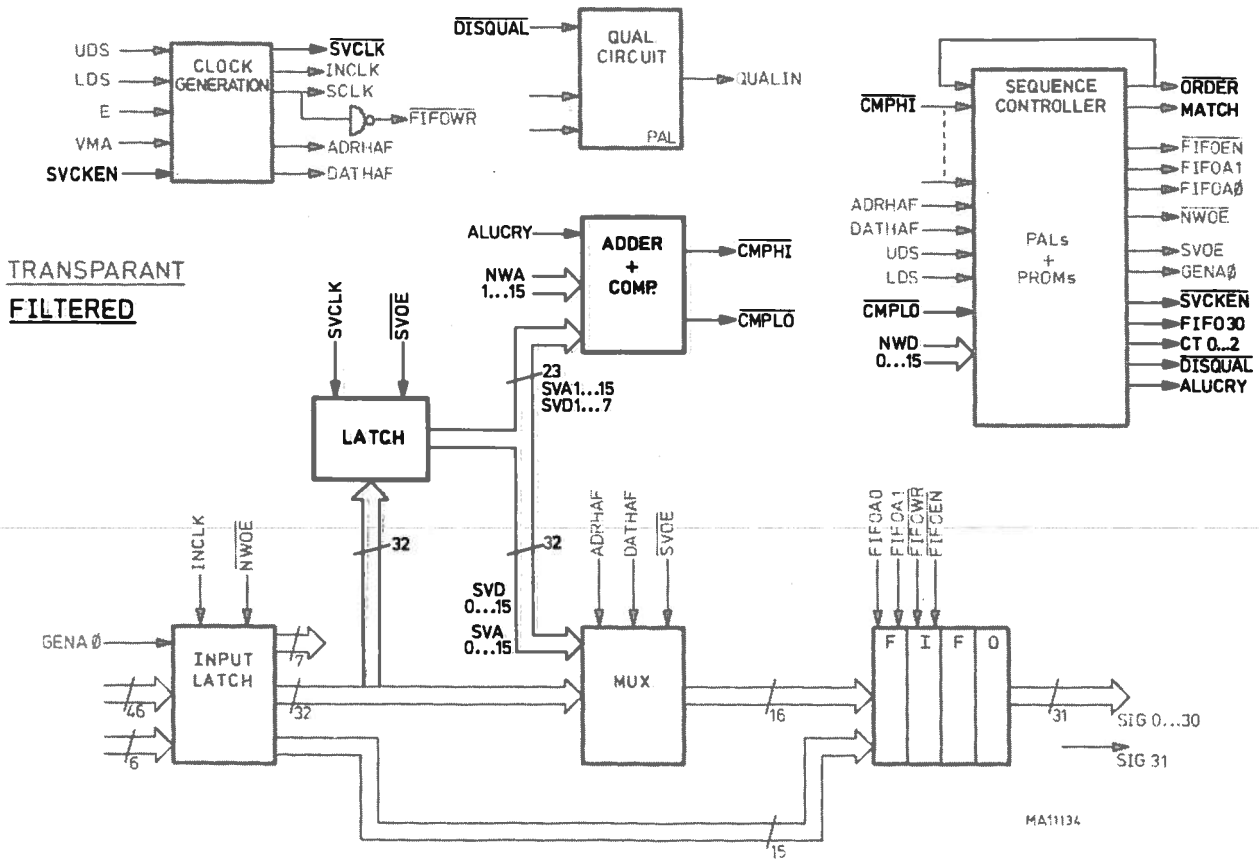


Figure 3.17: 68000/68010 uP pod block diagram (filtered mode).

TRANSPARANT

FILTERED

JUMP

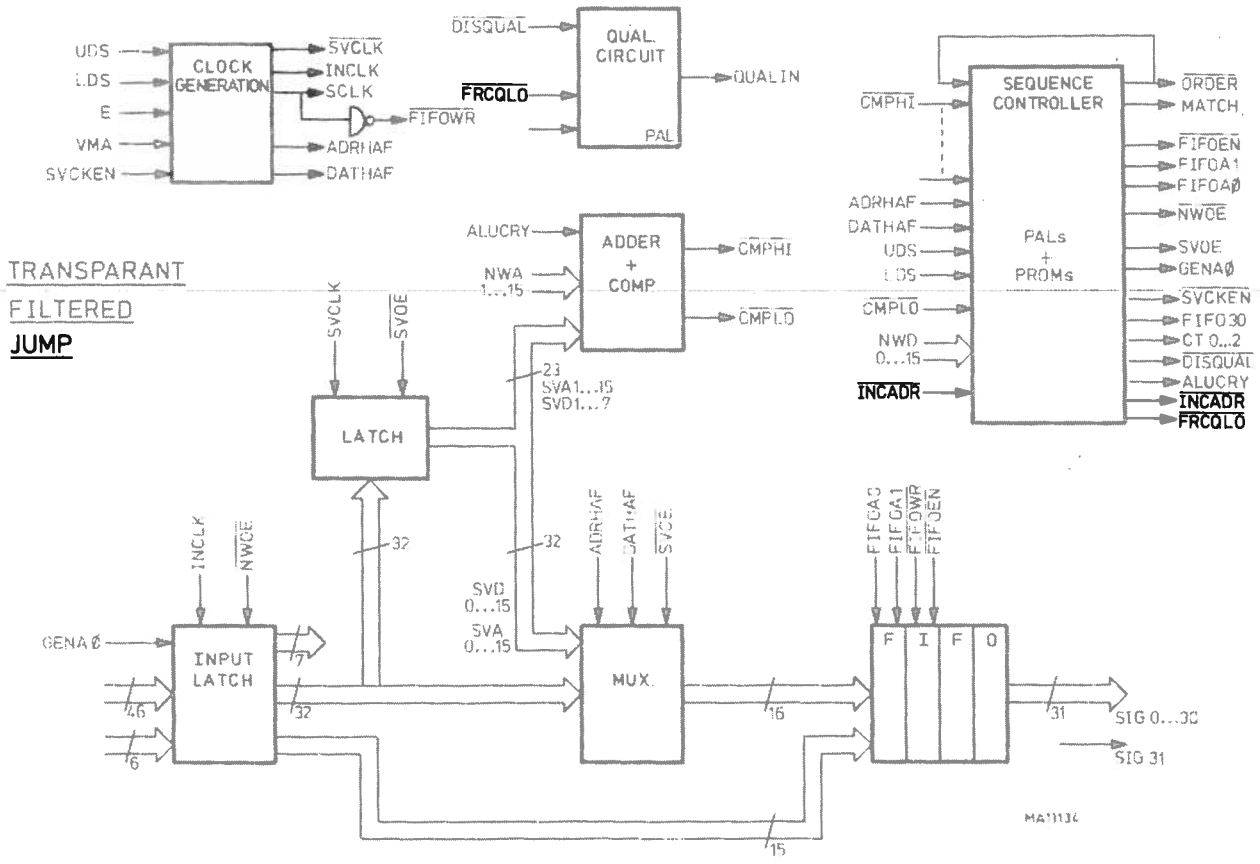


Figure 3.18: 68000/68010 uP pod block diagram (jump mode).

-Jump mode (see figure 3.18)

For this description, first read the block diagram desciptions of transparent and filtered mode.

In jump mode, only program discontinuities must be transferred to the mainframe.

In this mode, the sequence controller again detects a discontinuity in program flow by comparing cycle patterns.
As long as there is no discontinuity, the QUALIN signal that qualifies clocks to the mainfreame is forced low (via signal FRCQLO*).
At the moment when a discontinuity occurs, signal QUALIN will go high and the information will be stored in the mainframe.
After qualifying a discontinuity, the FIFO address lines will be incremented (INCARD*).

Circuit description

-Clock generation

For normal 68000/68010 cycles, the external clock for the pod is taken from signals UDS* (upper data strobe) and LDS* (lower data strobe). When one of these signals go high, a positive going INCLK (input clock) is generated via UL1,UK2. Signal INCLK will clock valid data, address and control/status information into the input latches.
Signal TAP0 (via flip flop UJ9) is then delayed in UK4 to generate the necessary timing signals to generate SCLK (selected clock, goes to mainframe), DATHAF (data half) and ADRHAF (address half). One INCLK pulse will generate two SCLK clock pulses, in order to clock the two halfs into the mainframe.This is shown in the timing diagram of figure 3.19.
For communication with 6800 (!) peripherals, the 68000 issues the VMA* (valid memory address) signal, which is synchronised with the 6800 peripheral using signal E (enable).
The E signal clocks a low VMA* level into flip flop UI1 which causes two SCLK pulses to clock the two halfs into the mainframe (see figure 3.19).

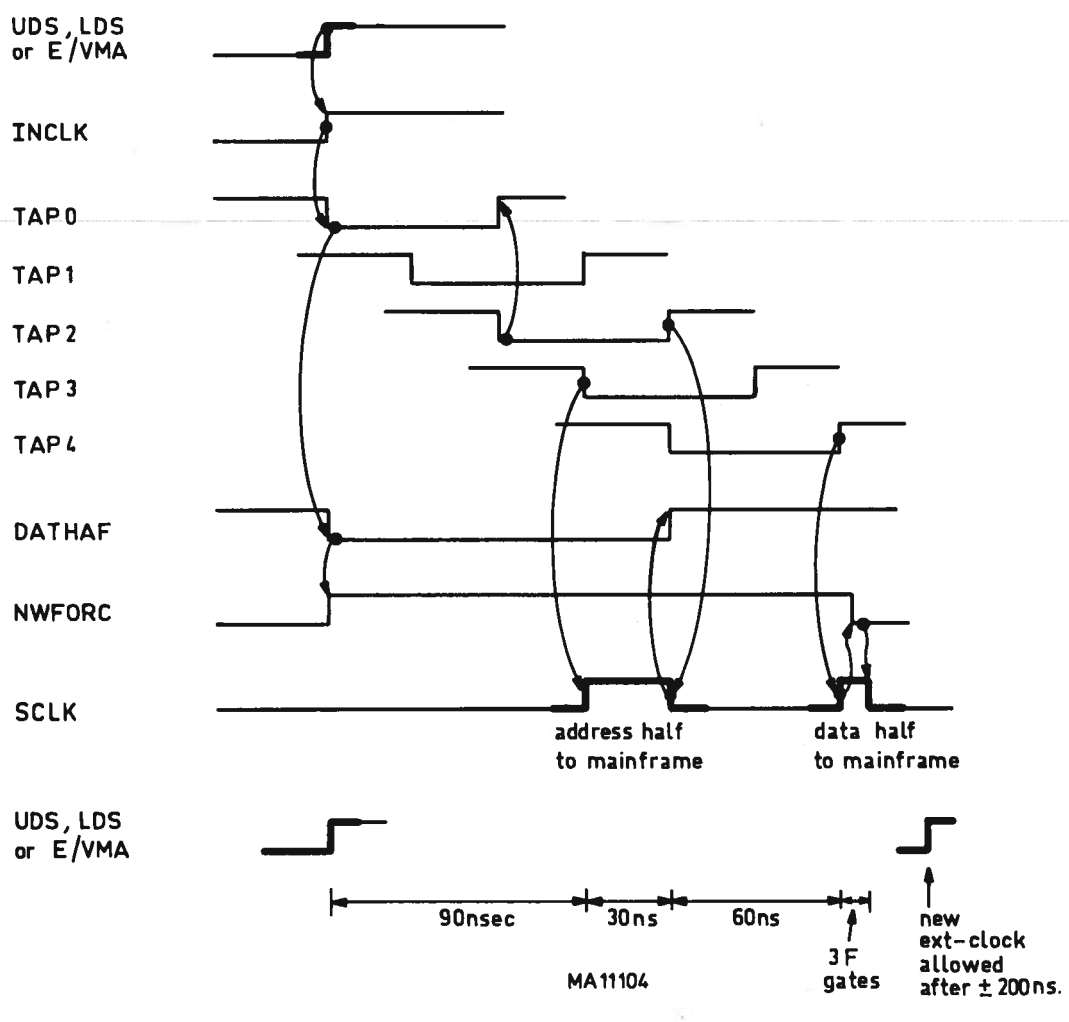


Figure 3.19: clock generation 68000/68010 disa pod.

-Transparent mode

Status of buffered pod select lines: BFPODSEL2 = 0, BFPODSEL1 = 0, BFPODSEL0 = 0.
Clock pulse INCLK (input clock) clocks the following data into the input latches (UE2, UH1, UD6-7, UD4-5, UC1-2, UD8-9, UD10-11):

addesses; A1 ... A23 + GENA0 (Generated A0, via PAL CYCTYP)
data ; D0 ... D15
control ; BERR*, VMA*, HALT*,
status ; R/W*, FC0 ... FC2,

Oepending on signal IPLSEL (interrupt priority level select, comes from dip switch 2), the IPL0...IPL2 or three spare channels (TST0 ... TST2) are connected to inputs 28 ... 30. This is done via multiplexer UA3-4.
In transparent mode, the outputs of the first row of latches are always enabled by a low signal NWOE* (new output enable not) and NWLSOE* (new status output) or a straight connection of the OE* pin to ground.

The information that is now in the first row of latches, goes via a first-in first-out memory (fifo, 32 bits x 8 ram, UL2 ... UL9) to the mainframe (SIG0 ... SIG30). In this mode the address lines for the fifo (FIFO0,FIFO1) are always stable, so the fifo is used as a register only.

first half

Because the mainframe is only 32 channels wide, the information in the input latches is divided into two halfs. During the first half (ADRHAF), the information in latches UC1-2 and UD4-5 (NWA0 ... NWA15, new addresses), is loaded into multiplexers UH4, UJ4, UF6 and UG5. Signal SVOE* (saved output enable not) is always high in this mode.
The outputs of these multiplexers (FIFO0 ... FIFO15) are connected to the fifo (UL2 ... UL5). During this half, the outputs of UH6, UJ5, UF7 and UG7 are tri-stated.
The outputs of latch UD6-7 and buffer UG3 (FIFO16 ... FIFO30) are connected to the fifo directly (UL6 ... UL9). During this half, the output of latch UH1 is tri-stated. Data from latch UE2 goes via buffer UG3 to the fifo (NWHS0 ... NWHS4). The information of the first half is written into the fifo on write pulse FIFOWR* (comes from clock generation UJ1).

second half

During the second half (DATHAF), the information in latches UD10-11 and UD8-9 (NWD0 ... NWD15, new data) is loaded intomultiplexers UH6, UJ5, UF7 and UG7.
The outputs of these multiplexers are also connected to the fifo (FIFO0 ... FIFO15).
During this half, the outputs of UH4, UJ4, UF6 and UG5 are tri-stated.
The outputs of latches UD6-7 and UH1 (FIFO15 ... FIFO30) are connected to the fifo directly.
During this half, the outputs of buffer UG3 are tri-stated. The information of the second half is also written into the fifo on write pulse FIFOWR*.

For both halfs, the location at which the information is stored in the fifo is pointed out by address lines FIFOA0, FIFOA1 and ADRHAF. Address line ADRHAF divides the fifo into two 4-samples deep shift register. One for the first half, and one for the second half (see figure 3.20). Address line FIFOA0 and FIFOA1 are generated out of signals TAP5 and PODSEL0; TAP5, in order to increment the address after every FIFOWR* pulse (via PAL FADDR, UJ10).

NOTE:
These address lines are both stable in transparent mode (PODSEL0 is low), in order to reduce the lenght of the fifo to one.

Signal FIFOEN* enables the output of the rams always, to send the data which is pointed out by the address lines up to the mainframe. FIFOEN* is high during the time that the mainframe reads the pod identity (via UL10).

> *NOTE:*
> *Note that because FIFOEN* is always low, information is sent up to the mainframe just before new information is written at the same location in the fifo.*

In transparent mode, all bus cycles must be transferred to the mainframe (also unused prefetches!). Therefore signal QUALIN (qualifier signal for clock to mainframe) is always held high via flip flop UK7 (near PAL UK8, QUAL).

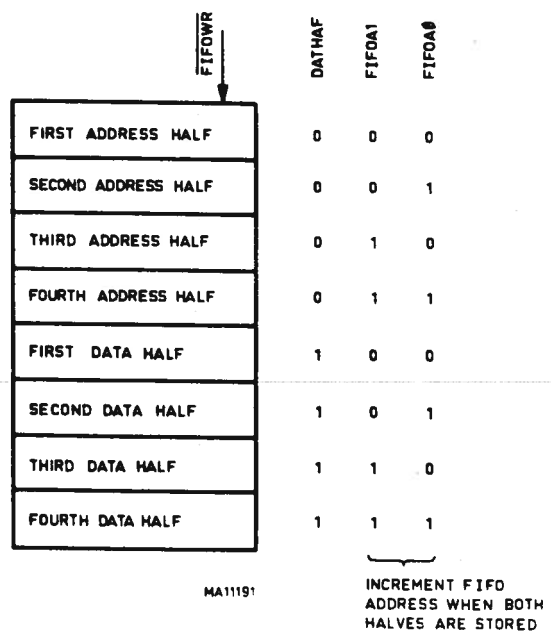


Figure 3.20: Fifo memory

-Filtered mode

NOTE: The following description of the pod in filtered mode decribes how the pod works in general. Because of the high complexity of the 68000 and 68010 microprocessors, there are some exceptions to this description. To explain all of these exceptions, a far too high knowledge of the 68000 and 68010 microprocessors would be required. Some faults in the pod may be caused by a part of the circuit which deals with these specific exceptions. If therefore you can not repair the pod with this description, just start replacing PALs and PROMs one by one.

After a new sample of addresses and data is in the input latches, the data part (NWD0 ... NWD15, new data) of this cycle is immediately going to PAL UE8-9 (DC0D68) and PROM UG9 (27128, DC68KP).
This circuit decodes every cycle pattern that appears on the data bus, and outputs an 8 bit code for every possible pattern (128 possibilities).
The outputs of the "pattern decoder" go via multiplexers UG9 and UH9 to a sequence controller: PROM UH9 (27128, ST68), PAL UK9, counter UG8 and flip flop UJ10.

This sequence controller does the following:

- It compares the incoming cycle pattern with the patterns stored in prom UG9. If the pattern matches a pattern stored in the prom, the sequence controller is synchronised. After synchronisation it is able to remove unused prefetches.
  If the seq. contr. can not match the incoming pattern, the following things can have happened:
  - the seq. contr. is out of synchronisation (can happen when: an unexpected program space read or a byte access occur)
  - a prefetch has occurred : prefetch is not used after a program discontinuity (caused by jump, branch etc.).
  - an exception has occurred: this causes a discontinuity in program execution.

When the seq. contr. detects that a prefetch occurred after an instruction cycle which may cause a discontinuity, it will make two calculations + compares within that cycle (one in every half).

first calc.: The seq.contr. will immediately make signal ALUCRY high. This signal is connected to an adder (UH3, UJ3, UF5, UG4). In this circuit a high signal ALUCRY is added to the saved address (address from previous sample) which is in the second row of latches (SVA1 ... SVA15). After this addition, the result (= old address + 2) is compared to the new address (NWA1 ... NWA15) in comparator UJ2 and UF4 (outputs of UH5 are zero due to a low TAP0).
When the old address + 2 = new address, than this means that there was no discontinuity.
This means that the prefetch was executed, and therefore must be transferred to the mainframe.
The result of this compare is signal ORDER*, via flip flop UK5.

second calc: For some cycle patterns however, this first compare is not enough to decide if the prefetch is executed or not (Branch short or long and JUMP).
This is also decoded in the seq. contr.. Output signals CT0 ... CT2 tell which compare has to be performed in the second compare (during data half):

short branch: Signal SHDOE* (via UK1) enables the outputs of latch UG6. Theses 8 bits are the offset portion of the short branch. The saved addresses are enabled via signal SVAOE* (via UJ8), and ALUCRY is low.
The result of the addition in UH3, UJ3, UF5 and UG4 (old address + short offset) is compared to the new address (NWA1 ... NWA15), in UJ2 and UF4.

long branch: Signal SVDOE* (via UK1, UJ1) enables the output of latch UH7. These 8 bits are a part of the long offset (the other part is not used in the compare). The saved addresses are enabled via signal SVAOE* (via UJ8), and ALUCRY is low.
The result of the addition in UH3, UJ3, UF5 and UG4 (old address + long offset) is compared to the new address (NWA1 ... NWA15), in UJ2 and UF4.

jump : Signal SVDOE* (via UK1, UJ1) enables the output of latch UH7. These 8 bits are a part of the destignation address of the jump (the other part is not used in the compare). The saved adresses are disabled (SVAOE*, via UJ8). The result of the addition in UH3, UJ3, UF5 and UG4 (jump address) is compared to the new address NWA1 ... NWA15, in UJ2 and UF4.

The result of this compare is signal MATCH* (via flip flop UK5).
Signals ORDER* and MATCH* are both fed back into the seq. contr. (PAL UK9, STATE), in order to "tell" the sequence controller if the prefetch which followed the program discontinuity was executed or not. If the prefetch was not executed, PAL UJ7 (NEWSAV) will make signal DISQUAL high.

PAL UK8 (QUAL) decides whether the information in the fifo must be transferred to the mainframe or not. It keeps track of the information in the fifo because it is synchronous to the clock that goes up to the mainframe (STCLK).
In filtered mode, this PAL looks at signal DISQUAL to qualify or disqualify the instructions in the fifo.
Because data cycles and interrupt acknowledge cycles must always be qualified, signals RATYP0,1 are connected to the QUAL PAL.
These signals are derived from the processor status lines FC0, FC1 (via latch UE2 -ACTYP0,1- via CYCTYP PAL UE1 -RFC0,1-).

ACTYP1	ACTYP0	
0	0	ignore (means retry or BG*, next cycle must not be sampled again). Signal IGNORE* stops the seq. contr. clock (STCLK via UH8, UK7, UJ8, UL1) in order to disgard the next cycle. Also fifo adress lines are not incremented (FADDR PAL).
0	1	data
1	0	instruction
1	1	IACK (in transparent mode, all cycles appear as IACK cycles)

This PAL also looks at signal LATEQ which is stored in the fifo together with the stored information. This signal is derived from signal SVOE*. It indicates if the information in the fifo is data/IACK or instructions.
Data/IACK cycles will always be transferred (SVOE* is high) instructions will only be sent to the mainframe if they are qualified (SVOE* is low).

The fifo which is now 4 samples deep, provides the necessary delay to make the decision if a prefetched instruction is executed or not.
This fifo is now used as a 4 deep shift register (see fig. 3.20), the addresses for the rams being provided by signals FIFOA0,1 (PAL UJ10, FADDR). In filtered mode, the address is incremented on clock pulse TAP5 (after an addresshalf and a data half have been written into the fifo). Signal IGNORE* prevents the address signals from incrementing when a retried cycle is captured, or after a BG* (bus grant).

Signal FIFO30 comes out of PAL UJ6 JUMP and informs the disassembler in the mainframe if the transferred information is an instruction fetch or data. Signal SVOE* (saved output enable not, generated by PAL UJ7 -NEWSAV-) is stored in the fifo together with the sampled information to indicate whether the stored information is an instruction cycle or a data/IACK cycle. This information (LATEQ) is passed to PAL UK8 (QUAL) which keeps track of all the information in the fifo in order to qualify or to disqualify the information when it is sent to the mainframe.

-Jump mode

In jump mode, only discontinuities must be transferred to the mainframe.
The JUMP PAL (UJ6) controls the qualification of instructions in JUMP mode.
Only the first word of an instruction is saved in the fifo.
In jump mode, the seq. contr. tells the JUMP PAL via signal DISQUAL whether the last captured instruction caused a discontinuity or not.
As long as there is no discontinuity, signal FRCQLO* stays low in order to force QUALIN low (via flip flops UJ10 and UK7). Signal INCADR* in that case is forced high in order to stop PAL UJ10 (FADRR) from incrementing the FIFO address lines.
As soon as there is a discontinuity, signal DISQUAL will make signal FRCQLO* high which will make signal QUALIN high in order to qualify the discontinuity.
The fifo adddress lines will be incremented.
In this mode signal FIFO30 tells the disasembler in the mainframe whether the address in the first half was a source or a destignation address.
Signals RATYP0,1 are used in this mode to increment the fifo address line also when an IACK cycle has occurred.

-Connection error and pod identity

To detect if the clip is connected correctly over the 68000/68010 uP, the 1458 (UC6) detects if the +5 V is on the correct pin of the clip (68KVcc). The first 1458 is only an invertor, and the second compares this voltage to a fixed reference voltage. If the voltage at pin 68KVcc is +5 V, FET Q1 connects ground of the system under test to ground of the pod. This protects the pod and the system under test against short circuits when the clip is connected incorrectly.

WARNING: The side probe (P3) has some pins connected to ground in the pod.
NEVER connect the ground wires of the side probe before fet Q1 has connected the ground of the target to the ground of the pod.
This will cause a short circuit of Q1 when the clip is not connected correctly!

To detect which pod is connected, the mainframe can read buffer UL10 via signal lines 24 ... 31 immediately after power-up. This buffer is selected via signal PODTYP* which comes from the BFPODSEL0 ... BFPODSEL2 lines (1,1,1).
Signal PTYPE indicates which mode the pod is set to by dip switch 1 (68000 or 68010 mode). The information if the pod is connected correctly is passed to the mainframe via one of the lines of this buffer.
During data acquisition, this buffer is tri-stated.

-Power supply

The power for the pod is derived from the -8.5 V power supply in the mainframe. UF10 outputs the switching frequency for transistors Q1 and Q2. When Q2 is switched-on, coil L1 is charged. As soon as transistor Q2 is switched-off, this coil will be discharged via diode CR2 (1N5822). This will cause a +5 V output voltage which is smoothened by coil L2 and C10.

repair methods

1. Check which pod mode if malfunctiong: transparent, filtered or jump.
2. Check power supply (derived from -8.5 V and +5 V).
3. If possible, go to transparent mode when repairing the pod.
   - Probe failure? Trace bad channel with an oscilloscope.
   - Check clock pulse (SCLK) to mainframe, and clock generation in pod.
   - Check if qualifier signal (QUALIN) ishigh.
   - Check selection signals for latches in data path (inputs-multiplexers-fifo).
4. If failure is in filtered or jump mode only:
   - Examine the customer's program, and check if it possibly contains instructions which cause unused prefetches to be transferred to the mainframe. Refer to the operating manual section for these instructions.
   - Check PROM checksums: UG9 (DC68KD) = 55A1 rev. A
     UH9 (ST68) = CCD6 rev. A
   - Check clock signal (SCLK) to mainframe and clock generation in pod.
   - Check if qualifier signal (QUALIN) goes high.
   - Replace PALs one by one and check if pod is working correctly.
5. Refer to the circuit descriptions for more details about the working of the pod.
6. If all repair attemps fail, you can return the pod to Concern Service for paid repair, via the normal repair procedure.

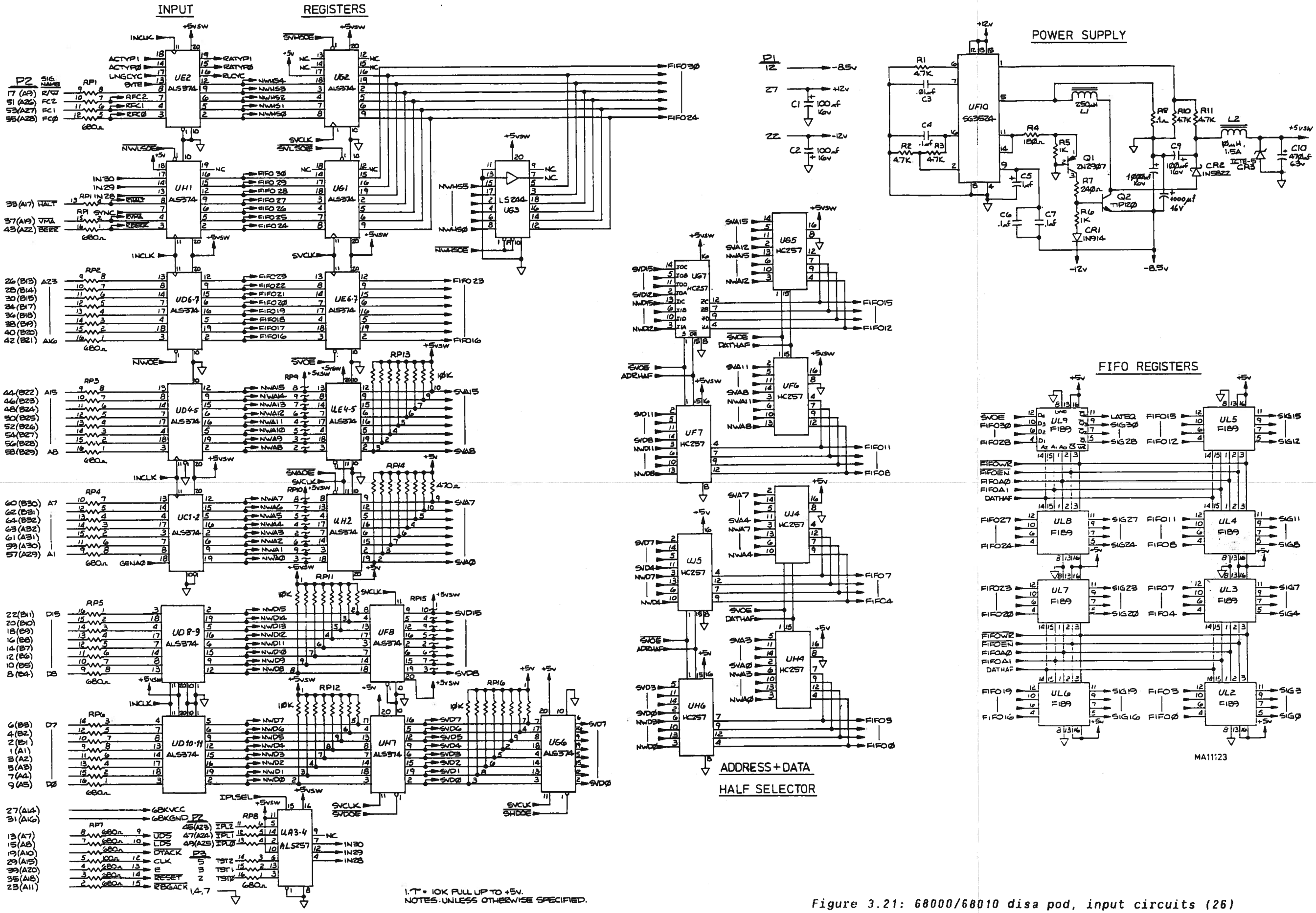


Figure 3.21: 68000/68010 disa pod, input circuits (26)

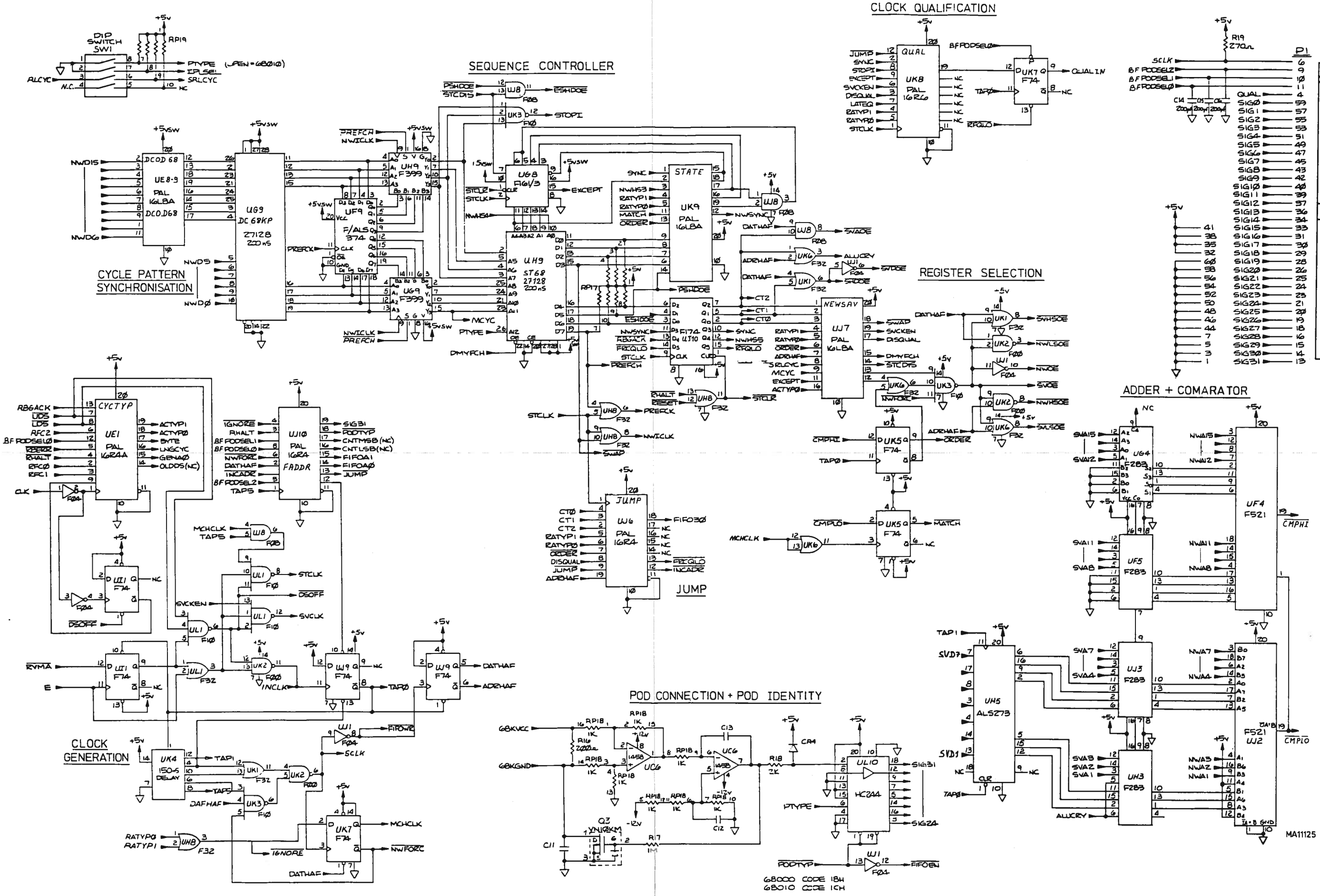


figure 3.22: 68000/68010 disa pod, sequence controller and clock circuitry (27)

3.6.7. 8086 & 8088 MICROPROCESSOR POD (see figures 3.29, 3.30 and 3.31)

General

This pod (PM8876) supports the INTEL 8086 and 8088 microprocessors.
Selection between these modes is done by a dip switch in the pod.
Like the 8086/8088 microprocessors, the pod has a minimum and a maximum mode.
Selection between these modes is also done by a dip switch in the pod. The position of this switch must correspond to the processor mode, or else the error message: POD CONNECTION ERROR will be displayed.

The pod has three different modes, which are under software control:

1. transparant mode
   All bus cycles that occur on the bus (also unused prefetches!) are sent to the mainframe. Unused prefetches are not disassembled by the disassembly software.
2. filtered mode (only in maximum mode !)
   All bus cycles, except for unused prefetches are sent to the mainframe. This prevents the mainframe to trigger on unused prefetches. Also unused prefetches do not use any memory in the mainframe.
3. jump mode (only in maximum mode!)
   Only bus cycles that caused a discontinuity in program flow are sent up to the mainframe.

Because the PM 3632 logic analyzer is only 32 channels wide, and for 8086/8088 support more channels are necessary, the data that is sampled from the bus is devided into two halfs. These two halfs are clocked into the mainframe sequentially. Sig31 indicates whether it is the first or the second half of the captured data (see below).

```
1st half: sig31 low
          addresses A0 ... A19 + S3 ... S6 +
           + min 8086: PHLD + IAK + M/IO* + DT/R* + DEN* + BHE*/S7
           + max 8086: LOCK + S2* + S1* + S0* + BHE*/S7
           + min 8088: PHLD + BHE* + IO/M* + DT/R* + DEN* + SS0*
           + max 8088: BHE* + LOCK* + S2* + S1* + S0*
2nd half: sig31 high
          data signals D0 ... D15 + spare signals (SIG17 + SIG18) +
          reset flag
```

Using the PM3632 together with an 8086/8088 uP pod affects the working of the mainframe trigger and data qualification circuits (see chapter 2).
For correct triggering, the triggerprom (labelled MT600-?) must always be installed at the PM8880/30 disa board.

The three different modes in which the pod can operate will be described in this paragraph separately. All three modes will be explained using the block diagram first.

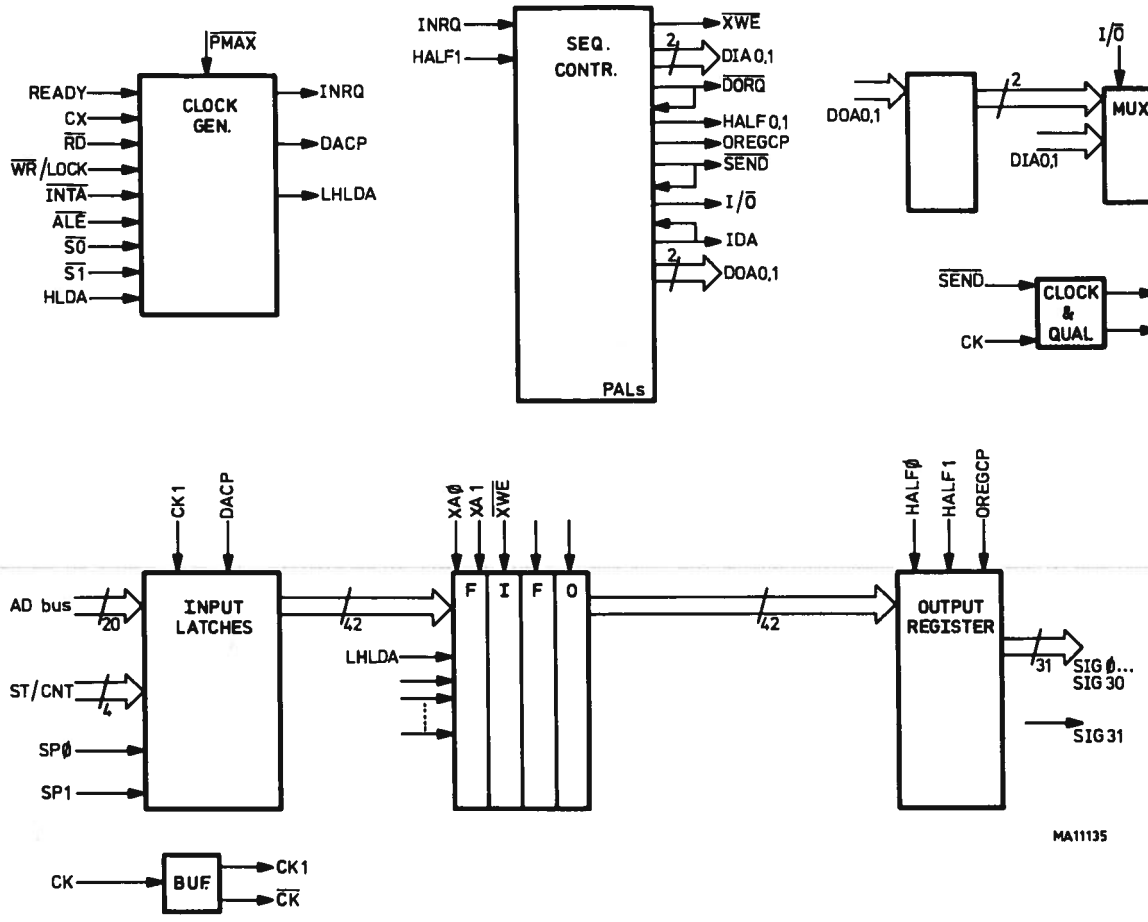


Figure 3.23: 8086/8088 uP pod, block diagram (transparent mode).

Block diagrams

-Transparent mode (see figure 3.23)

In the transparent mode, all bus cycles of the 8086/8088 microprocessors have to be transferred to the PM 3632 mainframe.
Therefore all cycles are treated as data cycles (data cycles always have to be stored in the mainframe).

Clock signals are generated differently in minimum and maximum modes:
minimum mode: In this mode, signals RD*, WR* and INTA* enable the sampling of the ready (READY) signal.
After this, the clock generator issues an INRQ (input request) signal to the sequence controller to indicate that there is valid data in the input latches.
maximum mode: S0* and S1* now enable the sampling of the ready (READY) signal.
After this, the clock generator issues the INRQ (input request) signal to the sequence controller to indicate that there is valid data in the input latches.
Signal DACP is issued as soon as there are valid addresses available on the microprocessor bus.

All the data signals, are continuously clocked into the input latches on clock pulse CK1 (is the processor clock signal CK).
When there are valid addresses on the bus, they are latched in the input latches on clock pulse DACP.

When there is valid information in the input latches, the sequence controller will store this information in the fifo by generating a write pulse (XWE*) and incrementing the fifo address lines (XA0, XA1).
This is done after the input request signal (INRQ) became active.

After the input request is accepted (signal IDA), and valid information is in the fifo, the sequence controller will notice that there is a difference between the input address (just incremented) and the output address (DOA0,1).
Therefore, it will generate an output request (DORQ*) in order to transfer the information in the fifo to the mainframe.
The valid information in the fifo will be addressed via the DOA0,1 (data output address 0,1) lines, and clocked into the output latches on the OREGCK clock pulse.

After the valid information is stored in the output registers, the sequence controller will transfer this information to the mainframe in two halfs: an address half and a data half.
This is done by enabling the two halfs of the output registers one at a time (signal HALF0 and HALF1, come from sequence controller).
The sequence controller will enable two SCLK clock pulses for the mainframe (via signal SEND*) to clock the two halfs into the mainframe.

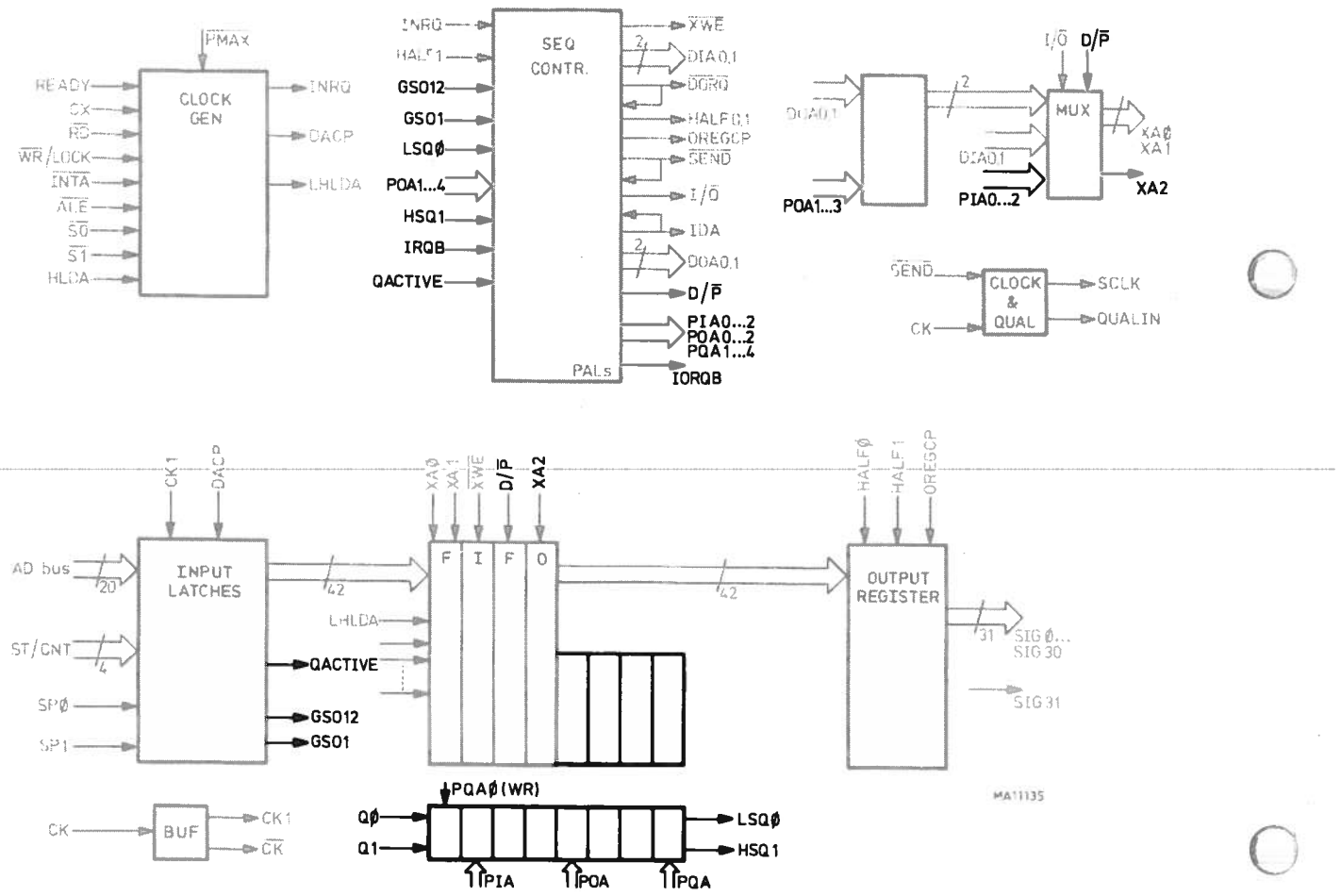


Figure 3.24: 8086/8088 uP pod block diagram (filtered mode).

-**Filtered mode** (see figure 3.24)

For this block diagram description, first read the transparent mode description.

In filtered mode, the pod works partly the same as in transparent mode. In order to disqualify unused prefetches, and thus not transfer them to the mainframe, the following special things are done:

1. to keep track of unused prefetches, the queue status (Q0, Q1) information must be stored also.
2. when sending instructions up to the mainframe, this queue status information must be checked whether the instruction was executed or not.
   In this way unused prefetches will not be sent up to the mainframe.
   Data cycles will always be sent up to the mainframe.

Conventions:

1. In the 8086 and 8088, only an instruction can be prefetched and not used.
   Therefore, only instructions must be checked if they are used or not.
2. Data and IACK (interrupt acknowledge) cycles must always be transferred to the mainframe.

In filtered mode, the input request and output request are performed similarly to the process in transparent mode.
In filtered mode however, the pod keeps track of which input request was due to an instruction fetch, and which one was due to a data cycle.

Therefore, status signals S0*, S1* and S2* are also latched and combined into signals GS01 and GS012.
The sequence controller sets signal D/P* (data/program) to the correct level when there is an input request (INRQ), depending on the state of signals GS01,GS012.
When the input request is for data, the addresss for the fifo is only two bits (XA0,XA1 via DIA0,1 -data input address-). This makes the fifo 4 samples deep.
When there is an input request for instructions (possibly prefetches!!), the fifo is 8 bytes deep (=4 samples; address line XA2 is also used, via PIA0,1,2 -program input address-).

In order to be able to judge if a sampled instruction was reallly executed, the pod monitores the queue status lines (Q0,Q1) and stores this information in an 8 x 2 (bits) x 2 (bytes) register file.
At every input request, which was caused by an instruction fetch (detected by the sequence controller), 4 bits are initialized in the register file (2 queue status bits for every byte). The address of these 4 bits is pointed out by address lines PIA0 ... PIA2.

As soon as there is queue activity in the 8086/8088 CPU (which means that something happened to an instruction byte in the queue), signal QACTIVE* will go low.
After this queue activity, the sequence controller will produce a write pulse (PQA0) for the register file in which the two queue status bits Q0 and Q1 will be written into the register file on a position that corresponds with the affected instruction byte (which is already in the fifo). This location in the register file is pointed out by queue address lines PQA1 ... PQA3.
After this write action, the queue address lines will be incremented.

As soon as there has been queue activity, the sequence controller will increment the queue address lines, and generate an output request for the affected instruction byte (IORQB).
However, this output request will not be granted if the contents of the register file (LSQ0 and HSQ0) indicates that the instruction byte was not executed.
The address of the instruction byte is pointed out by output address lines POA0 ... POA3 (go to fifo via multiplexers).

-**Jump mode** (see figure 3.25)

For this block diagram description, first read the transparent and filtered mode descriptions.

In jump mode, only discontinuities in program flow must be transferred to the mainframe.
If there was a discontinuity, is reflected by the queue status lines (Q0 and Q1), which are stored in the register file.
If the pod is set to this mode, the sequence controller will only qualify the information when it was due to a program discontinuity.

In this mode, two different modes of operation can be selected:
- show all discontinuities
- show only discontinuities due to an interrupt

Signal IDISC "tells" tells the sequence controller which mode is selected (IDISC is set by a dip switch).

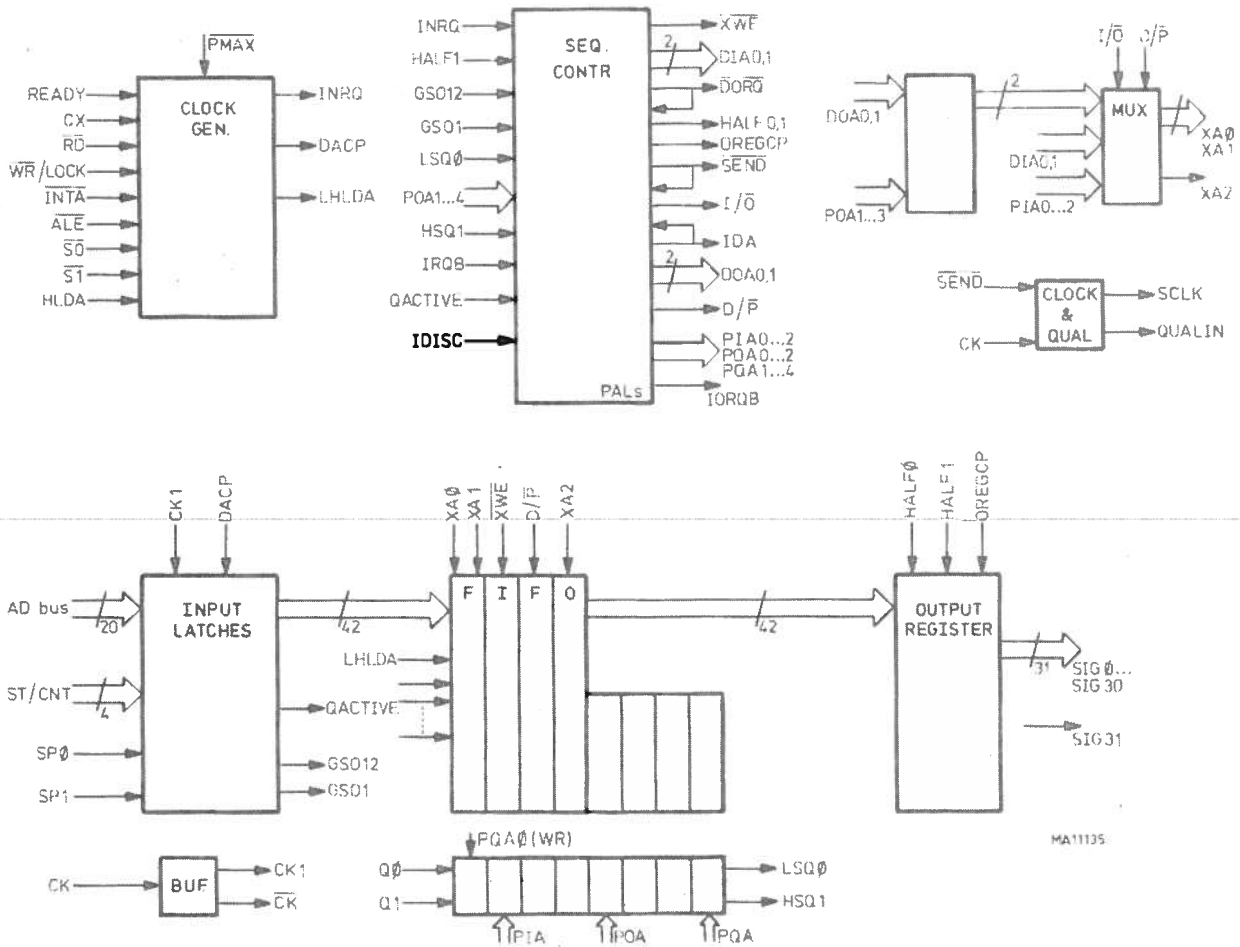


Figure 3.25: 8086/8088 uP pod block diagram (jump mode).

Circuit description

-Clock generation (see figure 3.26)

The external clock is derived from the READY signal from the 8086/8088 micros. This signal is sampled continuously by the microprocessor clock CK (in U64). When valid data is in the input registers, the clear input of this flip flop is released (via U59) to generate signal INRQ (input request). In minimum mode and maximum mode this is done in different ways.
The direction of U59 is set by the PMAX* signal (set via dip switch 1, which selects min and max mode).

Min mode:

* The release of the clear input (U64) comes as soon as the RD*, WR* or INTA* line goes low, which indicates that there is a read, write or interrupt acknowledge cycle being performed. This signal will be sampled on the next negative going edge of the microprocessor clock (CK*, in U52). The output of U52 will enable flip flop U64 via U59.
  In min mode, a high signal HLDA* (hold acknowledge, not) will stop the sampling of the RD*, WR* and INTA* (via U47, U57 signal LHLDA). This means that only 8086/8088 cycles will be transferred to the mainframe (no DMA cycles). Signal LHLDA* indicates to the mainframe which was the last cycle before a DMA cycle. The next 8086/8088 cycle will make LHLDA* high again.
  The ALE signal is also passed via multiplexer U59 in order to clock valid addresses into the input registers (signal DACP).

Max mode:

* The release of the clear input (U64) comes as soon as the S0* or the S1* status signal goes low. This low signal will release the clear input of flip flop U52A, which will sample a one on the next CK pulse. On the next CK pulse, a one will be sampled in flip flop U52B, which will release the clear input of U64 via multiplexer U59. Now the ready signal can be sampled on the next clock pulse CK.
  The one which is clocked into flip flop U52A will also generate a DACP clock pulse for clocking valid addresses into the input registers (30 ns later after clock pulse CK).

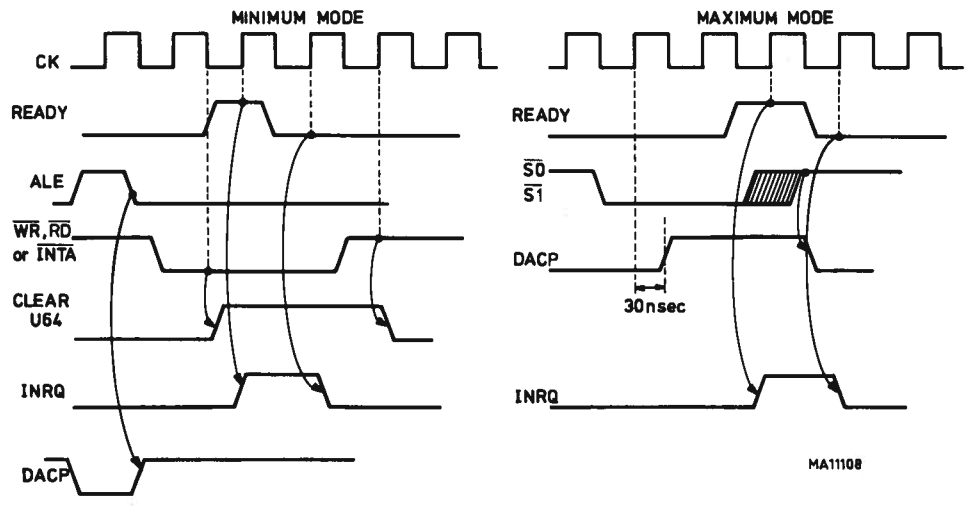


Figure 3.26: Clock generation, 8086/8088 disa pod.

-Transparent mode (see timing diagram of figure 3.27)

Input latches U2 ... U7 latch the following signals from the 8086/8088 bus:
- addresses (A0 ... A19) and control/status signals (M/IO*, S2*, S1*, S0*, DT/R*, DEN*, BHE*, S7*, SS0).
  These signals are sampled on every clock pulse DACP (from clock gen.).
  The control/status signals which are sampled, depend on the processor mode (see general).
- data (D0 ...D15) and status signals (S3 ... S6) are sampled continuously on every falling edge of the processor clock (CK1*).
- two spare channels are sampled in latch U25.

The outputs of the input latches are always enabled.

WARNING: The side probe (P3) has some pins connected to ground in the pod.
NEVER connect the ground wires of the side probe before fet Q3 has connected the ground of the target to the ground of the pod.
This will cause a short circuit of Q3 when the clip is not connected correctly!

The information in the latches, goes via a first-in first-out memory (fifo U11 ... U21) and output latches(U23, U24, U28 ... U32) to the mainframe (SIG0 ... SIG31).
In this mode, the fifo is used as a register only.

When there is valid data present on the 8086/8088 bus, signal INRQ (input request) will be generated by the clock circuitry (U64). This INRQ signal is connected to PAL U37 (86ARB) which will subsequently:
1. enable one write pulse for the fifo (XWE*) to store valid data at the next rising edge of the processor clock (CK, via U51)). Signal I/O* high indicates that there is input data.
2. generate an IDA (input data accepted) pulse which indicates that there is input data accepted.
   Signal D/P* (data/program) high indicates that the information in the fifo is data (not an instruction). In transparent mode this signal is always high.

Signal IDA is connected to PAL U36 (86DIO) which will subsequently do the following:
1. increment its data input pointers (DIA0,1) which will via multiplexer U39 increment the address lines XA0 and XA1 of the fifo. This causes new info to be written on a new address in the fifo on the next input request (INRQ).
2. then generate an output request (DORQ*, data output request not), because there is information in the fifo which has to be transferred to the mainframe. This DORQ* signal will cause PAL U37 (86ARB) to generate an OREGCK (output registerclock pulse) pulse which clocks the information from the fifo into the output registers (U23, U24, U28 ... U32). The address from which the information is read, is pointed out by the output pointers (DOA0,1 via U39; selected with a low signal I/O* and a high signal D/P*).
   Signal SEND* goes low and qualifies two clock pulses (CK) for the mainframe via U41 (SCLK). These two clock pulses will clock two halfs into the input-registers in the mainframe (HALF0* and HALF1*, enable the output register halfs; come from PAL U37).
   A low signal SEND* will also increment the output address pointer (DOA0,1) via PAL U36 (86DIO).

   The output request signal (DORQ*, PAL U36) is not generated when there is still an input request being handled (INRQ) or the previous information is not yet transferred to the mainframe (HALF1*).

Now the cycle is completed and the pod can accept new data again.

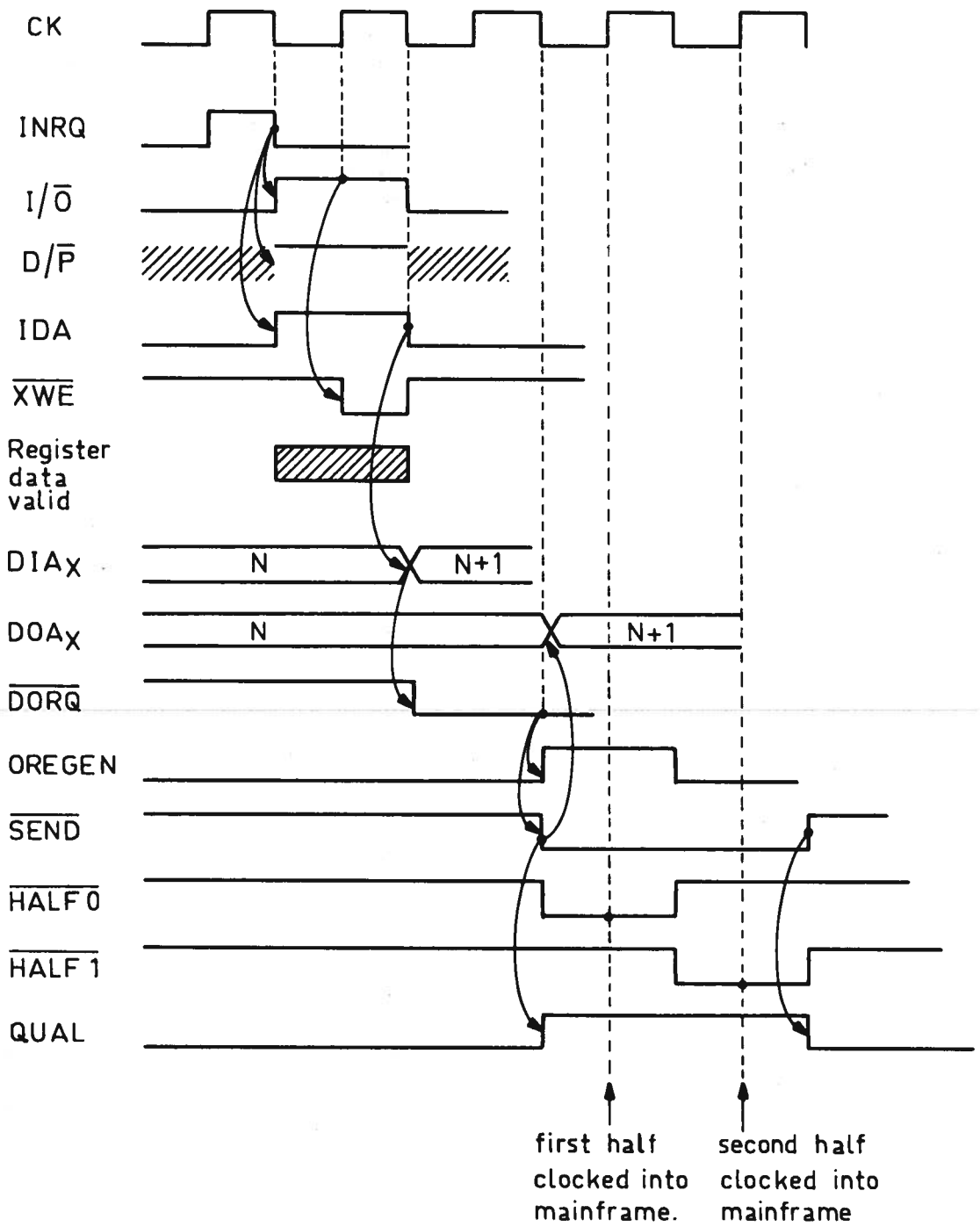


Figure 3.27: Tranparent mode, timing example.

-Filtered mode

NOTE: The following description of the pod in filtered mode decribes how the pod works in general. Because of the high complexity of the 8086 and 8088 microprocessors, there are some complex details omitted in this description. To explain all of these details, a far too high knowledge of the 8086 and 8088 microprocessors would be required. Some faults in the pod may be caused by a part of the circuit which deals with these specific details. If therefore you can not repair the pod with this description, just start replacing PALs one by one.

In filtered mode, the input request and output request are performed similarly to the process in transparent mode (see also figure 3.27).
In filtered mode however, the pod keeps track of which input request was due to an instruction fetch, and which one was due to a data cycle.

Therefore, status signals S0*, S1* and S2* are monitored (U6 and U7, IS0*, IS1*, IS2*). These signals are combined into signals GS01 and GS012 (in U58 and U65).
PAL U37 (86ARB) sets signal D/P* (data/program) to the correct level when there is an input request (INRQ), depending on the state of signals GS01,GS012.
When the input request is for data, the addresss for the fifo is only two bits (XA0,XA1 via U39 derived from DIA0,1 -data input address-)). This makes the fifo 4 samples deep.
When there is an input request for instructions (prefetches!!), the fifo is 8 bytes deep (=4 samples; address line XA2 is also used, via U40 derived from PIA0,1,2 -program input address-).

In order to be able to judge if a sampled instruction was reallly executed, the pod monitores the queue status lines (Q0,Q1) and stores this information in an 8 x 2 (bits) x 2 (bytes) register file (U45 and U46, see figure 3.28).
At every input request, which was caused by an instruction fetch (via PAL U44, 86PIO), 4 bits are initialized in the registed file (2 queue status bits for every byte). The address of these 4 bits is pointed out by address lines PIA0 ... PIA2.

As soon as there is queue activity in the 8086/8088 CPU (which means that something happened to an instruction byte in the queue), signal QACTIVE* will go low via U1 and U62 (signals Q0 and Q1).
After this queue activity, signal PQA0 will produce a write action for the register file (via PAL U44, 86PIO), in which the two queue status bits Q0 and Q1 will be written into the register file on a position that corresponds to the affected instruction byte (which is already in the fifo). This location in the register file is pointed out by queue address lines PQA1 ... PQA3.
After this write action, the queue address lines will be incremented (PAL U44, 86PIO).

As soon as there has been queue activity, and the queue address is incremented, PAL U43 (86POA) will generate an output request for the affected instruction byte. This is done via U50 and PAL U37 (86ARB). However, this output request will not be granted if the contents of the register file (LSQ0 and HSQ0) indicates that the instruction byte was not executed (via U50).
The address of the instruction byte is pointed out by output address lines POA0 ... POA3. These lines go to the fifo via U38, U39/U40.

If an instruction byte is output, then signal IORQB (instruction output request busy) will feedback to PAL U36 (86DIO) that there is an instruction output busy, so no data output request can be given.
The request to send instructions out will be ignored if there is an input request pending (signal INRQ, U54) or the pod is still busy sending out previous information (signal HALF0*).

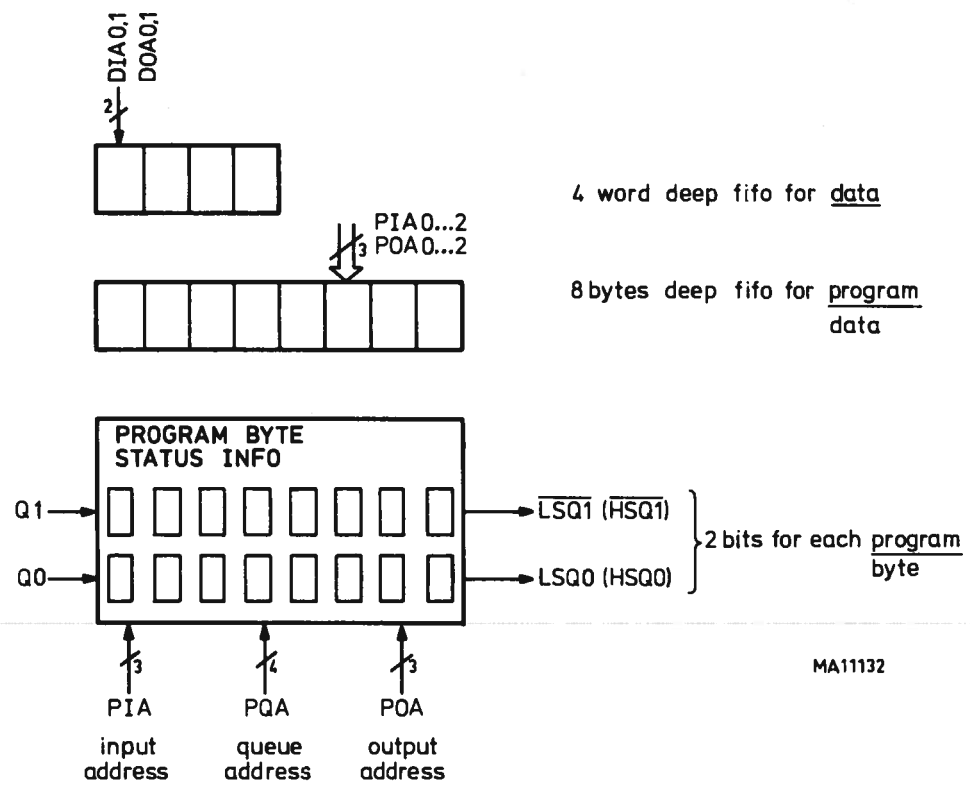


Figure 3.28: Register file storing queue status information.

Repacking:
The 8086 microprocessor prefetches words, but an instruction is built-up with a number of bytes. In filtered mode, the pod will normally transfer each byte to the mainframe immediately when it is executed by the CPU.
In the repack mode however, the pod will wait sending-up an instruction byte until the second byte of the prefetched instruction word is executed also. In this way, only words will be transferred to the mainframe, using memory space more efficiently.
PAL U37 (86ARB) will now only enable the instruction output request, when the high and the low byte of an instruction are executed (via U55, signals HSQ0,1 and LSQ0,1 derived from register file).
Then a complete word (the same as the one that was prefetched) will be transferred to the mainframe. Signals SIG29 and SIG30 indicate which byte of an instruction was the first byte of an instruction (via U53, U61 and U63).

-Jump mode

In jump mode, only discontinuities in program flow must be transferred to the mainframe.
If there was a discontinuity, it will be detected by the queue status lines (Q0 and Q1) which are stored in the register file (U45, U46). Multiplexer U55 will pass the queue status information from the register file to the 86ARB PAL. This PAL will then only allow an output request when there was a discontinuity.
Two modes of operation are possible (dip switch setting):

- show only discontinuities due to interrupts.
  When signal IDISC* (interrupt discontinuities) is low, all discontinuities due to an interrupt will be sent up to the mainframe. PAL U37 (86ARB) makes this decision. SIG30 indicates to the mainframe if the instruction that was sent was the source or the destignation of the discontinuity. Signal MTD* indicates the source (emptied queue).
- show all discontinuities.
  When signal IDISC* is high, all discontinuities will be sent up to the mainframe. In this case, signal SIG29 will indicate whether the discontinuity was due to an interrupt or not (via U61, IAK int. acknowledge).

-Connection error and pod identity

To detect if the clip is connected correctly over the 8086/8088 microprocessor, pin 40 of the microprocessor is checked for +5 V.
This information is passed to the mainframe when it reads the pod identity.
When the +5 V is on the correct pin of the clip, the ground of the pod will be connected to ground of the target system via fet Q3

To detect which pod is connected, the mainframe reads prom U42 via signal lines 24 ... 31 immediately after power-up. This is selected via signal BFPODSEL2.
Depending on the position of the dip switches, this prom will output a different code when it is selected.
min mode 8086: 17H
max mode 8086: 23H
min mode 8088: 18H
max mode 8088: 26H

-Power supply

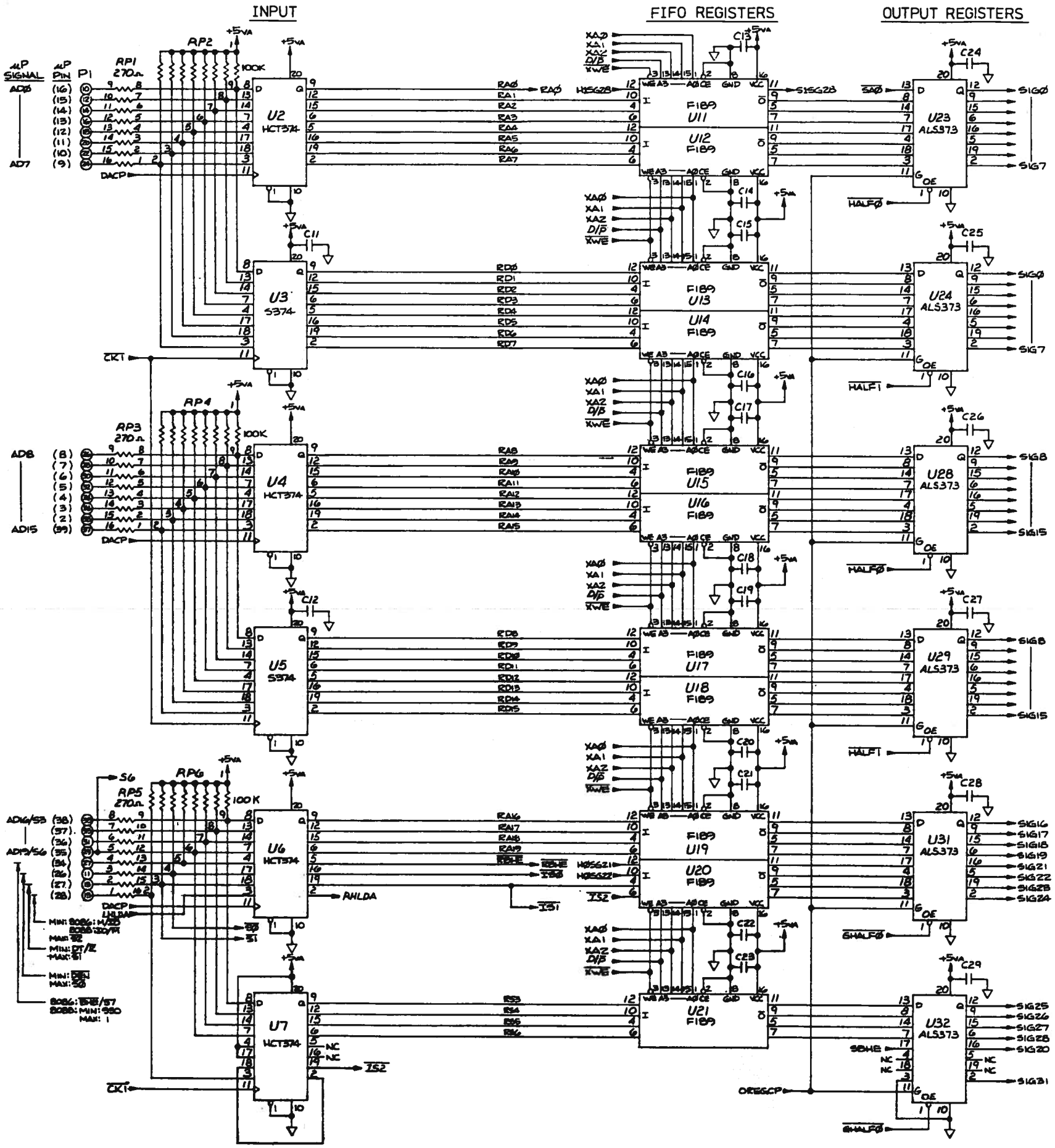
The power for the pod is derived from the -8.5 V power supply in the mainframe. U60 outputs the switching frequency for transistors Q1 and Q2. When Q2 is switched-on, coil L1 is charged. As soon as transistor Q2 is switched-off, this coil will be discharged via diode CR2 (1N5822). This will cause a +5 V output voltage which is smoothened by coil L2 and C10.

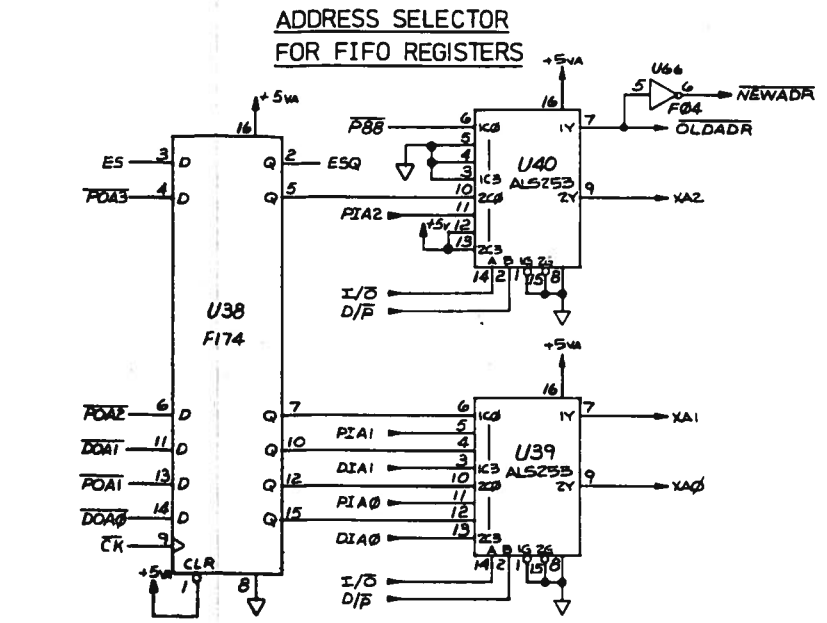
-not used circuitry

The circuit consisting of U8 ... U10, U22, U34, U33, U26 was intentionally used to record the queue activity between bus cycles. This circuit however is now not used by the software in the mainframe.

repair methods

1. Check which pod mode if malfunctiong: transparent, filtered or jump.
2. Check power supply (derived from -8.5 V and +5 V).
3. If possible, go to transparent mode when repairing the pod.
   - Probe failure? Trace bad channel with an oscilloscope.
   - Check clock pulse (SCLK) to mainframe, and clock generation in pod.
   - Check if qualifier signal (QUALIN) is high.
   - Check selection signals for latches in data path (inputs-fifo-output registers).
4. If failure is in filtered or jump mode only:
   - Examine the customer's program, and check if it possibly contains instructions which cause unused prefetches to be transferred to the mainframe. Refer to the operating manual section for these instructions.
   - Check clock signal (SCLK) to mainframe and clock generation in pod.
   - Check if qualifier signal (QUALIN) goes high.
   - Replace PALs one by one and check if pod is working correctly.
5. Refer to the circuit descriptions for more details about the working of the pod.
6. If all repair attemps fail, you can return the pod to Concern Service for paid repair, via the normal repair procedure.





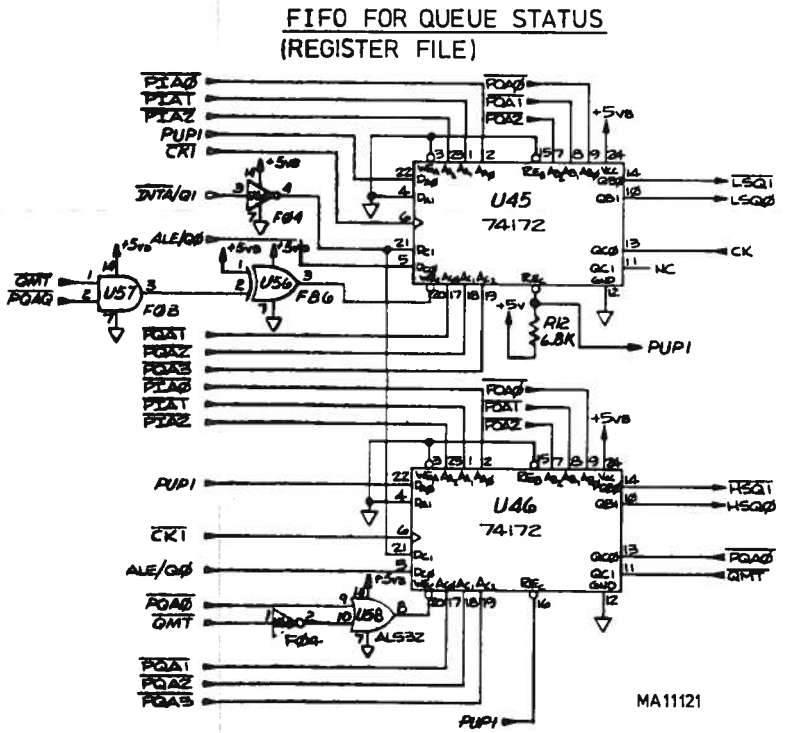


Figure 3.29: 8086/8088 disa pod, input circuits.

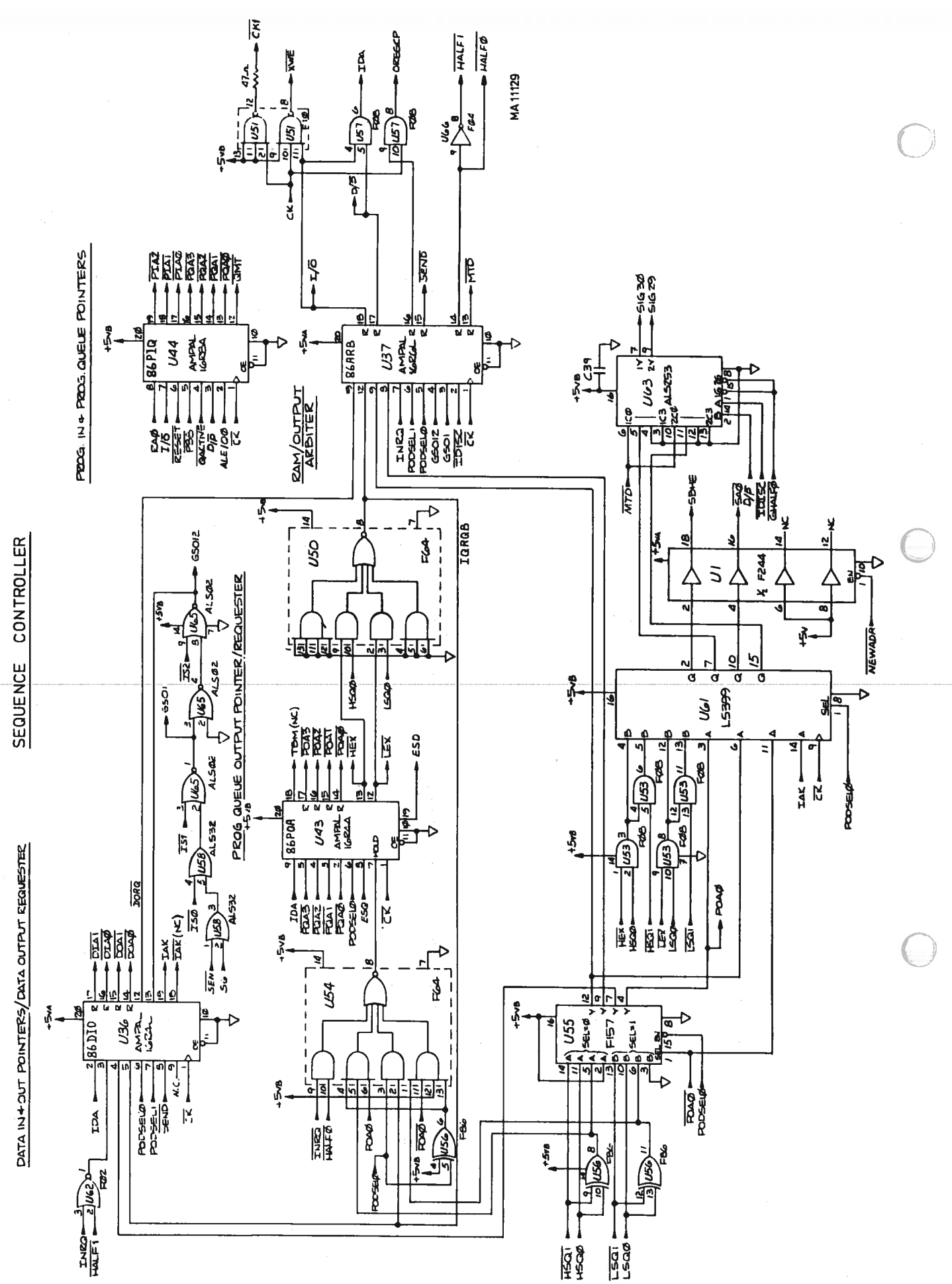


figure 3.30: 8086/8088 disa pod, control circuitry.

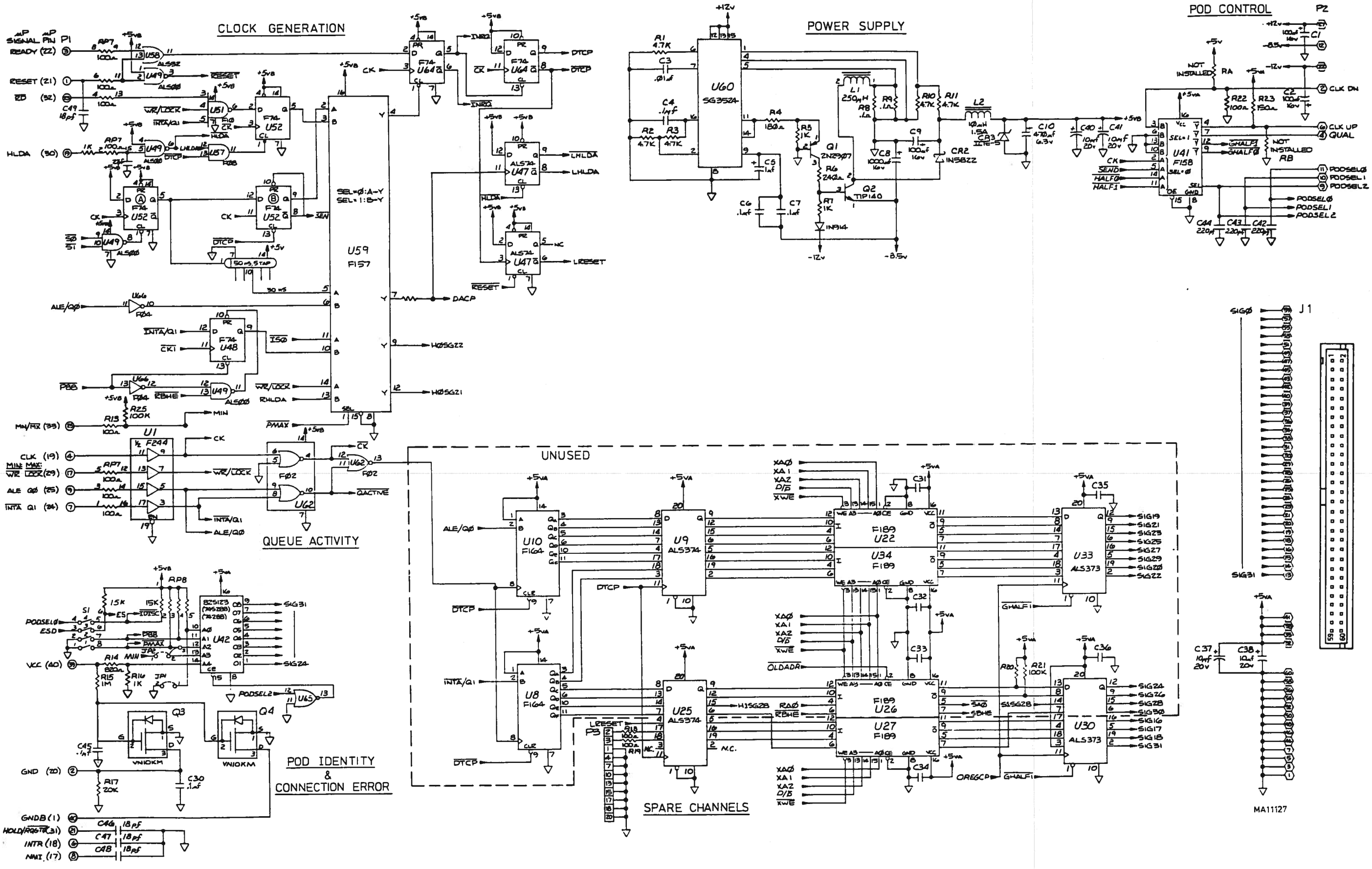


figure 3.31: 8086/8088 clock generation and power supply.

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3.7 PARTS LIST, PODS.

This list contains all components which are not standard.

The p.c. boards for the pods are not available from Concern Service. When, however, you need a spare p.c. board for a particular pod, you have to order it via the commercial department.

POSITION NUMBER	DESCRIPTION	ORDERING CODE
STANDARD LOGIC POD		
Integrated circuts:		
U18	74LS244	5322 209 86017
U13	74LS132	5322 209 85201
U21	74LS175	5322 209 84999
U26,25	74F194	5322 209 82418
U22	74LS240	5322 209 85862
U29,33	74F244	5322 209 81128
U9,14,26	74F374	5322 209 81909
U30	uA747	5322 209 84781
U10,11,15-17	NE521	5322 209 14441
U19,20,23,24	NE521	5322 209 14441
U27,28,31,32	NE521	5322 209 14441
U3,4,7,8,12	NE522	5322 209 86462
VR1	LM320T-5	5322 209 82842
Semi conductors:		
CR3,7	1N914B	5322 130 31487
CR5,6	1N961B	5322 130 34786
Various:		
CA	CAP-6.8PF,NP0,500V	5322 122 32275
CB	CAP-27PF,NP0.500V	5322 122 32274
P1A	CONNECTOR 26 PIN	5322 265 51111
P1B	CONNECTOR 20 PIN	5322 265 51109
P2	CONNECTOR 60 PIN	5322 265 61059
RA	RES. NETW. 82K 8 pins	5322 111 90841
RA	RES. NETW. 82K 6 pins	5322 111 90839
RB	RES. NETW. 18K 10 pins	5322 111 90837
RB	RES. NETW. 18K 6 pins	5322 111 90838
RC	RES. NETW. 1K	5322 111 94144
RD	RES. NETW. 2K2	5322 111 90469
RF	RES. NETW. 330E	5322 111 90295
S1	SLIDE SWITCH	5322 277 10848

POSITION NUMBER	DESCRIPTION	ORDERING CODE
4 CHANNEL FAST POD		
Integrated circuits:		
U5	74LS37	4822 209 80916
U1	74LS132	5322 209 85201
U4	74LS175	5322 209 84999
U3	74LS240	5322 209 85862
U15	74F244	5322 209 81128
U2,U6	SG3524	5322 209 81508
U9,20	F100102	5322 209 82875
U7	F100124	5322 209 82876
U16	F100125	5322 209 82877
U8,19	F100131	5322 209 82878
U17,18	F100151	5322 209 82879
U11,U24	LM555CN	5322 209 85824
U13	LM1458N	5322 209 84488
U10,U12,U14	AD9685BH	5322 209 82841
U21,22,23	AD9685BH	5322 209 82841
Semi conductors:		
Q4	T1P31A	5322 130 42504
Q2	T1P32A	5322 130 44333
Q1	2N2222A	5322 130 44115
Q3	2N2907A	5322 130 40621
CR5	1N5400	4822 130 31624
CR3,CR4	1N5820	5322 130 54064
CR7	1N756A	5322 130 32315
CR6	1N757A	5322 130 30682
CR9	1N914B	5322 130 31487
CR8	1N753A	4822 130 34167
CR1,CR2	1N4005	5322 130 34323
CR10,CR11	1N749A	5322 130 31837
CR12,CR13	1N750A	5322 130 34555
Various:		
L1	COIL	5322 158 10743
L2	COIl	5322 158 10744
DL1,2,5,6	DELAY LINE 6 nsec	5322 320 40128
DL3,4,7,8	DELAY LINE 2 nsec	5322 320 40127
K1, K2	RELAY	5322 280 80552
R15, R23	RESISTOR 0.1E 1 W	5322 113 31017
RL1 ... RL5	RES. NETW. 47E	5322 111 90846
RA	RES. NETW. 18K	5322 111 90854
RB	RES. NETW. 33K	5322 111 94071
RC	RES. NETW. 1K	5322 111 94176
RJ, RK	RES. NETW. 100E	5322 111 90786
RH	RES. NETW. 100E	5322 111 90787
R32	POTENTIOMETER 10K	5322 103 10269
S1	SLIDE SWITCH	5322 277 10848
J1	CONNECTOR 60 PIN	5322 265 61059

POSITION NUMBER	DESCRIPTION	ORDERING CODE

ROM EMULATOR POD

Integrated circuits:

U1	74LS00	5322 209 84823
U29	74LS02	5322 209 85407
U2P	74F02	5322 209 81535
U10	74F04	4822 209 80783
U6	74LS32	5322 209 85311
U7	74F139	5322 209 82234
U3	74LS157	5322 209 81521
U11	74LS166	5322 209 86292
U12,U24,U23	74LS244	5322 209 86017
U30	74F244	5322 209 81128
U19	74LS245	5322 209 86225
U26,U27	74F257	5322 209 81767
U2	74LS257	5322 209 86392
U9,U17,U18	74LS299	5322 209 86002
U13,U16	M58725P	5322 209 82855
U20-U23	M58725P	5322 209 82855
U4	74LS399	5322 209 82863

Semiconductors:

Q1...Q4	VN10KM	5322 130 42516

Various:

P1, P2	CONNECTOR 16 PIN	5322 265 40461
P3 ... P6	CONNECTOR 26 PIN	5322 265 51111
RP3, RP6	RES. NETW. 100E	5322 111 90851
RP1, RP2, RP5	RES. NETW. 470E	5322 111 94054
RP8	RES. NETW. 120E	5322 111 90849
RP11	RES. NETW. 180E	5322 111 90844
RP7	RES. NETW. 270E	5322 111 94157
RP10	RES. NETW. 820E	5322 111 90847
RP4	RES. NETW. 47K	5322 111 90853
RP9	RES. NETW. 220K	5322 111 90845

STANDARD BUS POD

Integrated circuits:

1C	74LS10	5322 209 84996
IE	74LS132	5322 209 85201
2B,2C,3C,3D	74LS244	5322 209 86017
2D	74LS374	5322 209 85869
1A,1D	74F00	5322 209 81534
2A	74F151	5322 209 81678

POSITION NUMBER	DESCRIPTION	ORDERING CODE
Integrated circuits (continued):		
3E	74F244	5322 209 81128
2E	74F373	5322 209 81533
1B	74HC00	4822 209 82377
3A,4A,4C	74HC244	5322 209 82861
3B,4B	74HC257	5322 209 82862
5C,5D	NE522	5322 209 86462
VR 1.	LM320T-5	5322 209 82842
Semiconductors:		
CR 6	1N914B	5322 130 31487
CR1-CR5,CR7	1N4005	5322 130 34323
Q1	VN10KM	5322 130 42516
Various:		
RP1 ... RP5	RES. NETW. 100K	5322 111 94202
RA,B,F,6A	RES.NETW. 270E	5322 111 90852
5E,6B,6C	RES. NETW. 1K	5322 111 90848
P2	CONNECTOR 60 PIN	5322 267 70161

Integrated circuits:		
U3	74F00	5322 209 81534
U9	74HC10	5322 209 82899
U2	74F32	5322 209 82133
U8	74LS139	5322 209 14876
U7	74F151	5322 209 81678
U12	74F240	5322 209 81127
U1,4,6,18,19	74LS244	5322 209 86017
U15,20	74HC244	5322 209 82861
U5,6,10,17	74HC257	5322 209 82862
U4	74LS279	5322 209 85346
U11	74F374	5322 209 81909
U13	74LS374	5322 209 85869
Semiconductors:		
CR1,2	1N9148	5322 130 31487
CR3,4	1N4005	5322 130 34323
Q1	VN10KM	5322 130 42516

POSITION NUMBER	DESCRIPTION	ORDERING CODE
Various:		
K1, K2	RELAY	5322 280 70267
RP2,4,5,7	RES. NETW. 270E	5322 111 90871
RP1,3,6,8	RES. NETW. 100K	5322 111 94227
RP9	RES. NETW. 3.3K	5322 111 90872
S1	4 POS. DIP SWITCH	5322 276 40351
P1	CONNECTOR 40 PIN	5322 267 70159
P2	CONNECTOR 60 PIN	5322 267 70161
P3	CONNECTOR 20 PIN	5322 267 51109

6800, 6809, 6502 MICROPROCESSOR PODS.

Integrated circuits:		
U2	74HC257	5322 209 82862
U1,9,13,16	74HC244	5322 209 82861
U4	74HC00	4822 209 82377
U8	74F151	5322 209 81678
U12	74F00	5322 209 81534
U3	74F373	5322 209 81533
U7,11	NE522	5322 209 86462
U6,10,14,17	74LS244	5322 209 86017
U5	uA747	5322 209 84781
VR1	LM320T-5	5322 209 82842
Semiconductors:		
CR1,2	1N914B	5322 130 31487
CR3	1N961B	5322 130 34786
CR4,5	1N4005	5322 130 34323
Q1	VN10KM	5322 130 42516
Various:		
S1	4 POS. DIP SWITCH	5322 276 40352
RN1,RN2	RES. NETW. 1K	5322 111 90848
RN3,RN4,RN5	RES. NETW. 4.7K	5322 111 90873
RN6	RES. NETW. 1K	5322 111 90848
K1	RELAY	5322 280 70267

Z80 MICROPROCESSOR POD

Integrated circuits:		
U15	74HC240	5322 209 82888
U6,10	74F00	5322 209 81534
U17	74HC00	4822 209 82377

POSITION NUMBER	DESCRIPTION	ORDERING CODE
Integrated circuits (continued):		
U16	74F151	5322 209 81678
U2	74F244	5322 209 81128
U4,8,13	74LS244	5322 209 86017
U3,5,9,14	74HC244	5322 209 82861
U1	74F373	5322 209 81533
U7,11	NE522	5322 209 86462
U12	74LS240	5322 209 85862
U18	uA747	5322 209 84781
VR1	LM320LZ-5	5322 209 82884
Semicondoctors:		
CR3,4	1N914B	5322 130 31487
CR1,2	1N4005	5322 130 34323
Q1	VN10KM	5322 130 42516
CR5	1N9618	5322 130 34786
Various:		
RP9	RES. NETW. 1K	5322 111 90848
RP1,RP4	RES. NETW. 270E	5322 111 90852
RP5,6,7,8	RES. NETW. 100K	5322 111 94202
RP2,RP3	RES. NETW. 4.7K	5322 111 90873
RP11,RP12	RES. NETW. 1K	5322 111 94152
RP10	RES. NETW. 2K	5322 111 90468
P1	CONNECTOR 40 PIN	5322 267 70159
P2	CONNECTOR 60 PIN	5322 267 70161
P3	CONNECTOR 20 PIN	5322 265 51109

NSC800 MICROPROCESSOR POD

Integrated circuits:		
U1, U2, U5, U7	74HC244	5322 209 82861
U15	74LS244	5322 209 86017
U3, U6	74LS374	5322 209 85869
U8, U9	74LS257	5322 209 86392
U16	74F373	5322 209 81533
U12	74HC20	5322 209 83206
U13	74LS74	5322 209 80782
U4	74HC00	5322 209 82377
U10	74LS32	5322 209 85311
U17	74F02	5322 209 81535
U14	74F151	5322 209 81678
U11	74LS04	4822 209 80783

POSITION NUMBER	DESCRIPTION	ORDERING CODE
Semiconductors:		
Q1	MOSFET VN10KM	5322 130 42516
CR3, CR4	DIODE 1N914	5322 130 31487
CR5	DIODE 1N753A	5322 130 34167
CR1, CR2	DIODE 1N4005	5322 130 30799

68000/68010 MICROPROCESSOR POD

Integrated circuits:		
UD2...UD5,UE2...UE4	74ALS374	5322 209 81646
UF8,UF9,UG1,UG2,UG6	74ALS374	5322 209 81646
UC1,UH1,UH7	74ALS374	5322 209 81646
UH5	74ALS273	5322 209 85792
UG7,UF6,UF7,UJ4,UJ5,UH4	74HC257	5322 209 82862
UH6,UG5	74HC257	5322 209 82862
UF10	SG3524	5322 209 81508
UF5,UG4,UH3	74F283	5322 209 81588
UF4,UJ2	74F521	5322 209 81543
UI1,UK5,UK7,UJ9	74F74	5322 209 81474
UK2	74F00	5322 209 81534
UJ1	74F04	5322 209 81577
UK10	74F174	5322 209 83326
UK1,UK6,UH8	74F32	5322 209 82133
UC6	LM1458N	5322 209 84488
UG9,UH9	74F399	5322 209 82852
UH2	74F374	5322 209 81909
UL10,UG3	74LS244	5322 209 86017
UJ8	74F08	5322 209 81574
UK3,UL1	74F10	5322 209 81681
UJ3	74F283	5322 209 81588
UG8	74F161	5322 209 82001
UA2	74ALS257	5322 209 81638
UK4	150 NSEC DELAY LINE	5322 320 40129
Semicondoctors:		
CR2	1N5822	5322 130 32677
CR1,CR4	1N914	5322 130 31487
CR3	TRANSORB. 5V 1.5KW	5322 130 34762
Q1	2N2907A	5322 130 40621
Q2	TIP120	5322 130 44529
Q3	VN10KM	5322 130 42516

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4. OPTIONS. CIRCUIT DESCRIPTION

4.1 GENERAL

This chapter describes all the options which are available for the PM 3632 logic analyzer.

A block diagram for the options is not enclosed. Figure 1.2, however, shows how the option boards are connected to the PM 3632 microprocessor bus.

A separate description of the setup memory (PM 8880/40) is not enclosed, because this option is a part of the setup data memory (PM 8880/50) and will be described there.

NOTE:

The setup and the setup data memory options can not be used together in one mainframe.

The PM 3632 has three options slots which can contain any combination of option cards.

These circuit desciptions contain no unit drawings. All component numbers are printed on the p.c. board which makes them self-explanatory.

In all circuit descriptions, a * behind a signal name indicates that it is low active. In the diagrams, the corresponding signal name has a bar above it.

4.2 DISA ROM BOARD [see figure 4.1]

This option board is used for disassembly of the microprocessor instructions, and can be plugged-in at any of the eight available positions.
The disa ROM can be a 2732, 2764 or a 27128.

Connector P1 connects the ROM disa board to the address, data and control busses ofg the microprocessor on the capture board.
Data and address lines are first buffered (U15, U16) before they are applied to the disassembler PROMs (U1...U8). The lower address lines are also latched in U11 (by means of the ALE pulse). The data bus on the option board is disconnected from the microprocessor databus when the option board is not selected (signal OPSEL via U17).

The option board is selected via signal OPSEL which is one of the three option select lines (OPSEL0....OPSEL2) that come from the microprocessor (U15, see figure 2.7). Because the option board can be in any of the three slots, the select signal is just called OPSEL. At power-up, the uP first reads the identity of the option boards in the slots (by reading buffer U10) and then knows which of the three OPSEL0...OPSEL2 lines it has to active to access the disa Rom board.
At power-up it also reads which disassembler PROMs are installed, and in which socket they are.

Decoder U18 is enabled only when the option board is selected (signal OPSEL) and when address line A15 is high (addresses 8000 and up; see also memory map figure 2.5). This decoder selects either the scratch pad RAM (U9, signal RAMEN*), the 'identity buffer ' (U10) or the bankselect register (U13, signal SELREG*).
This bank select register (U13) decodes the databus to select one of the 8 disa PROMs (via U12). The microprocessor can read the selected PROM back via register U14 (used at power-up, for reading the position of the PROMs).

LIST OF SIGNAL NAMES (diagram 21)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
6.2016 MHz	Video and uP clock	3	21
A 8	Addressline 8	2	21
A 9	Addressline 9	2	21
A10	Addressline 10	2	21
A11	Addressline 11	2	21
A12	Addressline 12	2	21
A13	Addressline 13	2	21
A14	Addressline 14	2	21
A15	Addressline 15	2	21
AD0	Address/data line 0	2	21
AD1	Address/data line 1	2	21
AD14*	Address/data line 14	21	21
AD15*	Address/data line 15	21	21
AD2	Address/data line 2	2	21
AD3	Address/data line 3	2	21
AD4	Address/data line 4	2	21
AD5	Address/data line 5	2	21
AD6	Address/data line 6	2	21
AD7	Address/data line 7	2	21
ALE	Address latch enable	2	21
BRD*	Buffered read signal	21	21
BRDSEL*	Board selection signal	21	21
BWR*	Buffered write signal	21	21
IO/M*	Input,output/ memory	2	21
OPINT*	Option interrupt	21	1,2,6
OPSEL*	Option select; slot 0,1 or 2	3	21
RAMEN*	Enable scratch pad ram	21	21
RD*	Read signal	2	21
READY	Ready	21	1,2,6
RESET OUT	Reset out signal	2	21
ROM0*	Select disa rom 0	21	21
ROM1*	Select disa rom 1	21	21
ROM2*	Select disa rom 2	21	21
ROM3*	Select disa rom 3	21	21
ROM4*	Select disa rom 4	21	21
ROM5*	Select disa rom 5	21	21
ROM6*	Select disa rom 6	21	21
ROM7*	Select disa rom 7	21	21
S0	Status line 0	2	21
S1	Status line 1	2	21
SELREG*	Select bank switch register	21	21
WR*	Write signal	2	21

Figure 4.1 : Disa ROM board (21)

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4.3 RS 232C CONTROL CARD.

This option board is used for uploading or downloading of data (in data memory option, setup memory option or Rom emulator pod) to or from any device which can communicate via an RS 232C link (in hex format).
This board is also used to control the Rom emulator pod via another serial link (not an RS 232C link).
The option board can be plugged-in at any option slot at the capture board, but the most left slot is preferred (J3).

Connector P1 connects the RS 232C control card to the address, data and control busses of the microprocessor on the capture board.
Data lines are first buffered via U15 and are only connected to the microprocessor databus when this option board is selected (signal OPSEL, via U10). The lower address lines are latched in U11 (by meansof the ALE pulse). The upper address lines are directly applied to PROM U6.

The option board is selected via signal OPSEL which is one of the three option select lines (OPSEL0....OPSEL2) that come from the microprocessor (U15, see figure 2.7). Because the option board can be in any of the three slots, the select signal is just called OPSEL. The microprocessor first reads the identity of the option boards in the slots (by reading buffer U2) and then knows which of the three OPSEL0...OPSEL2 lines it has to activate to access RS 232C control card.

Decoder U5 is only enabled when the option board is selected (OPSEL), and when address line A15 is high (addresses 8000 and up; see also figure 2.5, memory map). This decoder either selects PROM U6 (via ROMEN*, memory mapped), scratch pod RAM U7 (via RAMEN*, memory mapped), UART U12 (via UARTEN*, I/O mapped) or the 'identity buffer' U2 (via TYPEN*,I/O mapped).

The control software for the RS 232 control card is located on the option board itself (U6). This software controls the RS 232C connection (via UART U12) and the serial link for the ROM emulator pod (via 8155 U7).

RS 232C control:
The RS 232C connection is only a three wire connection: TXD, RXD and DSR.
The RS 232C connection is controlled via UART U12 which is loaded with the correct control data by the microprocessor, before it starts receiving or transmitting data via RXD and TXD lines.
The UART interrupts the microprocessor when it needs to fill the transmitter buffer when it is empty (via signal TXEMPTY) or when the uP needs to empty the receiver buffer when it is full (via signal RXRDY).
These signals interrupt the microprocessor via the INT* input via U9, U10 and U14. The interrupt is enabled by the micrprocessor only when it has activated this board (signal INTEN* via 8155 U7).
The interrupt for the transmitter buffer is only enabled when the RS 232C control card is in transmitter mode (signal TXIDIS*; loaded by software in control register of UART).
The clock for the UART is derived from the microprocessor clock (6.2016 MHz for instruments connected to a 50 Hz mains) via clock divider U1 (approx. 3.2 MHz). The baudrate clock is derived via the timer portion of U7 (freq.= 16 times the selected baudrate). This timer is loaded immediately after starting data transfer.

ROM emulator pod control:

The Rom emulator pod is controlled via a serial link which is under control of the microprocessor.
Buffer U13 transfers control signals (CTL0, CTL1) and pod select signals (SEL0, SEL1) to the ROM emulator pod. These signals are generated via the upper half of port A in U12.
Buffer U13 also transfers the clock signal (RCLK) -for the inputbuffers in the pod-, and the serial data that goes to the pod or comes from the pod (DDWN and SELDAT respectively).
The data that has to be downloaded or uploaded to or from the ROM emulator pod is loaded into shift register U3 via port B of U7.
A high signal LOAD loads data from the microprocessor into the shift register (U3) on the next clock pulse (on pin 12). The data is then shifted out to the pod (DDWN) on the next 8 clock pulses (LOAD is low).
A low signal LOAD permits the pod to shift data (DUP) into the shift register and then the microprocessor can read this data.

The clock signal (RCLK) for the pod and shift register is derived from the microprocessor clock via clock divider U1 (URTCK).
For loading one byte of information into the pod, 8 clock pulses are needed to fill the input shift registers in the pod (clocksignal RCLK).
For this, the uP resets U4 (via lower part of port A) when a data byte is ready in U3 or when a next data byte can be read from trhe pod.
U4 then counts 8 clock pulses and stops itself via the terminal count output.
For the next byte, the counter has to be reset again.
For loading one byte of data into U3 (via port B of U7) counter U4 is first loaded with 1110 (via lower part of port A, pin 22) and then counts 1 clock pulse before it stops itself via the terminal count output. This clock pulse loads data from port B into shift register U3.

LIST OF SIGNAL NAMES (diagram 22)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
6.2016 MHz	Video and uP clock	3	22
A 8	Address line 8	2	22
A 9	Address line 9	2	22
A10	Address line 10	2	22
A11	Address line 11	2	22
A12	Address line 12	2	22
A13	Address line 13	2	22
A14	Address line 14	2	22
A15	Address line 15	2	22
A15*	Address line 15	22	22
AD0	Address/data line 0	2	22
AD1	Address/data line 1	2	22
AD2	Address/data line 2	2	22
AD3	Address/data line 3	2	22
AD4	Address/data line 4	2	22
AD5	Address/data line 5	2	22
AD6	Address/data line 6	2	22
AD7	Address/data line 7	2	22
ALE	Address latch enable	2	22
BRD*	Buffered dear signal	22	22
BSELOAT	Buffered serial data up	14	22
CTL0	Control line 0	22	14
CTL1	Control line 1	22	14
DDWN	Data down (to Rom emulator)	22	14,22
DUP	Data up (from rom emulator)	22	22
ECLK	Rom emulator clock	22	14
INT	Interrupt signal	22	22
INTEN*	Interrupt enable	22	22
IO/M*	Input,output/ memory	2	22
LOAD	Load data	22	22
OPINT*	Option interrupt	22	1,2,6
OPSEL*	Option select line	3	22
RAMEN*	Enable scratch pad ram	22	22
RD*	Read signal	2	22
READY	Ready	22	1,2,6
RESET OUT	Reset out signal	2	22
ROMEN*	Enable control rom	22	22
RXRDY	Receiver register ready	22	22
S0	Status line 0	2	22
S1	Status line 1	2	22
SEL0	Select line 0	22	14
SEL1	Select line 1	22	14
TXEMPTY	Transmitter register empty	22	22
TXIDIS*	Enable transmitter interrupt	22	22
TYPEN*	Enable buffer for id read	22	22
UARTEN*	Enable uart	22	22
URTCK	Uart clock	22	22
WR*	Write signal	2	22

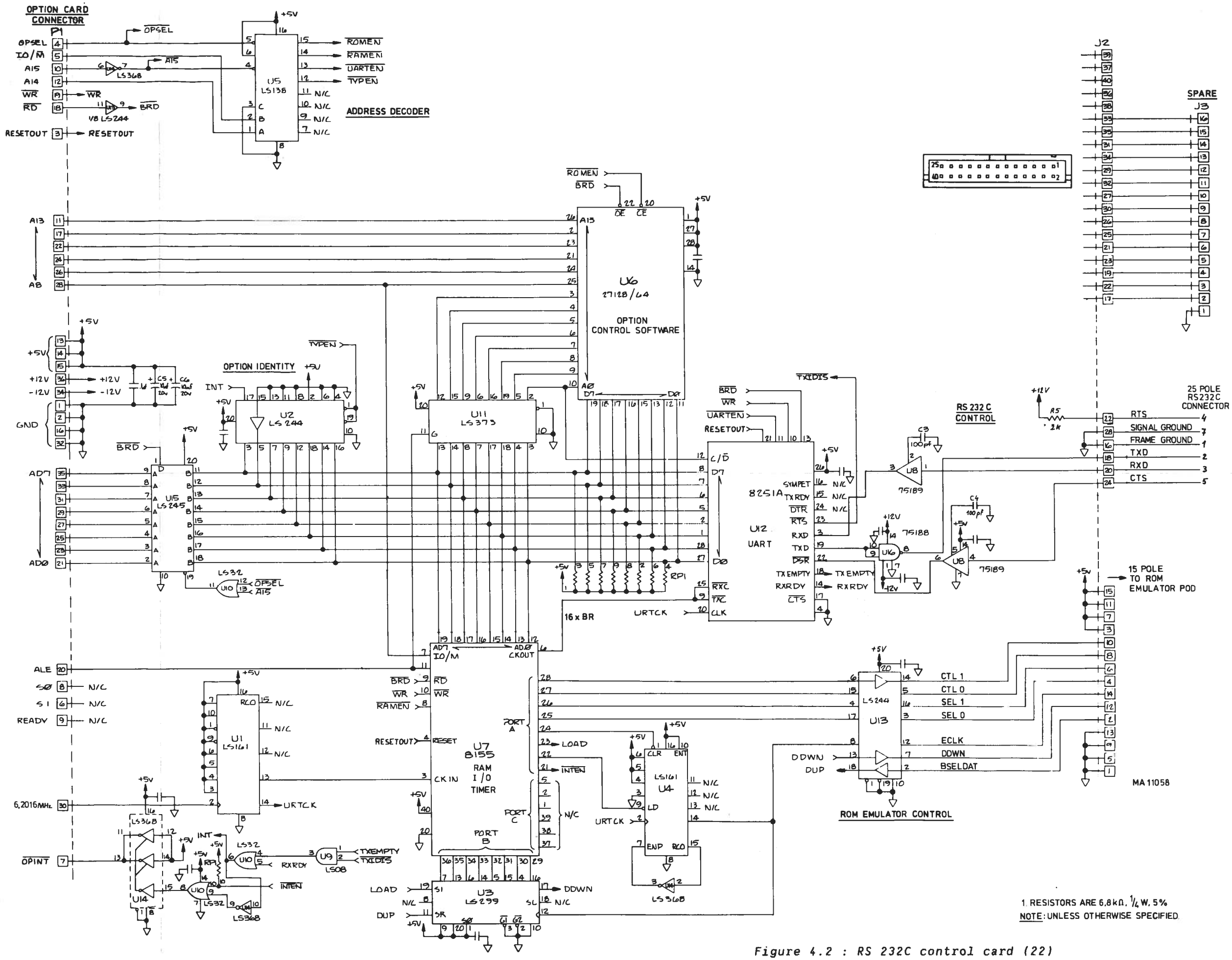


Figure 4.2 : RS 232C control card (22)

4.4 SETUP DATA MEMORY [see figures 4.3 and 4.4]

This option is used to store up to 8 different settings and up to 8K of data into non volatile memory.
Also compare, search and autosequence modes are possible when this board is installed.

NOTE:

This description also covers the setup memory option which is a part of the setup data memory option.
The difference between these options is that the setup data memory has:

- *4 extra EEPROMs (U3, U4, U5 and U6)*
- *1 extra RAM (U2)*
- *different control software (U1)*

Connector P1 connects the setup data memory option to the address, data and control busses of the microprocessor on the capture board (see figure 4.3).
Data and addresslines are first buffered via U16, U17.
The data lines of this option board are only connected to the databus of the microprocessor when this board is selected (signal BRDSEL*).
The lower addresslines are latched in U12 (by means of the ALE pulse).

The option board is selected via signal OPSEL which is one of the three option select lines (OPSEL0....OPSEL2) that come from the microprocessor (U15, see figure 2.7). Because the option board can be in any of the three slots, the select signal is just called OPSEL.
The microprocessor first reads the identity of the option boards in the slots (by reading buffer U11) and then knows which of the three OPSEL0....OPSEL2 lines it has to activate to access the setup data memory option.

Decoder U19 is enabled only when the option board is selected (signal OPSEL) and when address line A15 is high (addresses 8000 and up; see also figure 2.5, memory map).
This decoder selects (8 K blocks)

- bank switch register : U13, by means of signal SELREG* : I/O mapped.
- "identity buffer" : U11, by means of signal BRDTYPE*: I/O mapped.
- PROM U1 : U1, by means of signal ROM* :memory mapped.
- reference RAM : U2, by means of signal RAM1* :memory mapped.
- one extra 8K block

The extra 8 K block is further decoded by U14 (2 K blocks) which selects:

- -EEPROMS1...5 : U3, U4, U5, U6 or U7, by means of signals EEPROM1*...EEPROM5*: memory mapped
- -scratch pad RAM : U8, by means of signal RAM2 : memory mapped.

Bank select buffer U13 is used to select the different EEPROMs which are located on the same memory location (signal BANK, from U13 to U14).
When BANK = 0 : then EEPROMs U3, U4 and U7 are selected.
When BANK = 1 : then EEPROMs U5, U6 and U7 are selected.
Signal RA14 is used as bank select signal for the PROM that contains the control software (U1). This select signal is only used to switch-off PROM U1 in case it is a 27256 and the EEPROMs have to be selected. Until now this PROM has been a 27128 so this select signal is not yet used.

Via buffer U15, the microprocessor can read the status of the bankselection, the kind of EEPROMs that is used and also the RDY/BUSY* line of the EEPROMs when the INTEL PROMs are used.
In case of INTEL EEPROMs the microprocessor reads RDY/BUSY*. When it is high, the microprocessor can write new data to the PROMs.

The EEPROM can either be INTEL or XICOR PROMs. To select this, jumper W1 can be closed or opened, however only XICOR PROMs are used.
The EEPROMs have a power-down protection. This circuit, consisting of U9, Q1 and associated components, keeps the write line (BWR*) high when the power goes down from 4.5 V to 3.0 V. If the write line is not stable during this interval, it will overwrite the information in the EEPROMs.

LIST OF SIGNAL NAMES (diagram 23)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
6.2016 MHz	Video and uP clock	3	23
A 8	Addressline 8	2	23
A 9	Addressline 9	2	23
A10	Addressline 10	2	23
A11	Addressline 11	2	23
A12	Addressline 12	2	23
A13	Addressline 13	2	23
A14	Addressline 14	2	23
A15	Addressline 15	2	23
AD0	Address/data line 0	2	23
AD1	Address/data line 1	2	23
AD2	Address/data line 2	2	23
AD3	Address/data line 3	2	23
AD4	Address/data line 4	2	23
AD5	Address/data line 5	2	23
AD6	Address/data line 6	2	23
AD7	Address/data line 7	2	23
ALE	Address latch enable	2	23
ASD0	Address line 0	23	24
ASD1	Address line 1	23	24
ASD2	Address line 2	23	24
ASD3	Address line 3	23	24
ASD4	Address line 4	23	24
ASD5	Address line 5	23	24
ASD6	Address line 6	23	24
ASD7	Address line 7	23	24
BA 8	Buffered address line 8	23	24
BA 9	Buffered address line 9	23	24
BA10	Buffered address line 10	23	24
BAD0	Buffered address/data line 0	23	24
BAD1	Buffered address/data line 1	23	24
BAD2	Buffered address/data line 2	23	24
BAD3	Buffered address/data line 3	23	24
BAD4	Buffered address/data line 4	23	24
BAD5	Buffered address/data line 5	23	24
BAD6	Buffered address/data line 6	23	24
BAD7	Buffered address/data line 7	23	24
BANK	Bank select	23	23
BRD*	Buffered read signal	23	23
BROSEL*	Board selection	23	23
BROTYPE*	Enable id buffer	23	23
BWR*	Buffered write signal	23	23,24
EEPROM1*	Enable EEPROM 1	23	24
EEPROM2*	Enable EEPROM 2	23	24
EEPROM3*	Enable EEPROM 3	23	24
EEPROM4*	Enable EEPROM 4	23	24
EEPROM5*	Enable EEPROM 5	23	24

LIST OF SIGNAL NAMES (diagram 23, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
IO*/M	Input/output/memory	23	24
IO/M*	Input,output/ memory	2	23
OPINT*	Option interrupt	23	1,2,6
OPSEL*	Option select; slot 0,1 or 2	3	23
RA14	Address line 14	23	23
RAM1*	Enable reference ram	23	23
RAM2*	Enable scratch pad ram	23	23
RD*	Read signal	2	23
RDY/BUSY*	Ready/Busy signal	23	24
READY	Ready	23	1,2,6
RESET OUT	Reset out signal	2	23
ROM*	Enable control rom	23	23
S0	Status line 0	2	23
S1	Status line 1	2	23
SELREG*	Select bank switch register	23	23
WR*	Write signal	2	23

LIST OF SIGNAL NAMES (diagram 24)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
ASD0	Address line 0, setup/data	23	24
ASD1	Address line 1, setup/data	23	24
ASD2	Address line 2, setup/data	23	24
ASD3	Address line 3, setup/data	23	24
ASD4	Address line 4, setup/data	23	24
ASD5	Address line 5, setup/data	23	24
ASD6	Address line 6, setup/data	23	24
ASD7	Address line 7, setup/data	23	24
BA 8	Buffered address line 8 setup	23	24
BA 9	Buffered address line 9 setup	23	24
BA10	Buffered address line 10 setup	23	24
BAD0	Buffered address/data line 0 setup	23	24
BAD1	Buffered address/data line 1 setup	23	24
BAD2	Buffered address/data line 2 setup	23	24
BAD3	Buffered address/data line 3 setup	23	24
BAD4	Buffered address/data line 4 setup	23	24
BAD5	Buffered address/data line 5 setup	23	24
BAD6	Buffered address/data line 6 setup	23	24
BAD7	Buffered address/data line 7 setup	23	24
BWR*	Buffered write signal, setup/data	23	24
EEPROM1*	Enable EEPROM1	23	24
EEPROM2*	Enable EEPROM2	23	24
EEPROM3*	Enable EEPROM3	23	24
EEPROM4*	Enable EEPROM4	23	24
EEPROM5*	Enable EEPROM5	23	24
RDY/BUSY*	Ready/Busy signal, setup/data	23	24

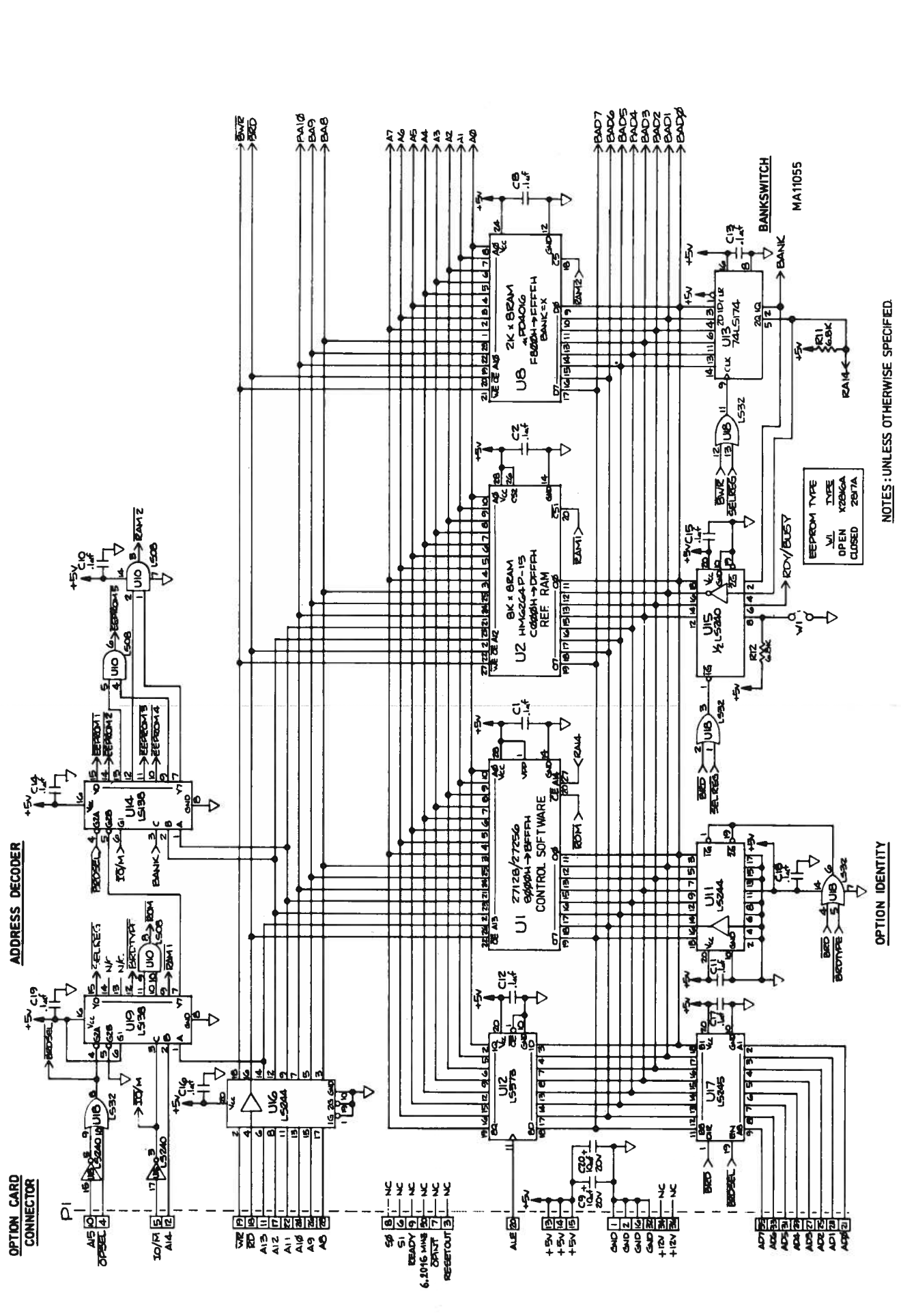


Figure 4.3 : Setup data memory (23)

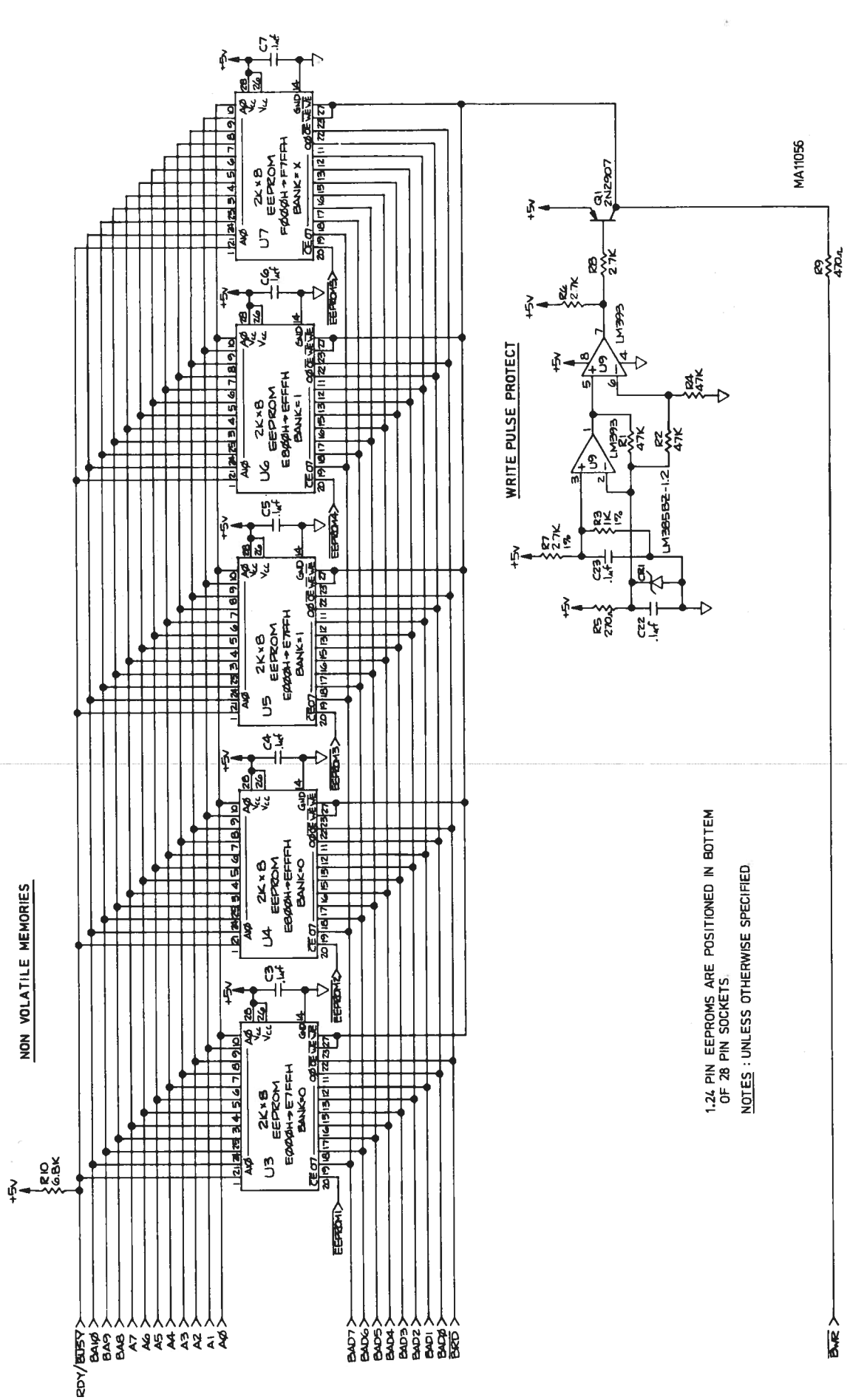


Figure 4.4 : Setup data memory; EFPROMs (24)

4.5 COMPOSITE VIDEO OUTPUT (see figure 4.5)

This option is used to generate a composite video signal which can be used to connect an external monitor, or for example a video printer.

The video output **MUST** be installed in the service workshop, and is certainly not user installable (see section 7.3 for installation instructions).

The video interface combines the following signals into one composite video signal:

VRTC	(Vertical retrace)
HRTC	(Horizontal retrace)
VIDEO	(Video signal from microcomputer-video interfavce)

The output signal is a composite video signal which can be used on 50 Hz monitors, or for example on a video printer.

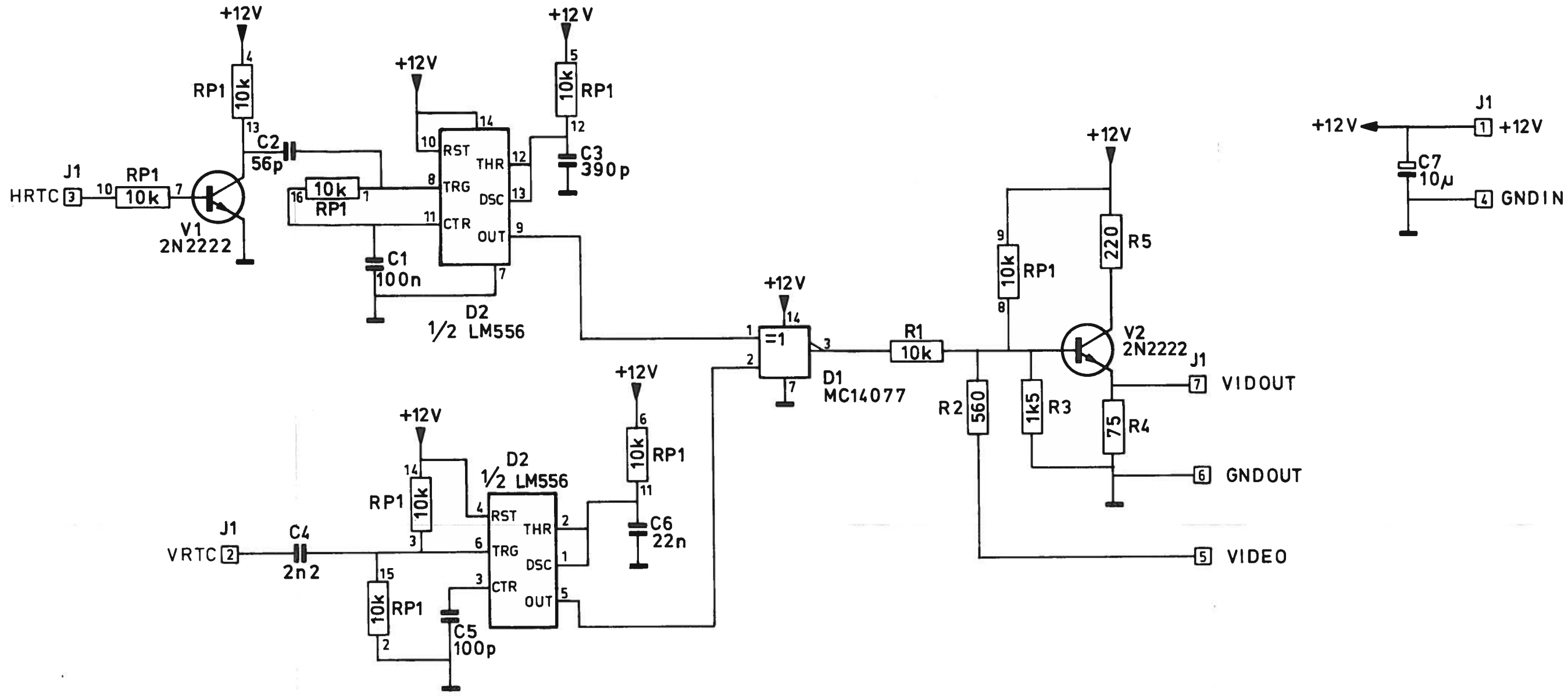
The vertical and horizontal retrace signals, both pass a one-shot (U2), before they are combined into one synchronisation signal (in U1).
The video signal, generated by the video interface of the microcomputer, is added to the synchronisation signal in the output stage (Q2).
After the output stage, there is a composite video signal available.
This output stage has a 75 ohm output impedance.

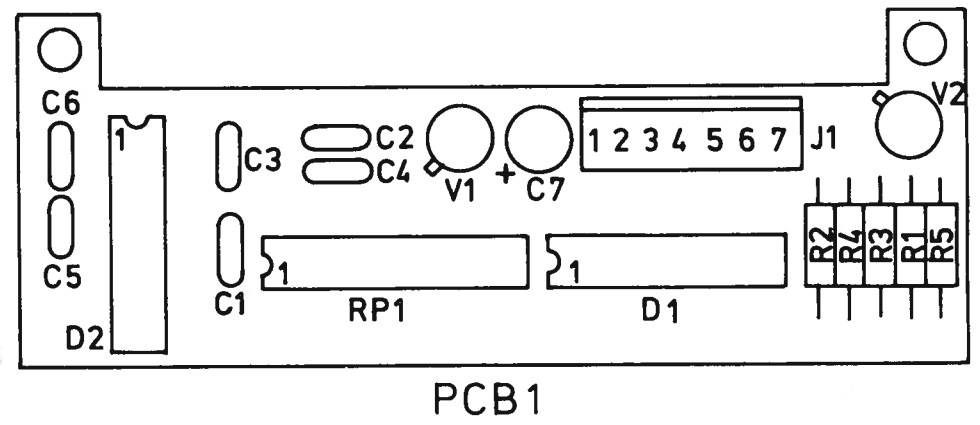
NOTE: U2 (LM556) is a selected part. Only tested parts can be used!!

LIST OF SIGNAL NAMES (diagram 31)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
HRTC	Horizontal retrace	2	31
VRTC	Vertical retrace	2	31
VIDEO	Video signal	2	31
VIDOUT	Composite video out	31	BNC plug
GNDOUT	Ground signal out	31	BNC plug





MA11176

Figure 4.5 : Video output (31)

4.5 SPARE PARTS, OPTIONS

This list contains all components which are not standard.

The p.c. boards for the options are not available from Concern Service. When, however, you need a spare p.c. board for a particular option, you can order it via the commercial department.

Proms with option software are also not available from Concern Service. When you want to order option software, contact the DTE Supply Centre Service group.

NEDERLANDSE PHILIPS BEDRIJVEN B.V.
MIG S&I, T&M SERVICE DEPARTMENT DTE
BUILDING TQ V-2
EINDHOVEN

POSITION	DESCRIPTION	ORDERING CODE
DISA ROM BOARD		
Integrated circuits:		
U17	74LS32	5322 209 85311
U12,18	74LS138	5322 209 85647
U14	74LS240	5322 209 85862
U10,15	74LS244	5322 209 86017
U16	74LS245	5322 209 86225
U13	74F379	5322 209 82887
U9	M58725P	5322 209 82855
U11	74LS373	5322 209 86062
Various:		
RP1	RES. NETW. 6.8K	5322 111 90834
RS 232C CONTROL CARD		
Integrated circuits:		
U10	74LS32	5322 209 85311
U5	74LS138	5322 209 85647
U1,4	74LS161	5322 209 85915
U2,13	74LS244	5322 209 86017
U15	74LS245	5322 209 86225
U3	74LS299	5322 209 86002
U14	74LS368	4822 209 80448
U11	74LS373	5322 209 86062

POSITION	DESCRIPTION	ORDERING CODE
Integrated circuits (continued):		
U7	8155	5322 209 14563
U12	P8251A	5322 209 14866
U16	75188	5322 209 84307
U8	75189	5322 209 86103
Various:		
RP1	RES. NETW. 6.8K	5322 111 90834
J2	CONNECTOR 40 PIN	5322 267 70158
J3	CONNECTOR 20 PIN	5322 267 70158

SETUP DATA MEMORY

Integrated circuits:		
U2	HM6264P-12	5322 209 82897
U8	M58725P	5322 209 82855
U9	LM393	4822 209 80797
U10	74LS08	5322 209 84995
U11,16	74LS244	5322 209 86017
U12	74LS373	5322 209 86062
U13	74LS174	4822 209 81821
U14,19	74LS138	5322 209 85647
U15	74LS240	5322 209 85862
U17	74LS245	5322 209 86225
U18	74LS32	5322 209 85311
U3...U7	X2816AP	5322 209 82885
Semiconductors:		
CR1	LM385BZ-1.2	5322 130 32688
Q1	2N2907A	5322 130 40621

VIDEO OUTPUT

Integrated circuits:		
U1	HEF4077BP	4822 209 10223
Semiconductors:		
Q1,2	2N2222	5322 130 40221

NOTES:

NOTES:

5. TROUBLESHOOTING

5.1 GENERAL

This chapter describes how to proceed when there is a fault in the PM 3632 or its pods or its options.
The tools that are available for troubleshooting, are:

1. This service manual, with circuit diagrams and descriptions
2. Faultfinding tree, which leads you via most possible symptoms to the circuit that you have to check.
3. Diagnostic software, which can be divided into two parts:
   - Diagnostics, standard in every instrument.
   - Optional diagnostics, available as a **diagnostic tools kit** (PM 8891).
4. Listing of initialisation program of PM3632, which helps finding faults in the microprocessor and associated circuits (section 5.5).

5.2 FAULTFINDING TREE

This tree is the first thing to follow when there is a fault in your instrument.
This faulfinding tree (see next page) leads you through most symptoms that can occur when there is something wrong with the PM 3632 or its options or pods.
Each symptom described:

- will end in a part of the tree that points to a particular circuit that has to be faulty. Via the index at the beginning of this manual, you will find the page number where to find the corresponding diagrams.
- or will end in a part of the tree that points to the diagnostic software which is contained in the PM 8891 (diagnostic tools kit for the PM 3632). The diagnostic tools kit is described in chapter 5.4.

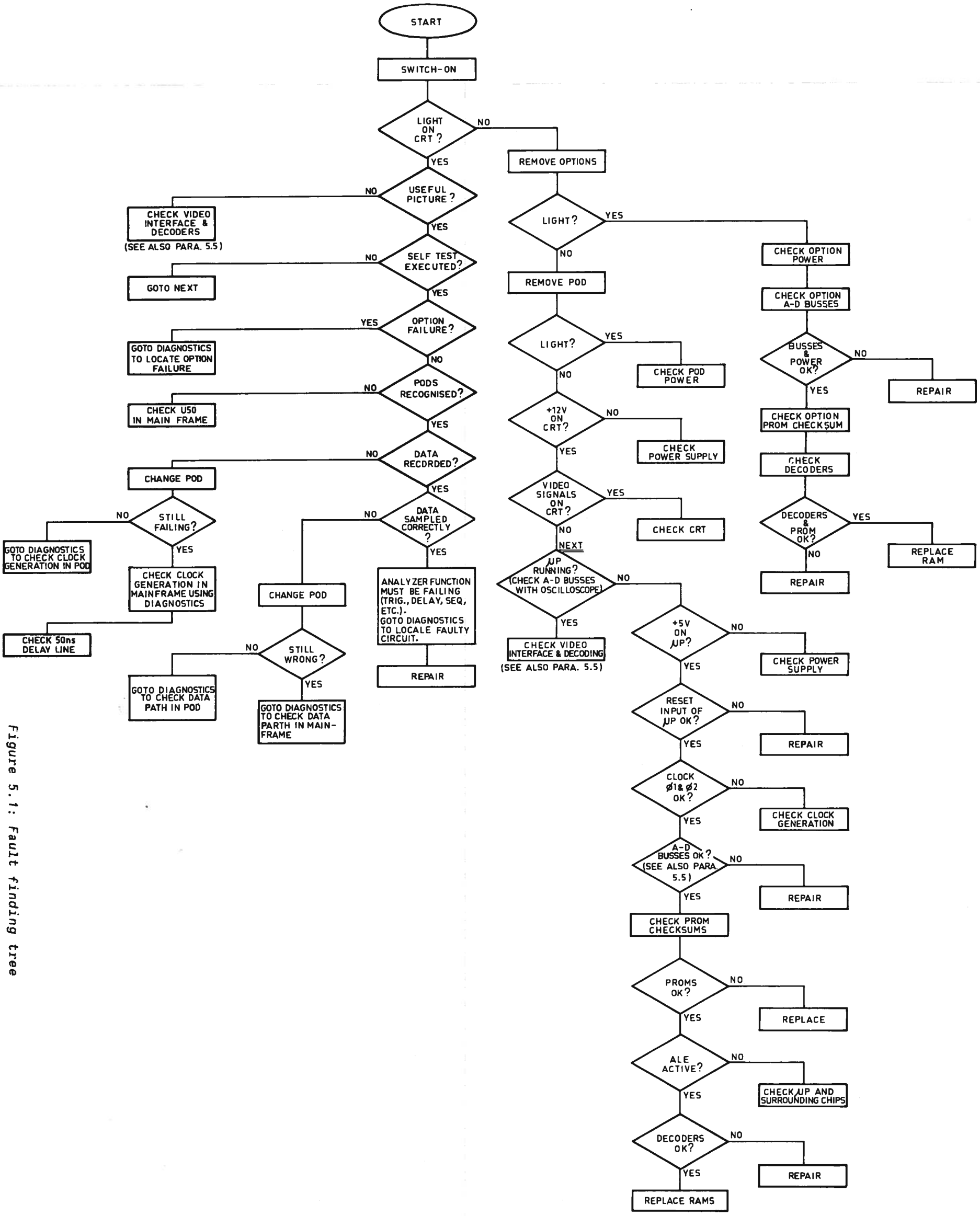


Figure 5.1: Fault finding tree

5.3 STANDARD DIAGNOSTICS

The diagnostic software that is installed in every instrument, is performed always immediately after power-up.
It does the following tests in the shown sequence. When there is a failing function in the mainframe, it will display the test results and stay in that screen.

Rom checksum	:	pass/fail Calculates checksum of system software (U113 and U121) and compares it to the checksums stored in Prom.
Ram test	:	pass/fail AA55 test on the rams which are a part of U134, U135, U136, U15 and U16. Addressed and read via address/data bus.
TRACE test	:	pass/fail Clocks address counter of data acquisition memories until there is an overflow. Concerns parts U39, U40, U41 and U42 Clock pulses via "data storage clock generation".
Trace ram	:	pass/fail Address test for data acquisition rams. Concerns parts U1 ... U8. Addressed via addresse counter, read and write via U15 and U16 (TRCD0 ... TRCD31).
Trigger	:	pass/fail Address test for trigger rams. Concerns parts U9, U17, U25 and U33 Addresssed via U15 and U16 (TRRCD0 ... TRCD31), read and write via U135 (TRWA? ... TRWD?).
Sequence	:	pass/fail Address test for sequence controller rams. Concerns U124. Addressed via U135 (TRWA? ... TRWD?), and read and write via U135 (STATRAM0 ... STATRAM3).

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5.4 PM 8891, DIAGNOSTIC TOOLS KIT

The diagnostic tools kit is specially developed for repairing the PM 3632 in an easier way.
The PM 8891 contains (see figure 5.2):

- three EPROMs, containing diagnostic programs (27128).
- one disa rom board (PM8880/30).
- one 32 channel test board.
- one 8085/Z80 microprocessor target.
- one option extender card

5.4.1 Targets

Most tests in the diagnostic software require a target connected to the logic analyzer (via a pod). The two targets in the diagnostic tools kit are:

- **32 channel test board.**

This test board generates the following data patterns, depending on the setting of the dip-switches on the board:

dip-switches:

1	2	3	4			
down	up	up	up	=	walking zero	;requires an internal sampling clock of min 30 nsec.
up	down	up	up	=	walking one	;requires an internal sampling clock of min 30 nsec.
up	up	up	up	=	8 bit counter pattern	;on external clock.

The test board connects to the 32 channel logic pod inputs via connector P1A and P1B, while the outputs (flat cable) of the 32 channel logic pod are connected to P2. The connection from the 32 channel test board to the PM 3632 is made via the flat cable that fits into connector P3 (see figure 5.3)

The test board connects to the 4 channel fast pod inputs via connector P4, while the outputs of the 4 channel fast pod are connected to P2. The connection from the 32 channel test board to the PM 3632 is made via the flat cable that fits into connector P3.

Note: when being connected to the 4 channel fast pod, the test board also generates a walking zero/one, but since only the least significant four bits are used, it is not a real walking zero/one pattern!

Figure 5.4 shows the circuit diagram of the 32 channel test board.
A circuit description of this board is not included in this manual.

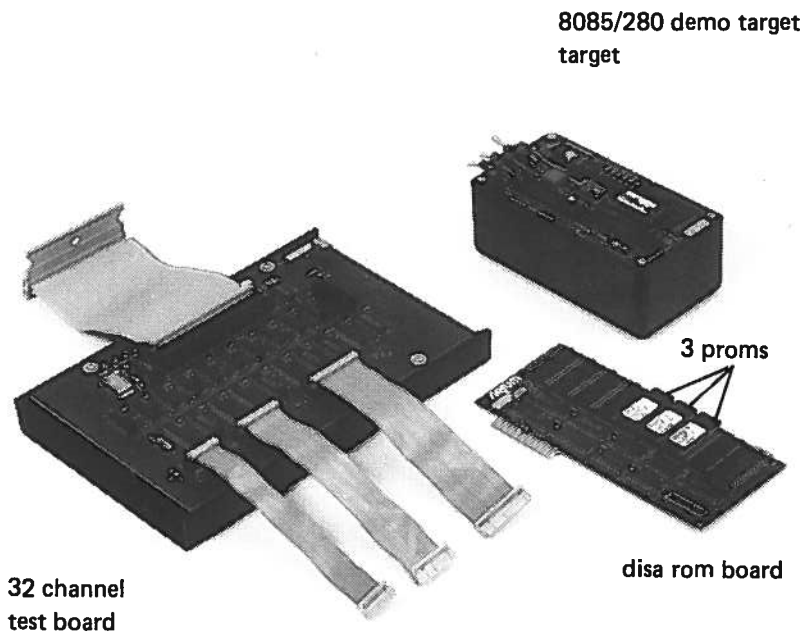


Figure 5.2: PM8891, Diagnostic tools kit for the PM3632.

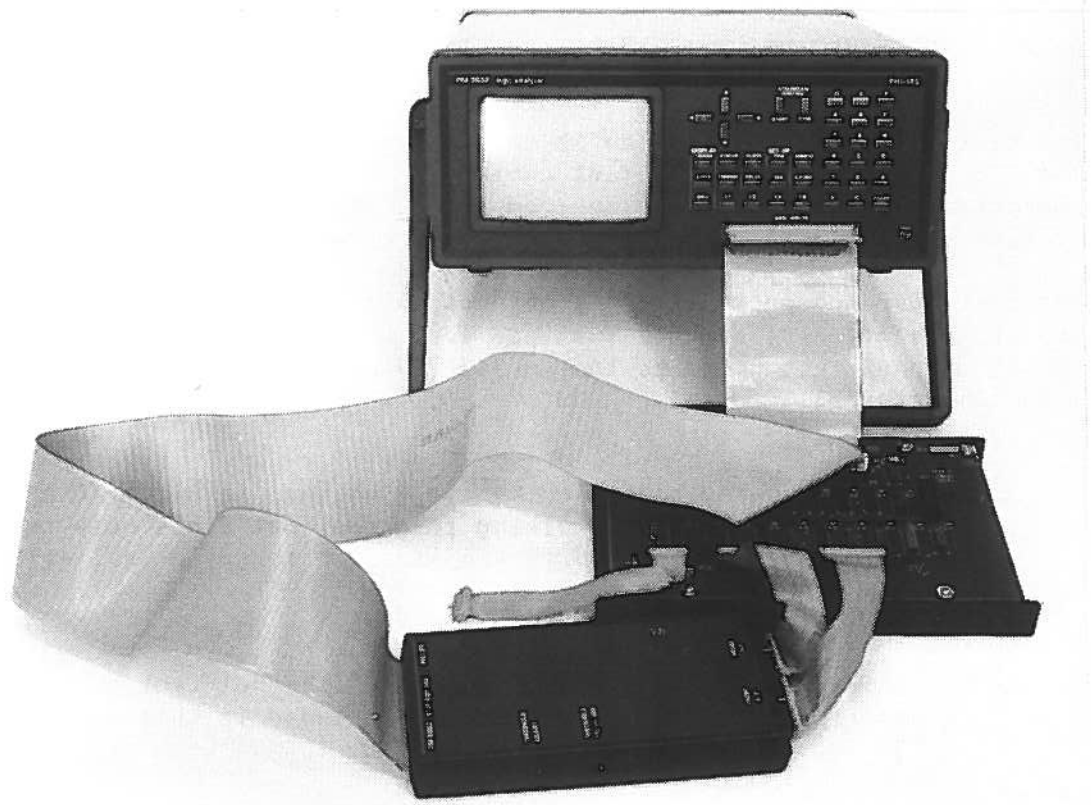


Figure 5.3: Connection of 32 channel test board.

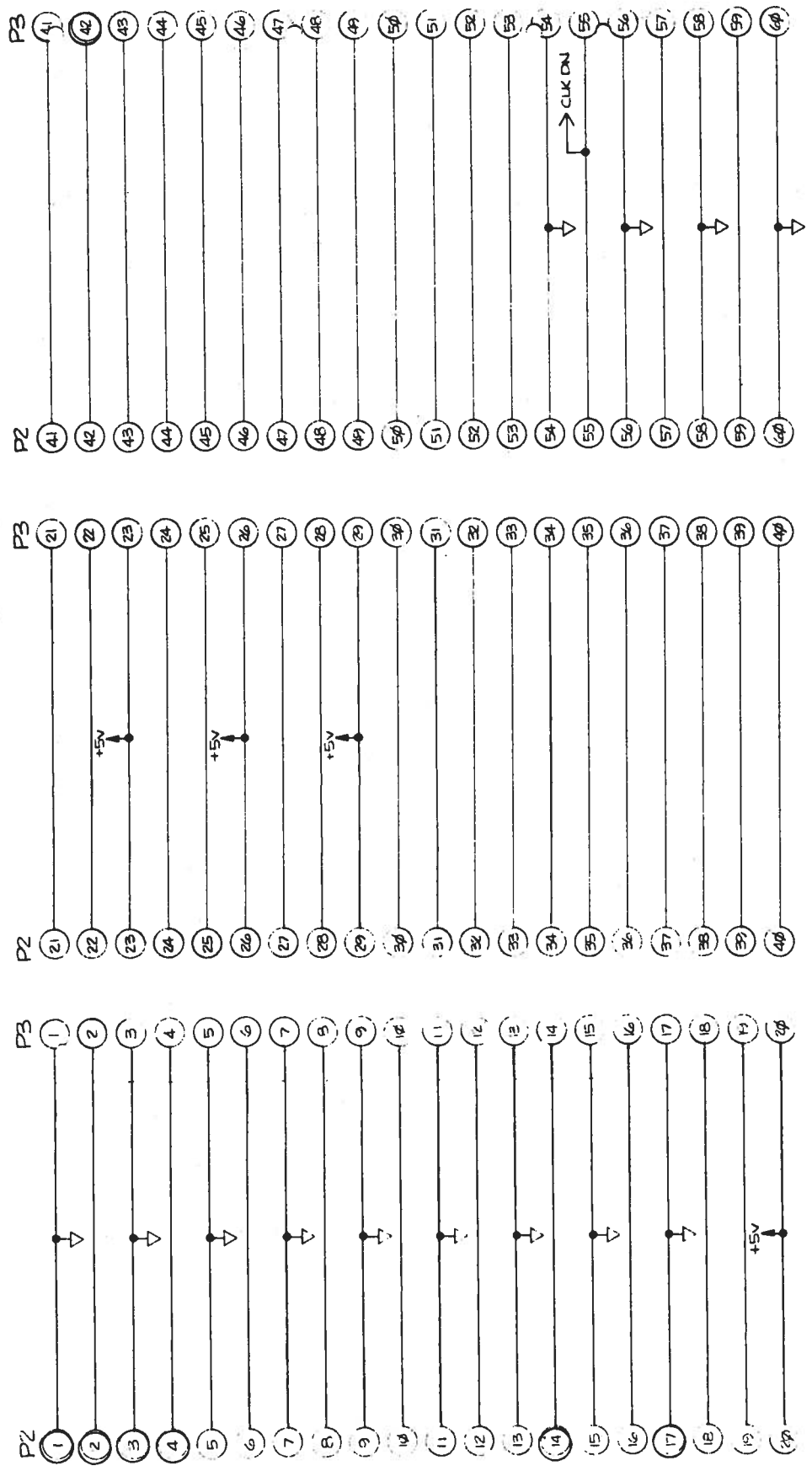


Figure 5.4: 32 channel test board, circuit diagram.

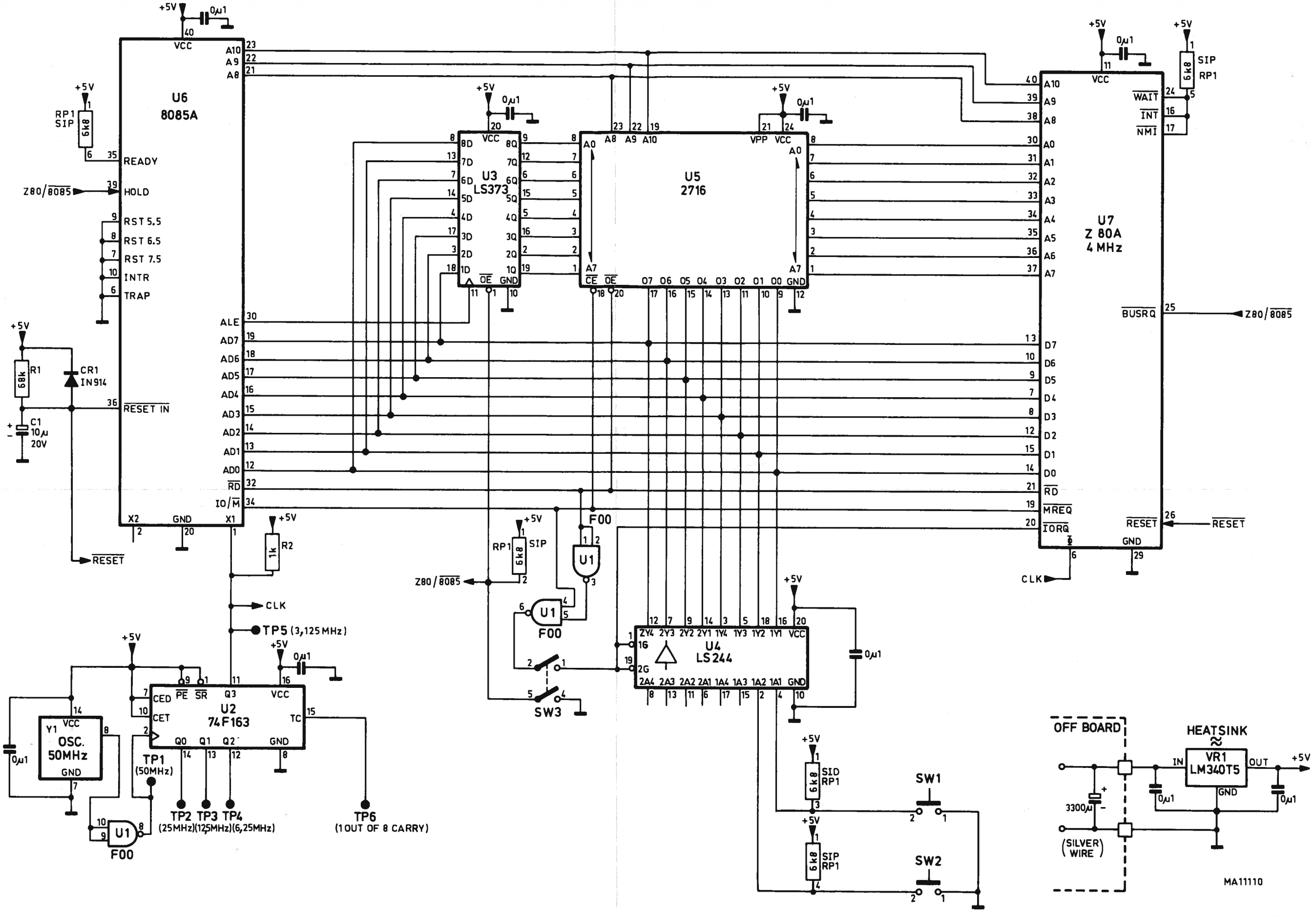
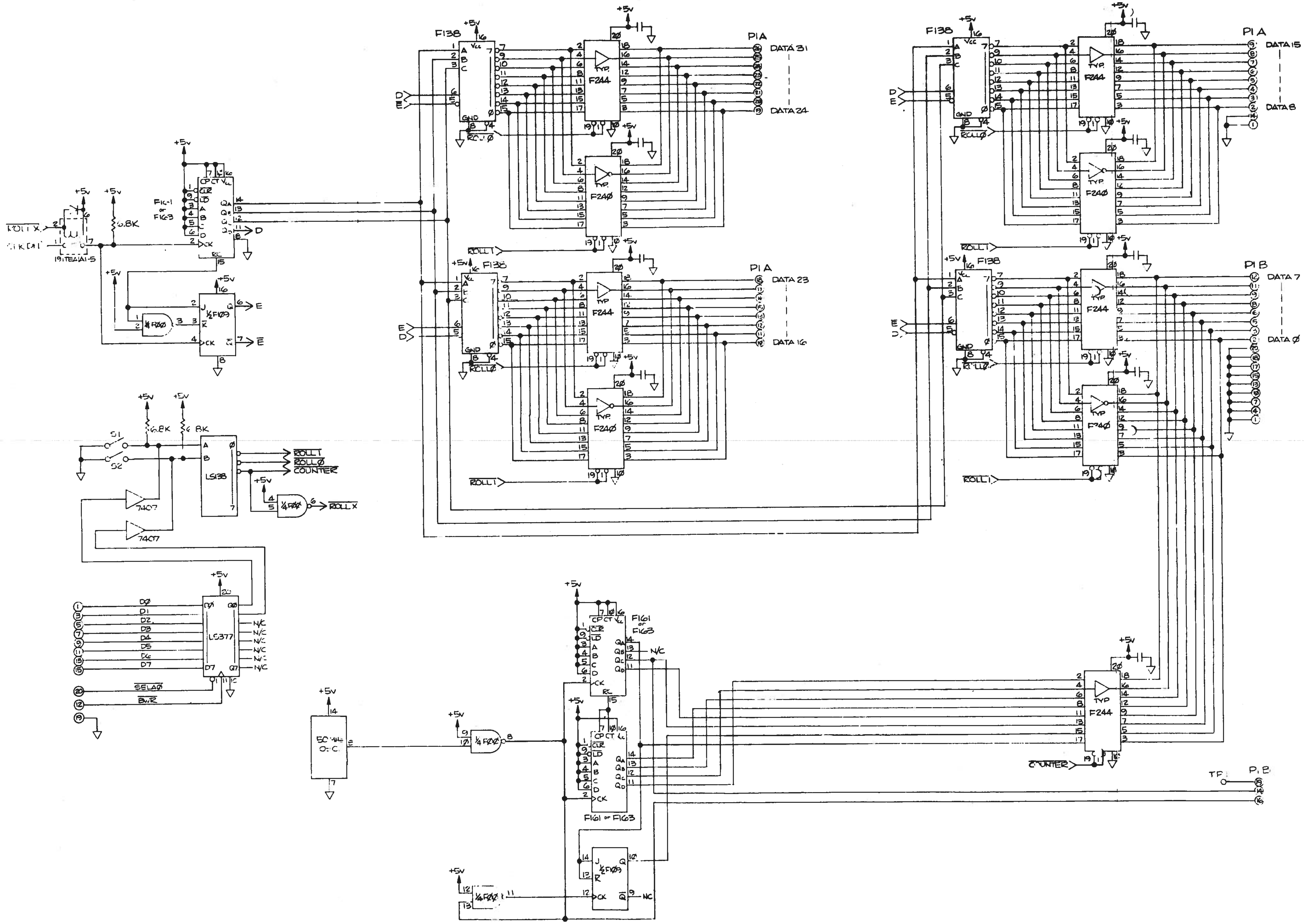


Figure 5.5: 8085/Z80 target, circuit diagram.


P1A
DATA 31
DATA 24
DATA 23
DATA 16
DATA 15
DATA 8
P1B
DATA 7
DATA Ø
F138
F244
F24Ø
ROLL 1
ROLL Ø
ROLL X
COUNTER
LS138
LS377
74O7
5C 4-4 OSC
F161 or F163
1/2 F1Ø9
D0
D1
D2
D3
D4
D5
D6
D7
SELAØ
BWR
TP
P.B
N/C
+5v

- **8085/Z80 microprocessor target**

This board contains both, the 8085 and the Z80 microprocessors, which run the same program which is stored in one prom (program listing, see appendix D). Which processsor runs the program in the prom, is selected by switch SW3.

The program contains 3 loops, which can be selected with switches SW1 and SW2. After power-up, or reset, loop 0 is entered (see figure 5.6)

Note: Power supply for the microprocessor target is not included in the PM 8891.
The unit must be supplied with the following voltage and current:
voltage: min 7.5 V connected between the IN and GND spots near voltage regulator VR1 (+7.5V at + sign).
current: min 450 mA.

Figure 5.5 shows the circuit diagram for the 8085/Z80 target.
A circuit description is not included in this manual.

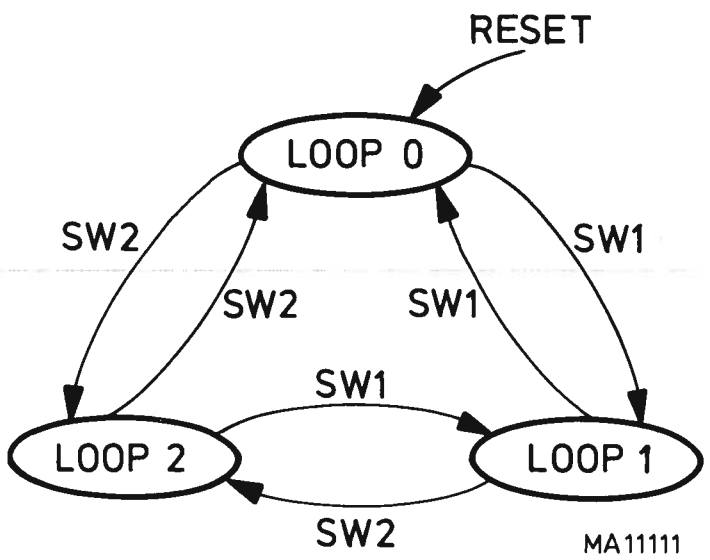


Figure 5.6: Program loops in 8085/Z80 targets.

5.4.2. Diagnostic software

The diagnostic software for the PM 3632 is contained in 3 EPROMs (27128).
These proms must be located on a disa rom board (PM8880/30) which is a part of the diagnostic tools kit. These proms must be located in sockets U5 ... U8 (sequence doesn't matter).
The disa rom board can be used together with any option, and with any software release!

No disa proms may be installed on the disa board that contains diagnostic software !

TO ENTER THE DIAGNOSTICS, THE MICROPROCESSOR AND VIDEO INTERFACE CIRCUITS MUST WORK CORRECTLY ! IF NOT, REFER TO THE FAULTFINDING TREE AND THE PROGRAM LISTING OF THE POWER-UP ROUTINES (section 5.4.3), TO FIND FAULTS IN THESE CIRCUITS.

TO ENTER A TEST, AND RUN IT SUCCESFULLY, POWER MUST BE CYCLED FIRST!!

Install disa rom board with diagnostic software in PM 3632.
Switch instrument on and press SPECIAL FUNCTIONS F.

Now you will see one of the following menus:

MENU 1:

1: Mainframe 1
2: Mainframe 2
3: Mainframe 3
4: Logic pod
5: CRT

MENU 2:

1: Fast pod
2: 8085/Z80 disa pods
3: Setup memory
4: Setup & data memory
5: RS232C control card

MENU 3:

1: Rom emul. pod: ram
2: Rom emul. pod: external
3: Rom emul. pod: input
4: RS232C: UART, osc.
5: Timing: Internal clock
6: Micro : Decoders, osc.
7: Micro : PPI, osc.

To select one of the other menus, use the scroll-up key.

To invoke a test, just press the number that is listed in front of the test. This will not present a new menu for the several subtests, but all subtests will be done sequentially.
The several subtests are listed on the next page

After a test is performed, pressing any key will return to the menu from which the test was invoked (except for the oscilloscope loop tests).

List of subtests:

Mainframe 1	:	100 MHz oscillator
		Address counter and trigger clock test
		Demultiplexers
		Internal clock dividers (partially)
Mainframe 2	:	Data path mainframe (32 channels)
Mainframe 3	:	Triggering
		Sequence controller
		Data qualification (combinational and state)
		Final delay
		Veil
Logic pod	:	External clock (falling and rising edge)
		Internal clock
		Data path (32 channels)
		Clock qualifier (high and low)
CRT	:	Video adjust
Fast pod	:	External clock (falling and rising edge)
		Internal clock
		Data path no-glitch mode (4 channels)
		Data path glitch mode (4 channels)
		Glitch capture
		Clock qualifier (high and low)
8085/Z80 disa pods	:	Pod identity (both pods)
		Pod connection (both pods)
		External clock (both pods)
		Internal clock (both pods)
		Data path (32 channels, both pods)
Setup memory	:	Non volatile storage of settings
		Edit of name fields
Setup & data memory	:	Non volatile storage of settings
		Edit of name fields
		Non volatile storage of B-memory data
		B-memory ram
		B-memory mask ram
RS232C control card	:	Uploading and downloading via RS232C connection
Rom emul. pod: ram	:	Rom emulator pod rams
Rom emul. pod: external	:	Pod connection circuit
		Port connection test circuit (ports A, B, C, D)
		Data bus, emulation side (ports A, B, C, D)
		Address bus, emulation side (ports A, B, C, D)
Rom emul. pod: input	:	Rom emulator input circuit (oscilloscoop loop)
RS232C: UART, osc.	:	RS232C transmit mode (oscilloscope loop)
Timing: Internal clock	:	Internal clock dividers
Decoders, osc.	:	Micro computer decoders (oscilloscope loop)
Micro : PPI, osc.	:	Micro computer PPI outputs (oscilloscope loop)

MENU 1

1: mainframe 1

Checks demultiplexers of PM 3632 mainframe for stuck high bits, by taking-in data via a 32 channel pod (without target) and verifing if captured data is all zero (without target, only zeroes are captured!). Also the 100 MHz clock generation, addess-counter clock and trigger clock are checked.
The internal clock dividers are partially tested.
- Connect 32 channel logic pod to mainframe - REMOVE TEST LEADS!
- Switch-on and enter test.
- Messages:

CHECK 100 MHZ AT U63 PIN 8
Clock generation, diagram 3 (the message ACTIVE blinks when this test is running).

CHECK 100 MHZ AT U37 PIN 11
Demultiplexer clock, diagram 5 (the message ACTIVE blinks when this test is running).
If not present, trace clock signal between U63 and U37, via pod.

CHECK FOR SQ. WAVE (40 NS PERIOD) AT U37-12
Demultiplexer clock, diagram 5 (the message ACTIVE blinks when this test is running).
If not present, then U37 bad.
Also check Q0, Q1, Q2 and Q3 outputs of U37 for correct phase shift (90 degrees each).

CHECK FOR 4 V PULSES AT U32 PIN 3
Trigger clock, diagram 5 (the message ACTIVE blinks when this test is running).
If not present, check 50 nsec delay line (U57) and associated circuits.

CHECK FOR 4 V PULSES AT U32 PIN 11
Address counter clock, diagram 5 (the message ACTIVE blinks when this test is running).
If not present, check 50 nsec delay line (U57) and associated circuits.

During the demultiplexer test, the test can not be interrupted. When there is something wrong, one of the following 8 messages can appear:

CHANNELS NOT ALL ZERO 100 MHZ 4CH
Input demultiplexers, diagram 5.
If bad check SIGSEL0 ... SIGSEL3 lines, and multiplexer outputs.
For connection details, see figure 2.9

CHANNELS NOT ALL ZERO 50 MHZ 8CH
Input demultiplexers, diagram 5.
If bad check SIGSEL0 ... SIGSEL3 lines, and multiplexer outputs.
For connection details, see figure 2.10

CHANNELS NOT ALL ZERO 33 MHZ 8CH
Input demultiplexers, diagram 5.
If this test fails, previous test must be ok. Therefore demultiplexers are ok. Check internal clock generation, diagram 3, diagnostic menu 3.

CHANNELS NOT ALL ZERO 25 MHZ 16CH
Input demultiplexers, diagram 5.
If bad check SIGSE0 ... SIGSEL3 lines, and multiplexer outputs.
For connection details, see figure 2.11

CHANNELS NOT ALL ZERO 20 MHZ 16CH
Input demultiplexers, diagram 5.
If this test fails, previous test must be ok. Therefore demultiplexers are ok. Check internal clock generation, diagram 3, diagnostic menu 3.

CHANNELS NOT ALL ZERO 16 MHZ 16CH
Input demultiplexers, diagram 5.
If this test fails, previous tests must be ok. Therefore demultiplexers are ok. Check internal clock generation, diagram 3, diagnostic menu 3.

CHANNELS NOT ALL ZERO 14 MHZ 16CH
Input demultiplexers, diagram 5.
If this test fails, previous tests must be ok. Therefore demultiplexers are ok. Check internal clock generation, diagram 3, diagnostic menu 3.

CHANNELS NOT ALL ZERO 12.5 MHZ 32CH
Input demultiplexers, diagram 5.
If bad check SIGSE0 ... SIGSEL3 lines, and multiplexer outputs.
For connection details, see figure 2.12

After the demultiplexer test, the test is continued with the following messages:

CHECK FOR SQ. WAVE (1 USEC PERIOD) AT U37-11
Demultiplexer clock, diagram 5
If not ok, check internal clock generation (diagram 3; see also menu 3 for a more detailed test).

CHECK FOR SQ. WAVE (6 USEC PERIOD) AT U37-11
Demultiplexer clock, diagram 5
If not ok, check internal clock generation (diagram 3; see also menu 3 for a more detailed test).

CHECK FOR SQ. WAVE (10 MSEC PERIOD) AT U37-11
Demultiplexer clock, diagram 5
If not ok, check internal clock generation (diagram 3; see also menu 3 for a more detailed test).

2: mainframe 2

Checks complete 32 channel data path in PM 3632 mainframe by taking-in a walking zero and walking one data pattern from 32 channel test board.

- Connect 32-channel test board to mainframe (via P3).
- Connect probe inputs of logic pod to P1A and P1B of 32 channel test board.
- Connect logic pod outputs (shielded flat cable) to P2 of test board.
- Switch-on and enter test.
- Messages:

SET SWITCHES DN UP UP UP - PRESS ANY KEY

Applies to DIP switch SW1 (switch 1 is down) on the 32 channel test board.

SET SWITCHES UP DN UP UP - PRESS ANY KEY

Applies to DIP switch SW1 (switch 2 is down) on the 32 channel test board.

WALKING ZERO'S ERROR

If this message appears, check state screen for a channel never changes state (1 or 0). Set triggerword to 010 and press START. Trace the bad channel with an oscilloscope, diagram 5. If the analyzer beeps 3 times, then this means that channel 0 is always high. Press START and trace channel 0, diagram 5.

WALKING ONE'S ERROR

If this message appears, check state screen for a channel which always stays low (0). Set triggerword to 101 and press START. Trace the bad channel with an oscilloscope, diagram 5. If the analyzer beeps 3 times, then this means that channel 0 is always low. Press START and trace channel 0, diagram 5.

3: mainframe 3

Checks all logic analyzer functions, by taking-in data from 8085/Z80 target and verify if captured data is correct.
This test checks:
* Triggering * Trigger sequence * Data qualification * Final delay * Veil.

- Connect 8085 pod to PM3632.
- Clip pod to microprocessor on 8085/Z80 target.
- Switch-on and enter test.
- Messages:

PRESS RESET ON TARGET
PRESS SW1

SW1 applies to switch SW1 on the 8085/Z80 target.
If this message appears, and the analyzer beeps 3 times after 15 seconds then this means that there has no trigger occurred. If the analyzer passes mainframe tests 1 and 2, than there is a trigger failure. Press START and check trigger ram address lines and outputs with an oscilloscope, diagram 5. If ok, check sequence controller and stop circuitry, diagram 6. The PPI test in menu 3 can be used as a help.

PRESS SW1 TWICE
If after pressing SW1 twice (on target), this meassage does not disappear, then press any key at the PM3632 front panel!
After pressing any key, one of the below mentioned error messages will appear, and control is given back to the keyboard again.
Note: This message will appear 6 times in total.

SEQUENCE ERROR
Indicates sequence controller error. Triggerword recognition is ok, but a sequence of triggerwords A and B fails. Check sequence controller ram U124, diagram 6. The PPI test in menu 3 can be used as a help.

SEQ WORD C-D OR QUAL ERROR
Indicates sequence controller or data qualification error. Triggerword recognition is ok, but a sequence of words C and D fails, This can also be caused by a stable TRCSTAT line (U125 pin 7). Check sequence controller ram U124, diagram 6. The PPI test in menu 3 can be used as a help.

COMB. -ONLY- QUALIFICATION ERROR
If this test fails, check data qualification circuitry U116 and U118-pin 1, diagram 6.
Press START; now the lines connecting these ic's must go up and down.

COMB. -ALL BUT- QUALIFICATION ERROR
If this test fails, check data qualification circuitry U116 and U118-pin 0, diagram 6.
Press START; now the lines connecting these ic's must go up and down.

STATE QUALIFICATION ERROR
If this test fails, check data qualification circuitry U116 and U118-pin 3. Also check U125 and associated circuits, diagram 6.
Press START; now the lines connecting these ic's must go up and down.

DELAY ERROR
Final delay circuitry fails. Check U126 (diagram 6) and U15 (diagram 3).

After these subtests, the veil test has to be done visually. The following message will appear:

CHECK FOR 40 CLOCKS VEIL
If 40 clocks veil not present, or no veil present, check timers in U135 and U136 and flip flops U109, diagram 2.

4: logic pod

This test checks 32 channel logic pod data path by taking-in a walking zero and walking-one pattern from the 32 channel tester. This is done at different clock edges, and different qualifier levels.

- Connect 32-channel test board to mainframe (via P3).
- Connect probe inputs of logic pod to P1A and P1B of 32 channel test board.
- Connect logic pod outputs (shielded flat cable) to P2 of test board.
- Switch-on and enter test
- Messages:

SWITCHES: DN UP UP UP - PRESS ANY KEY

Applies to DIP switch SW1 (switch 1 is down) on 32 channel test board

After pressing any key on the PM 3632 front panel, one of the following error messsages can appear:

EXTERNAL RISING ERROR

Press any key to go to scope loop (in loop, presssing any key will continue with next test).
Check external clock flow (rising edge), diagram 11.
Flow: P1B-pin16, U17-pin4, U33, SCK (p2-pin55).
If external clock ok, press any key to go to next test.

EXTERNAL FALLING ERROR

Press any key to go to scope loop (in loop, presssing any key will continue with next test).
Check external clock flow (falling edge), diagram 11.
Flow: P1B-pin16, U17-pin19, U33, SCK (p2-pin55).
If external clock ok, press any key to go to next test.

INTERNAL CLOCK ERROR

Press any key to go to scope loop (in loop, presssing any key will return to prom menu).
Check internal clock flow, diagram 11.
Flow: BFCLKOUT, U29, SCLK and CLK.
If all clocks (internal and external) are ok, then check clock qualification circuit, diagram10.In these tests, signal QUALIN must be high always.

32-BIT - WALKING ZEROES ERROR

Check in state display which channel does not go low.
Press START and trace with an oscilloscope the bad channel, diagram 10/11.
If analyzer beeps three times after about 15 seconds, then press START and check channel 0.

After these subtests, the test continues with the following message:

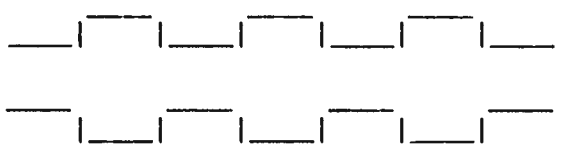
SWITCHES: UP DN UP UP - PRESS ANY KEY

Applies to DIP switch SW1 (switch 2 is down) on 32 channel test board

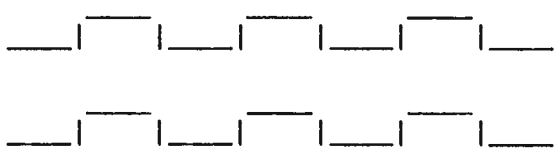
After pressing any key on the PM 3632 front panel, one of the
following error messsages can appear:

32-BIT - WALKING ONES ERROR
Check in state display which channel does not go high.
Press START and trace with an oscilloscope the bad channel,
diagram 10/11.
If analyzer beeps three times after about 15 seconds, then press
START and check channel 0.

CLOCK QUALIFIER LOW ERROR
Press any key to go to scope loop (in loop, pressing any key
will return to prom menu).
Check clock qualifier circuitry, diagram 10.
The QUALIN sinal must be high when the external qualifier signal
is low.



CLOCK QUALIFIER HIGH ERROR
Press any key to go to scope loop (in loop, pressing any key
will return to prom menu).
Check clock qualifier circuitry, diagram 10.
The QUALIN sinal must be high when the external qualifier signal
is high.



5: CRT

This test writes a square pattern (like a checker board) on the crt.
This test can be used for video adjustment and for fault finding in
the video interface circuit.
During this test, pressing any key returns to menu 1.

MENU 2

1: fast pod

This test checks 4 channel fast pod data path by taking-in a walking zero and walking-one pattern from the 32 channel test board, in glitch mode and no-glitch mode.
This is done at different clock edges, and different qualifier levels.
The glitch capture circuit is also tested (not for 5 nsec glitches).

- Connect 32-channel test board to mainframe (via P3).
- Connect probe input of fast pod to P4 of 32 channel test board.
- Connect fast pod outputs (shielded flat cable) to P2 of test board.
- Switch-on and enter test.
- Messages:

SWITCHES: DN UP UP UP - PRESS ANY KEY

Applies to DIP switch SW1 (switch 1 is down) on 32 channel test board.
After pressing any key on the PM 3632 front panel, one of the below mentioned error messages can appear.

SWITCHES: UP DN UP UP - PRESS ANY KEY

Applies to DIP switch SW1 (switch 2 is down) on 32 channel test board.
After pressing any key on the PM 3632 front panel, one of the below mentioned error messages can appear.

SWITCHES: UP UP UP UP - PRESS ANY KEY

Applies to DIP switch SW1 (all switches up) on 32 channel test board.
After pressing any key on the PM 3632 front panel, one of the below mentioned error messages can appear.

EXTERNAL RISING ERROR

Press any key to go to scope loop (in loop, presssing any key will continue with next test).
Check external clock flow (rising edge), diagram 13.
Flow: J2-pin1, U10, K1/K2, U16, U15, SCK (p2-pin55).
If external clock ok, press any key to go to next test.

EXTERNAL FALLING ERROR

Press any key to go to scope loop (in loop, presssing any key will continue with next test).
Check external clock flow (falling edge), diagram 13.
Flow: J2-pin1, U10, K1/K2, U16, U15, SCK (p2-pin55).
If external clock ok, press any key to go to next test.

INTERNAL CLOCK ERROR

Press any key to go to scope loop (in loop, presssing any key will return to prom menu).
Check internal clock flow, diagram 13.
Flow: BFCLKOUT, U7, K1, U16, U15, SCLK.
If all clocks (internal and external) are ok, then check clock qualification circuit, diagram10.In these tests, signal QUALIN must be high always.

NON-GLITCH 4-BIT - WALKING ZEROES ERROR

Check in state display which channel does not go low.
Press START and trace with an oscilloscope the bad channel, diagram 12 (non glitch path).
If analyzer beeps three times after about 15 seconds, then press START and check channel 0.

NON-GLITCH 4-BIT - WALKING ONES ERROR

Check in state display which channel does not go high.
Press START and trace with an oscilloscope the bad channel, diagram 12 (non glitch path).
If analyzer beeps three times after about 15 seconds, then press START and check channel 0.

GLITCH 4-BIT - WALKING ZEROES ERROR

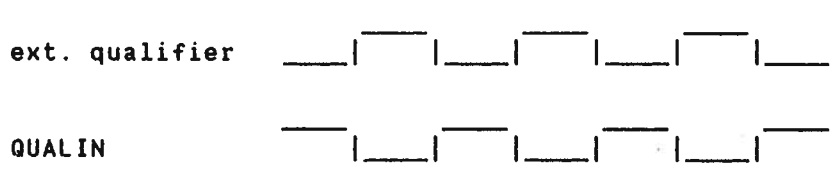
Check in state display which channel does not go low.
Press START and trace with an oscilloscope the bad channel, diagram 12 (glitch path)
If analyzer beeps three times after about 15 seconds, then press START and check channel 0.

GLITCH 4-BIT - WALKING ONES ERROR

Check in state display which channel does not go high.
Press START and trace with an oscilloscope the bad channel, diagram 12 (glitch path).
If analyzer beeps three times after about 15 seconds, then press START and check channel 0.

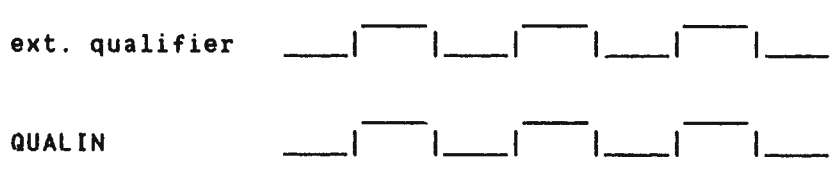
CLOCK QUALIFIER LOW ERROR

Press any key to go to scope loop (in loop, pressing any key will return to prom menu).
Check clock qualifier circuitry, diagram 13
The QUALIN sinal must be high when the external qualifier signal is low.



CLOCK QUALIFIER HIGH ERROR

Press any key to go to scope loop (in loop, pressing any key will return to prom menu).
Check clock qualifier circuitry, diagram 13.
The QUALIN sinal must be high when the external qualifier signal is high.



After these subtests, the test continous with the following message:

CHECK FOR EQUAL AND REGULAR
SQ WAVE ON ALL CHANNELS
If not present, then there is a glitch capture error. Pressing any key will always go to a scope loop. In loop, pressing any key will return to menu 2.
Check bad channel with oscilloscope, diagram 13.

2: 8085/Z80 pod

This test checks the 8085 and Z80 disa pods for a bad data channel (only in 8085 or Z80 mode).
This is done by taking-in data from the 8085/Z80 demo unit and checking all the used data channels if they are sampled correct.
Also pod connection, external and internal clock are tested.

- Connect 8085/Z80 pod to microprocessor target.
- Switch-on and enter test
- Messages:

SWITCH-OFF AND CONNECT DISA POD
TO PM 3632
THEN ENTER DIAGNOSTICS AGAIN
This message indicates that the microprocessor in the mainframe can not read buffer U19 correctly.

This test, can not be interrupted. When there is something wrong, one of the following messages can appear:

POD CONNECTION ERROR
When this message appears, then the either the pod is not connected correctly by the user, or the circuit that checks the pod connection is bad. When this message appears, pressing any key will continue the tests.

ACTIVE
When this message appears, then there is something wrong in the pod. Press any key to view error message.

EXTERNAL CLOCK FAILURE
TRACE EXTERNAL CLOCK FROM
U9 (U7/U11) VIA U7 (U16) TO
DEMULTIPLEXERS IN MAINFRAME
When this message appears, the logic analyzer is in a loop in which it will not trigger, so you can check the complete external clock circuitry.
The numbers between brackets apply to the Z80 pod.

INTERNAL CLOCK FAILURE
TRACE INTERNAL CLOCK FROM
MAINFRAME VIA U7 (U16) TO MAINFRAME
When this message appears, the logic analyzer is in a loop in which it will not trigger, so you can check the complete internal clock circuitry.
The number between brackets applies to the Z80 pod.

ADDRESS AND DATA ERROR
There is a failure in the address bus and the data bus. This causes the test to fail when it tries to trigger. After pressing any key, press START and check manually which channels are stuck to zero or one.

PROBE [ ] BAD
Indicates that a certain channel is stuck high or low. Pressing any key proceeds to next test. When all tests are done and one or more channels are bad, then the logic analyzer is put in a loop in which you can trace the bad channel(s) with an oscilloscope.
NOTE: When using this test on pods PM8865-revision C, the side probes SP0...SP3 will always be reported BAD because they are always high and the test assumes they are always low.

3: Setup memory
This test stores settings under each of the 8 available setup files. Then it reads these settings back and verifies if they are correct. Also the name field is tested, if it is possible to fill-in a name.
- Connect any pod to PM3632 (no target required).
- Switch-on and enter test.
- Messages:

A/B RAM FAILURE
This message appears immediately after power-up, when there is something wrong with rams U2 or U8 at the setup and data memory option. Check read, write and select lines to these twwo rams.

SWITCH-OFF AND CONNECT DISA POD
THEN ENTER DIAGNOSTICS AGAIN
No disa pod is connected, connect any pod and enter diagnostics again.

This test can not be interrupted. Dureing the test, one of the following messages can appear:

SETUP MEMORY CHECKSUM ERROR
One of the EEPROMs is bad, check U7.

SETTINGS CAN NOT BE SAVED
Check read, write and chip select signals to EEPROM.

NAME FIELD CAN NOT BE CHANGED
Check system prom U1.

4: Setup & data memory
Note that this test takes about 10 minutes.
For setup memory test, see setup memory test.
For data memory testing, the PM 3632 takes-in data from the 8085 demo unit and stores this data in the data memory file.
After this, the stored data is read back and is verified if it is correct.
The edit mode is checked by writing data (0, 1 and X) into b-memory and check if the written data is actually stored in b-memory.
- Connect 8085 or Z80 pod to micropocessor target
- Switch-on and enter test.
- Messages:

A/B RAM FAILURE

This message appears immediately after power-up, when there is something wrong with rams U2 or U8 at the setup and data memory option. Check read, write and select lines to these twwo rams.

SWITCH-OFF AND CONNECT DISA POD
THEN ENTER DIAGNOSTICS AGAIN

No disa pod is connected, connect 8085 or Z80 pod and enter diagnostics again.

This test can not be interrupted. Dureing the test, one of the following messages can appear:

SETUP MEMORY CHECKSUM ERROR

One of the EEPROMs is bad, check U3, U4, U5, U6 and U7, diagram 23, 24.

SETTINGS CAN NOT BE SAVED

Check read, write and chip select signals to EEPROMs, diagrams 23, 24.

NAME FIELD CAN NOT BE CHANGED

Check system prom U1, diagram 23.

B MEMORY CHECKSUM ERROR

One of the EEPROMs is bad, check U3, U4, U5, U6 and U7, diagram 23, 24.

BIT STUCK TO ZERO IN B MEMORY

RAM U2 (B-memory) is failing and must be replaced, diagram 23.

BIT STUCK TO ONE IN B MEMORY

RAM U2 (B-memory) is failing and must be replaced, diagram 23.

B MEMORY DONT CARE NOT POSSIBLE

RAM U2 (B-memory) is failing and must be replaced. Or addressline A12 is always zero, diagram 23.

5: RS232C control card

The RS232C control card is checked by sending out settings via the transmit output to the PM4202 digital cassette recorder (or any other device that can receive and transmit data), and read the same data back afterwards.

- Install Setup and data memory option
- Install RS232C control card
- Make sure that cassette is at beginning of tape!
- Test can only be done immediately after power-up of the instrument
- Switch-on and enter test.
- Messages:

MAKE CONNECTIONS TO PM4202
OIGITAL CASSETTERECORDER AS FOLLOWS:

PM3632		PM4402
(FG)	1 --	1 (FG)
(TXD)	2 --	3 (RXD)
(RXD)	3 --	2 (TXD)
(CTS)	5 --	4 (RTS)
(SG)	7 --	7 (SG)

Connections to cassette recorder must be made as described.
If connections were not already present, power must be cycled after connections are made.
If no cassette recorder is available, refer to the manuals of the connected device, for connection details. Connections to PM3632 remain as described.

SET SWITCHES ON RECORDER AS FOLLOWS:

KEYS	ENABLE
KEYS	REMOTE
BLOCK LENGTH	1024
CRC CHECK	NO
AUTO REWIND	YES
TRANSPARENT	YES
RS232C	V24
PARITY	EVEN
WORD	8 BITS
STOP BIT	1
PARITY	DISABLE
BAUDRATE	9600

Settings of the cassette recorder must be mede as described, in order to make communication with analyzer possible.
If another device is connected, refer to the manuals to make the correct settings.

PRESS WRITE ON RECORDER
Puts cassette recorder in receiver mode.
If another device is connected to the analyzer, refer to the manuals how to put it in receiver mode.

PRESS WRITE AGAIN
Empties receiver buffer of cassette recorder onto the tape.
If another device is connected, refer to the manuals how to handle received data.

DOWNLOAD ... PLEASE WAIT
If this message is fashing on the display, then press on the casette recorder: STANDBY, REVERSE, READ, in this sequence.
If this message does not disappear a few seconds after pressing READ, then check the TXD and RXD lines. Menu 3 contains an oscilloscope loop for checking the TXD line).
If anaother device is connected, refer to the manuals how to transmit the received data back to the analyzer.

RS 232C COMMUNICATION ERROR
This message means that the settings received back from the cassette recorder are not the same as the settings that were sent to it. Check system prom U6 for correct checksum.
Also UART U12 can be bad.
The analyzer however has recognized the end of transmit character.

MENU 3

1: Rom emul. pod: Rams

Note that this test takes about 5 minutes.
This test checks for stuck high or low bits in the rom emulator pod rams, by filling the rams with zeroes or ones and then calculate a checksum.
- Connect rom emulator pod via rs232c control card to PM3632.
- Switch-on and enter test.
- The following error messages can appear:

CONNECT CABLE BETWEEN RS232C CARD
AND ROM EMULATOR POD

Cable between rs232c and rom emulator pod is not connected, or the input circuit of the pod is bad.
If it was not connected, power must be cycled after connection is made.
If you are sure that the cable is correct, then test rom emulator pod input circuit, menu 3. See diagram 14.

BIT STUCK TO ONE IN EMULATOR RAM

Somewhere in the rom emulator pod, there is a bit stuck to one.
To find out in which ram the bat spot is, scroll through the contents of the rom emulator pod, and consult the following table (diagrams 14 and 15):
bad spot between:

0000	07FF	RAM U13
0800	0FFF	RAM U14
1000	17FF	RAM U15
1800	1FFF	RAM U16
2000	27FF	RAM U20
2800	2FFF	RAM U21
3000	37FF	RAM U22
3800	3FFF	RAM U23

Note that when a ram failure is pointed out, it can also be the selection of those rams! For example, when an output enable line of one of the rams is always low, that particular ram will be displayed ok, but all the others as bad.

BIT STUCK TO ZERO IN EMULATOR RAM

Somewhere in the rom emulator pod, there is a bit stuck to zero.
To find out in which ram the bat spot is, scroll through the contents of the rom emulator pod, and consult the following table (diagrams 14 and 15):
bad spot between:

0000	07FF	RAM U13
0800	0FFF	RAM U14
1000	17FF	RAM U15
1800	1FFF	RAM U16
2000	27FF	RAM U20
2800	2FFF	RAM U21
3000	37FF	RAM U22
3800	3FFF	RAM U23

Note that when a ram failure is pointed out, it can also be the selection of those rams! For example, when an output enable line of one of the rams is always low, that particular ram will be displayed as ok, but all the others as bad.

2: Rom emul. pod: External

This test checks the inputs of the rams in the rom emulator pod, from the "emulation side".
It checks the connection circuitry of the pod to the RS232C control card, and the connection error circuitry for each of the 4 ports.
Then it tests the data bus and the address bus that go to the rams in the pod (for each of the 4 ports).

- Connect an 8085 or Z80 pod to 8085/Z80 target
- Remove prom from target
- Install RS232C control card
- Connect rom emulator pod to RS232C card
- Switch-on and enter test
- Messages:

TEST REQUIRES Z80 OR 8085 POD
Disa pod is not connected to the analyzer.

TEST REQUIRES ROM EMULATOR POD
Rom emulator pod is not connected to the analyzer. If it is connected, go to rom emulator input test to find fault in input circuit.

CONNECT ROM CABLE TO PORT A (B, C OR D)
THEN CONNECT ROM PLUG TO TARGET
CONNECT CLIP OF POD TO MICROPROCESSOR
Make rom emulator pod connection to target prom socket (red wire is pin 1), and connect clip of disa pod to microprocessor on target. Pressing any key will start test.

INSTALLATION ERROR PORT A (B, C OR D)
CHECK Q1 (Q2, Q3 OR Q4)
Appears only when there is a connection error, or a failure in the connection error detection circuit.
Check FET Q1 which generates connection error for port A and passes this information to the mainframe via U11. Pressing any keey will repeat this test, see diagram 15 and 14.

RESET TARGET
Rom emulator pod is filled with new data. Target must be reset in order to make analyzer trigger correctly on new data.

After resetting the target, the test can not be interrupted anymore.
If there is something wrong, then one of the following error messages can appear:

POD CONNECTION ERROR
The disa pod is not connected to the target correctly.
Make correction correctly and enter test again (after switch-off).

ACTIVE
When this message keeps blinking after target is reset, then press any key to view error message.

DATA BUS FAILURE: CHECK MANUALLY (can be for ports A, B, C or D)
This message can appear with data all AA or all 55. Control is back to front panel again. Check data bus for a stuck high or low bit. Fill data field in trigger menu with 0011 and press START. Then trace bad channel(s) with and oscilloscope, diagram 14 and 15.

ADDRESS BUS FAILURE: CHECK MANUALLY (can be for ports A, B, C or D)
The address bus should be displayed in increasing order. The address at the top line of the display is not 1 higher than the previous address, but has some other value. Check manually which channel must be wrong. Then fill data field in trigger menu with 0011 and press START. Then trace bad channel(s) with an oscilloscope, diagram 14 and 15.

U24/U25/U7/U8 FAILURE (can be for ports A, B, C or D)
Due to a failure in the selection of the ram addresses, the wrong data is written at the wrong place in the ram, or the microprocessor reads the wrong data at a different address.
If rom emulator ram test is ok, then the failure must be in U24, U25 or RP1.
The rom emulator must be filled with 55 on all addesses, except for the following addresses:

0000	00
0001	A8
0004	A9
0008	AA
0010	AB
0020	AC
0040	AD
0080	AE
0100	AF
0200	B0
0400	B1

If the sampled data does not show this data at these addresses, check manually which address line must be bad.
Fill data field in trigger menu with FF and press START, then bad address lines with an oscilloscope, diagram 14 and 15.

3: Rom emul. pod: Inputs, osc.
This test sends out data to the rom emulator pod continuously.
This can be traced with and oscilloscope.
The test requires a good working rom emulator pod and a good working RS232C control card.
- Install RS232C control card
- Connect good working pod to RS232C control card
- Switch-on and enter test
- Messages:

ROMPOD INPUT ERROR
SWITCH-OFF AND REPLACE FAULTY POD
WITH WORKING POD
THEN ENTER DIAGNOSTICS AGAIN
This message indicates that the conected rom emulator pod is faulty. Connect a good working pod and cycle power. This is necessary in order to enter the oscilloscope loop.

CHECK RS232C CARD
The RS232C control card is not installed or the identity buffer (U2) of this card is failing. If installed, go to UART osc. test.

ROM EMULATOR POD: OK
CONNECT FAULTY POD
WITHOUT SWITCH-OFF
The rom emulator pod that was connected was the good one. Now connect the bad one and press any key. This will activate the oscilloscope loop.

ROMPOD INPUT ERROR
SCOPE LOOP
The test is in a loop now. You can trace the clock signal to the pod (BCLK) and a continuous data stream through U12, U9, U17, U18, U11, U13, U12, see diagram 14 and 15.
Power must be turned-off to abort the scope loop, since it is not possible for the microprocessor to monitor the keyboard when it is performing this loop.

4: RS232C: UART, osc.

This test checks the internal clock dividers in the mainframe.

Data is transmitted continuously via the RS232C control card. This data stream can be traced with an oscilloscope.

- Install RS232C control card in mainframe
- Connect 32 channel logic pod to analyzer (any disa pod can be used also, but it must be connected to a terget then).
- Switch-on and enter test
- Messages:

SWITCH-OFF AND CONNECT LOGIC POD
THEN ENTER DIAGNOSTICS AGAIN
There is no pod connected to the analyzer. This test however requires a pod.

POD CONNECTION ERROR
Appears when disa pod is used used and it is not connected to the target correctly.

U2 BAD
Identity buffer U2 can not be read by the microprocessor, or the RS232C control card is not installed correctly. Pressing any key will return to prom menu 3.

When STATE display is displayed, then test is in a scope loop, continuously sending out the state analyzer screen. The TXD line of the RS232C control card can be traced now with an oscilloscope. Power must be turned-off to abort the scope loop, since it is not possible for the microprocessor to monitor the keyboard when it is performing this loop.

5: Timing: Internal clock, osc.

This test checks the internal clock dividers in the mainframe.

- Connect 32 channel logic pod to analyzer
- Switch-on and enter test
- Messages:

CHECK 100 MHZ CLOCK AT U63 PIN 6
VIA U61/U62
TRACE CLOCK SIGNAL INTO POD
AND BACK TO U37 IN MAINFRAME
Internal clock dividers for 100 MHz can be traced with an oscilloscope, diagrams 3, 5, 10 and 11.

CHECK 50 MHZ CLOCK AT U63 PIN 6
VIA U53/U59/U61/U62
TRACE CLOCK SIGNAL INTO POD
AND BACK TO U37 IN MAINFRAME
Internal clock dividers for 50 MHz can be traced with an oscilloscope, diagrams 3, 5, 10 and 11.

CHECK 10 MHZ CLOCK AT U63 PIN 6
VIA U53/U51/U52/U59/U62
TRACE CLOCK SIGNAL INTO POD
AND BACK TO U37 IN MAINFRAME
Internal clock dividers for 10 MHz can be traced with an oscilloscope, diagrams 3, 5, 10 and 11.

CHECK 10 KHZ CLOCK AT U63 PIN 6
VIA U53/U16/U52/U59/U62
TRACE CLOCK SIGNAL INTO POD
AND BACK TO U37 IN MAINFRAME
Internal clock dividers for 10 kHz can be traced with an oscilloscope, diagrams 3, 5, 10 and 11.

6: Micro : Decoders, osc.
This test puts the decoder of the microprocessor in a scope loop, in which all of the decoder outputs are selected one by one.
- No connections required
- Messages:

DECODER TEST ACTIVE
SCOPE LOOP
Pulses can be measured at the following points, diagram 2:
U103 pin 15
U103 pin 14
U103 pin 13
U103 pin 12
U103 pin 11
U103 pin 10
U103 pin 9
U103 pin 7
U113 pin 20
U121 pin 20
Power must be turned-off to abort the scope loop, since it is not possible for the microprocessor to monitor the keyboard when it is performing this loop.

7: Micro : PPI, osc.
This test puts all the PPI outputs in a scope loop, in which all of the outputs are selected one by one.
- No connections required
- Messages:

PPI TEST ACTIVE
SCOPE LOOP

Pulses can be measured at the following points, diagram 2:

U16 pins 1, 2, 5, 21 ... 39

U15 pins 1, 21 ... 39
To check pins 2 and 5, the diagnostic board must be put in different connectors at the capture board. The signals at these 2 pins are stable, refer to the following table:

diagnostic board in:	J3	J4	J5
state of pin 2	H	L	H
state of pin 5	L	H	H

U134 pins 1, 21 ... 36, 39
The remaining pins have in this test always the same state:
pin 2,5, 37 High
pin 38 Low

U135 pins 1, 2, 5, 21 ... 39

U136 pins 1, 2, 5, 21 ... 39

Power must be turned-off to abort the scope loop, since it is not possible for the microprocessor to monitor the keyboard when it is performing this loop.

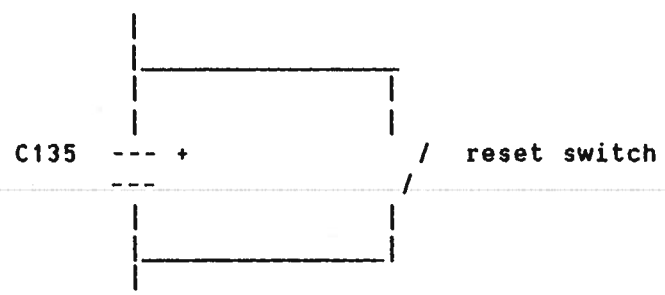
5.4.3. Power-up routines

When it is not possible to enter the diagnostics, or get a useful picture on the screen, then there is something wrong in the microcomputer of the PM 3632.

This part can be tested, using a second logic analyzer (PM 3632 or PM 3551(A)) which has to be connected to the 8085 microprocessor in the faulty PM 3632 mainframe.
Twelve test are available for this: Six for main software revision K, and six for main software revision L. If the faulty PM 3632 (which we will further call **target-analyzer**) passes six of these tests (depending on the software revision) then it is able to enter the software on disa rom board (program starts at address 8000).

This section only describes the test procedure, using a PM 3632. The following is required to do the tests succesfully:

- PM 3632 mainframe (which we will further call **test-analyzer**).
- PM 8865 intel disassembler pod
- Because the PM 3632 can not capture power-up routines, you have to add a reset switch with which you can short circuit capacitor C135 at the microcomputer board (in the test-analyzer).



- Install 8085 disassembler prom at the PM8880/30 disassembler board.
- Install disa rom board in the test-analyzer.
- Connect the 8085 disassembler pod to the 8085 microprocessor in the target-analyzer.
- Switch-on both logic analyzers.

NOTE: When using a PM 3551(A) logic analyzer as the test-analyzer, the reset-switch is not necessary. To use this analyzer, you need:

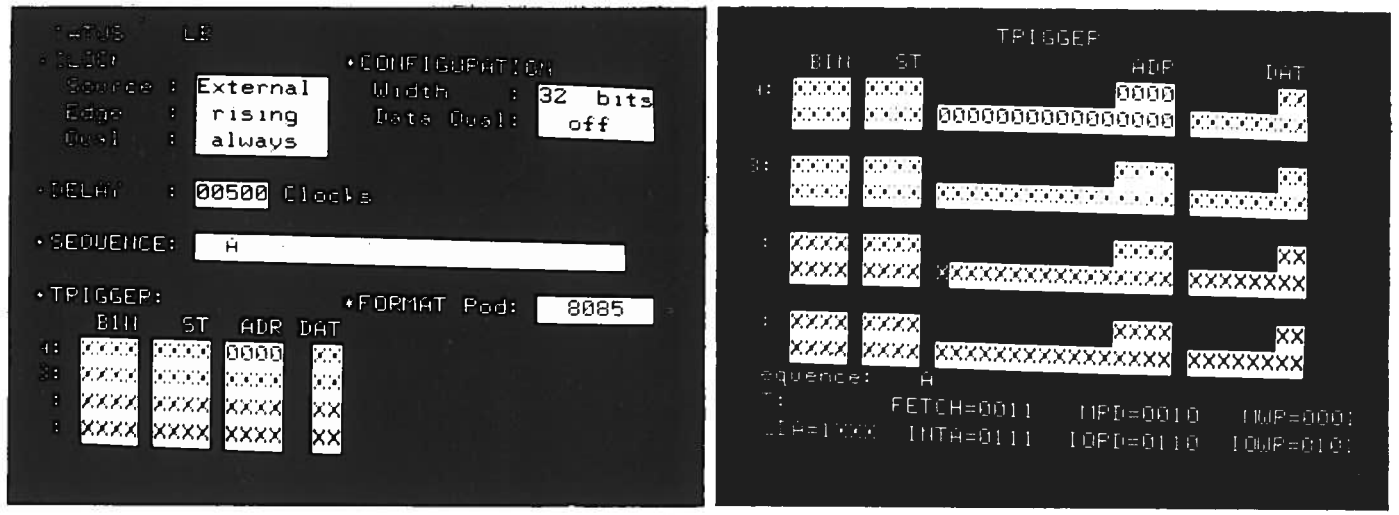
- *PM 3551(A)/10 mainframe or better.*
- *A or N pack disassembler.*
- *8085 personality adapter.*
- *any option board on which you can install the disassembler.*

Then connect the personality adapter to the 8085 microprocessor in the target-analyzer PM 3632, and switch-on the PM 3551(A).
After this, the PM3551(A) settings can be selected by selecting the 8085 disassembler in the option menu.
The target-analyzer can be reset by switching it off and on.

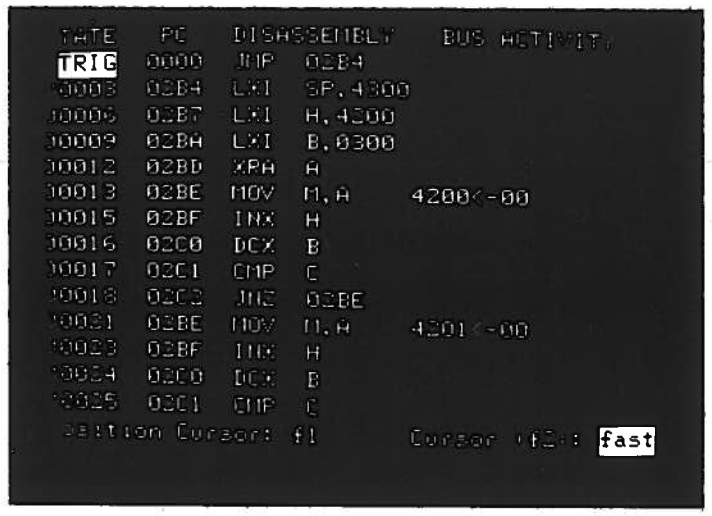
- **SOFTWARE REVISION K**

- **test 1**

At the test-analyzer, set triggerword A: XXXX XXXX 0000 XX and trigger sequence to "A" (FIND WORD A).

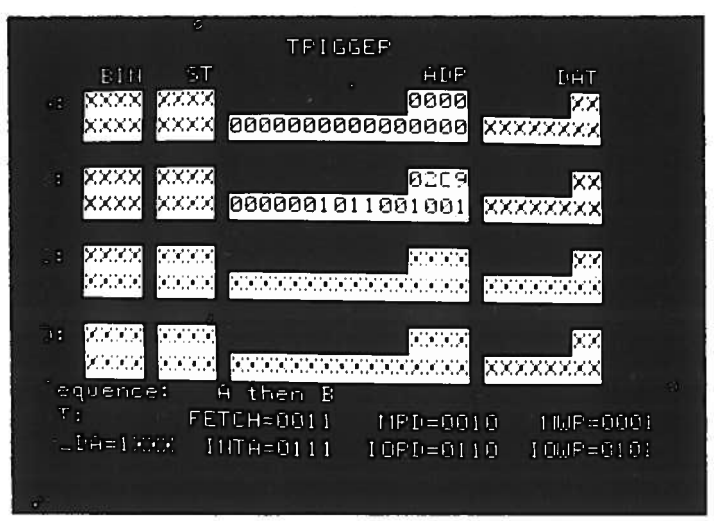


Start data acquisition and press the reset switch.
The test-analyzer must show the following data:

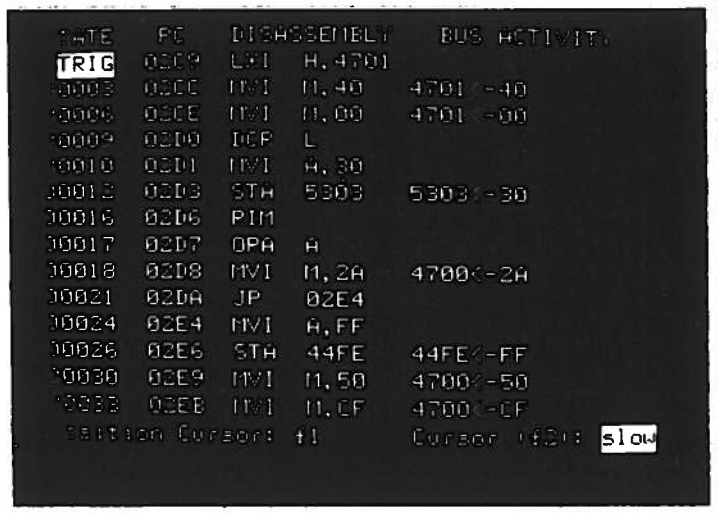


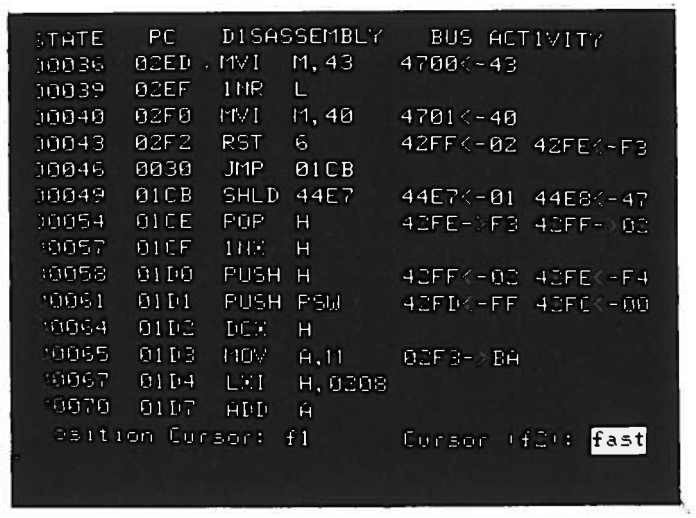
- **test 2**

At the test-analyzer, set triggerword A: XXXX XXXX 0000 XX and triggerword B: XXXX XXXX 02C9 XX. Set trigger sequence to "A then B"



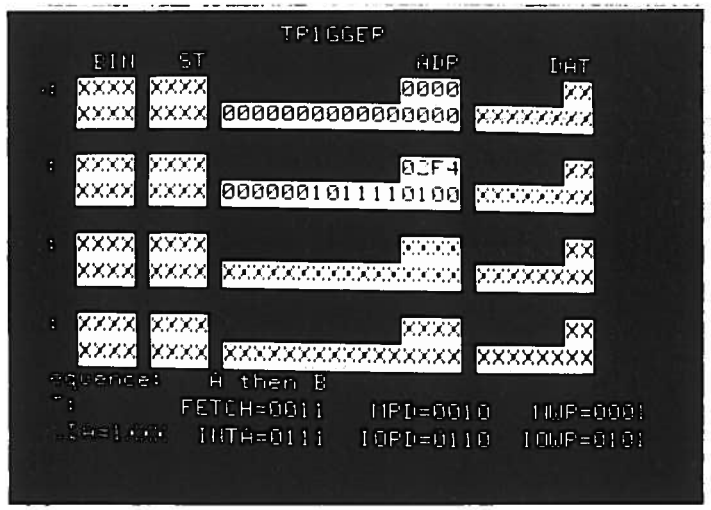
Start data acquisition and press the reset switch.
The test-analyzer must show the following data:



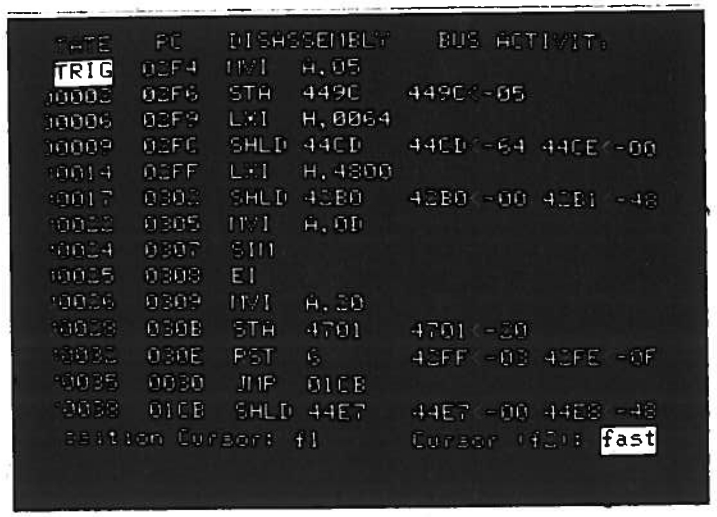


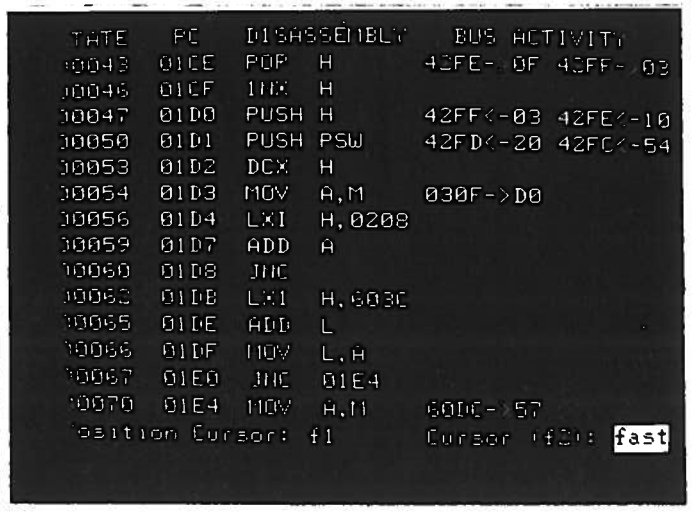
- test 3

At the test-analyzer, set triggerword A: XXXX XXXX 0000 XX and triggerword B: XXXX XXXX 02F4 XX. Set trigger sequence to "A then B"



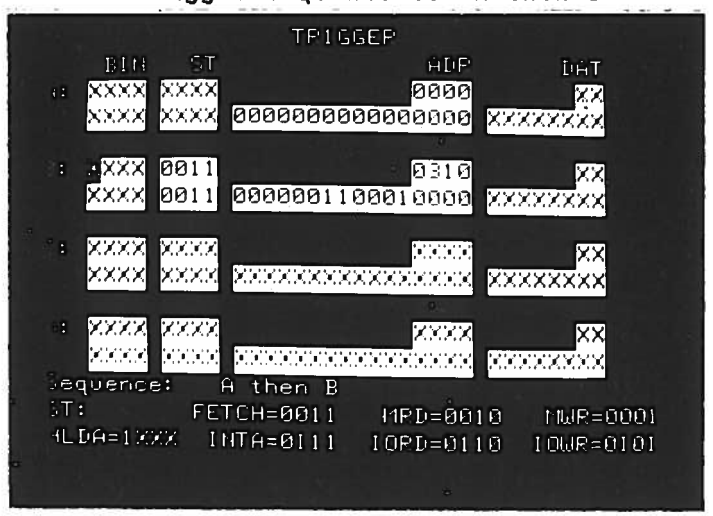
Start data acquisition and press the reset switch.
The test-analyzer must show the following data:



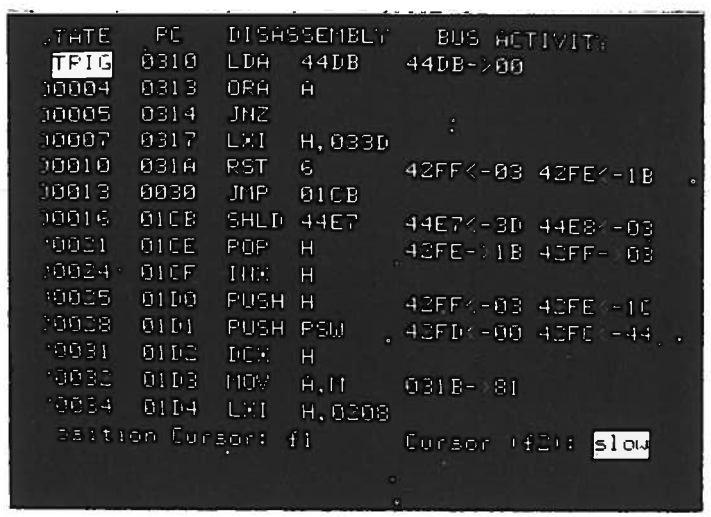


- test 4

At the test-analyzer, set triggerword A: XXXX XXXX 0000 XX and triggerword B: XXXX 0011 0310 XX. Set trigger sequence to "A then B"

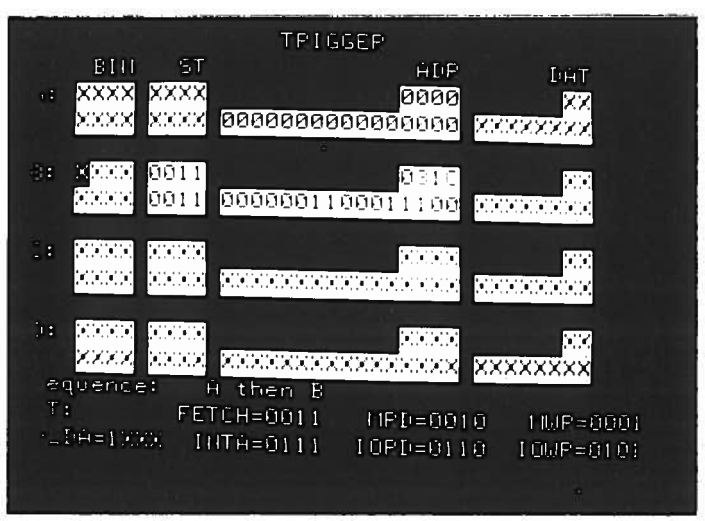


Start data acquisition and press the reset switch.
The test-analyzer must show the following data:

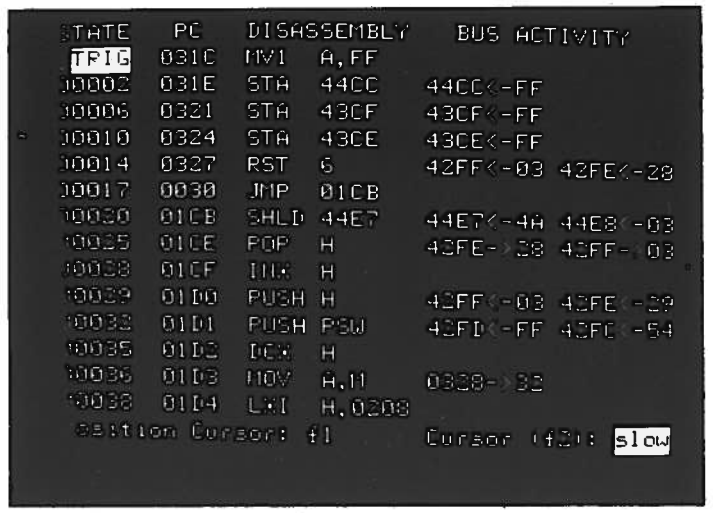


- test 5

At the test-analyzer, set triggerword A: XXXX XXXX 0000 XX and triggerword B: XXXX 0011 031C XX. Set trigger sequence to "A then B"

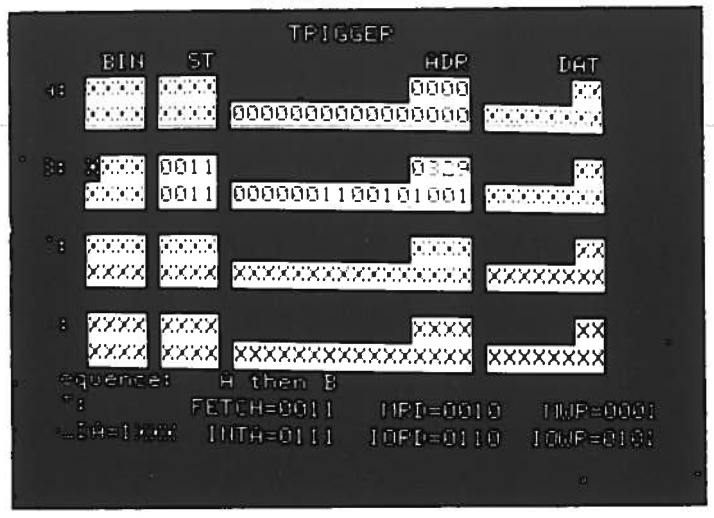


Start data acquisition and press the reset switch.
The test-analyzer must show the following data:

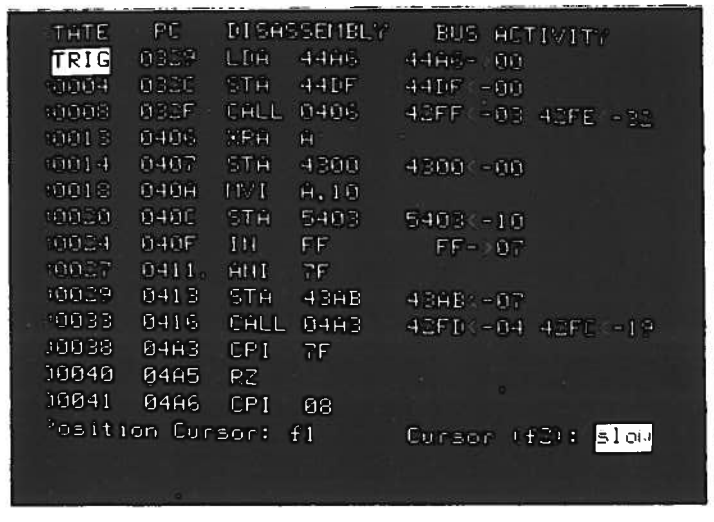


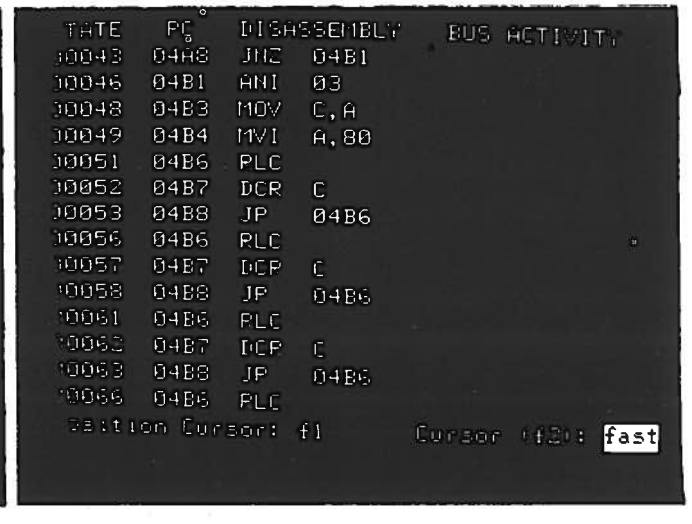
- test 6

At the test-analyzer, set triggerword A: XXXX XXXX 0000 XX and triggerword B: XXXX 0011 0329 XX. Set trigger sequence to "A then B"



Start data acquisition and press the reset switch.
The test-analyzer must show the following data:





```
STATE   PC   DISASSEMBLY    BUS ACTIVITY
00067  04B7  DCR  C
00068  04B8  JP
00070  04BB  MVI  B,00
00072  04BD  DCR  A
00073  04BE  MOV  C,A
00074  04BF  JZ
00076  04C2  IN   80        80->FD
00079  04C4  ANI  F8
00081  04C6  ORA  C
00082  04C7  OUT  80        80<-FF
00085  04C9  CALL 04DC    42FB<-04 42FA<-CC
00090  04DC  LDA  8000    8000->AA
00094  04DF  XPI  AA
00096  04E1  RNZ
Position Cursor: f1       Cursor (f2): fast
```

```
STATE   PC   DISASSEMBLY    BUS ACTIVITY
00097  04E2  INR  B
00098  04E3  PUSH D        42F9<-40 42F8<-0D
00101  04E4  PUSH B        42F7<-01 42F6<-07
00104  04E5  LDA  8001     8001->03
00108  04E8  LXI  H,0400
00111  04EB  DAD  H
00112  04EC  DCR  A
00113  04ED  JP   04EB
00116  04EB  DAD  H
00117  04EC  DCR  A
00118  04ED  JP   04EB
00121  04EB  DAD  H
00122  04EC  DCR  A
00123  04ED  JP   04EB
Position Cursor: f1       Cursor (f2): fast
```

```
STATE   PC   DISASSEMBLY    BUS ACTIVITY
00126  04EB  DAD  H
00127  04EC  DCR  A
00128  04ED  JP
00130  04F0  LXI  D,8000
00133  04F3  XCHG
00134  04F4  RST  6        42F5<-04 42F4<-F5
00137  0030  JMP  01CB
00140  01CB  SHLD 44E7     44E7<-00 44E8<-80
00145  01CE  POP  H        42F4->F5 42F5->04
00148  01CF  INX  H
00149  01D0  PUSH H        42F5<-04 42F4<-F6
00152  01D1  PUSH PSW      42F3<-FF 42F3<-84
00155  01D2  DCX  H
00156  01D3  MOV  A,M      04F5->BC
Position Cursor: f1       Cursor (f2): fast
```

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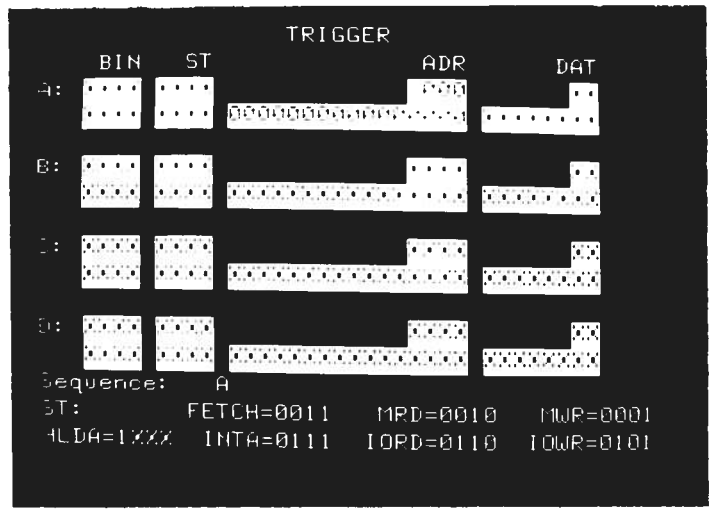
- **SOFTWARE REVISION L**

- **test 1**

At the test-analyzer, set triggerword A: XXXX XXXX 0000 XX and trigger sequence to "A" (FIND WORD A).



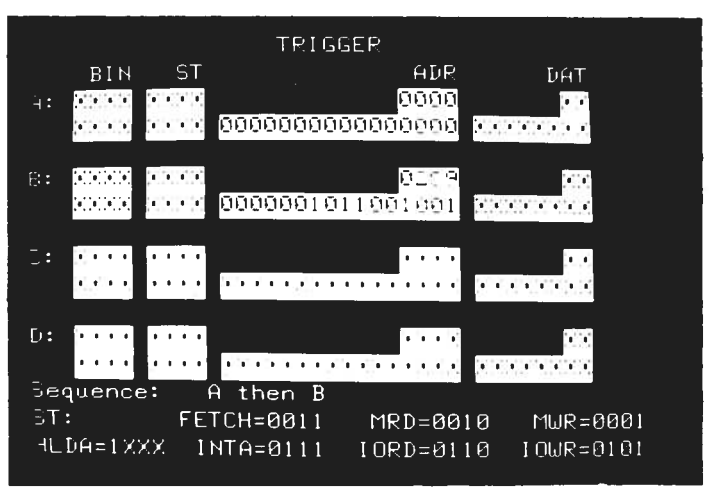
Start data acquisition and press the reset switch.
The test-analyzer must show the following data:

```
STATE   PC    DISASSEMBLY    BUS ACTIVITY
TRIG    0000  JMP   02B4
00003   02B4  LXI   SP,4300
00006   02B7  LXI   H,4200
00009   02BA  LXI   B,0300
00012   02BD  XRA   A
00013   02BE  MOV   M,A     4200<-00
00015   02BF  INX   H
00016   02C0  DCX   B
00017   02C1  CMP   C
00018   02C2  JNZ   02BE
00021   02BE  MOV   M,A     4201<-00
00023   02BF  INX   H
00024   02C0  DCX   B
00025   02C1  CMP   C
Position Cursor: f1       Cursor (f2): slow
```

```
STATE   PC    DISASSEMBLY    BUS ACTIVITY
00026   02C2  JNZ   02BE
00029   02BE  MOV   M,A     4202<-00
00031   02BF  INX   H
00032   02C0  DCX   B
00033   02C1  CMP   C
00034   02C2  JNZ   02BE
00037   02BE  MOV   M,A     4203<-00
00039   02BF  INX   H
00040   02C0  DCX   B
00041   02C1  CMP   C
00042   02C2  JNZ   02BE
00045   02BE  MOV   M,A     4204<-00
00047   02BF  INX   H
00048   02C0  DCX   B
Position Cursor: f1       Cursor (f2): fast
```

- **test 2**

At the test-analyzer, set triggerword A: XXXX XXXX 0000 XX and triggerword B: XXXX XXXX 02C9 XX. Set trigger sequence to "A then B"



quisition and press the reset switch.
lyzer must show the following data:

STATE	PC	DISASSEMBLY		BUS ACTIVITY
TRIG	02C9	LXI	H,4701	
00003	02CC	MVI	M,40	4701<-40
00006	02CE	MVI	M,00	4701<-00
00009	02D0	DCR	L	
00010	02D1	MVI	A,30	
00012	02D3	STA	5303	5303<-30
00016	02D6	RIM		
00017	02D7	ORA	A	
00018	02D8	MVI	M,2A	4700<-2A
00021	02DA	JP	02E4	
00024	02E4	MVI	A,FF	
00026	02E6	STA	44FE	44FE<-FF
00030	02E9	MVI	M,50	4700<-50
00033	02EB	MVI	M,CF	4700<-CF

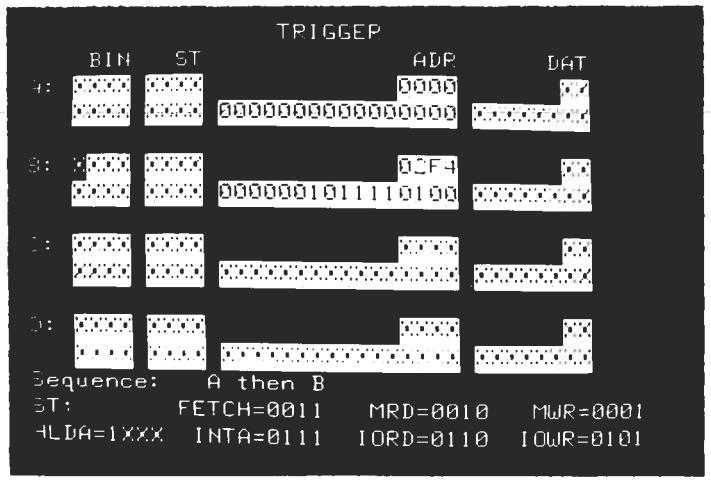
Position Cursor: f1 Cursor (f2): slow

STATE	PC	DISASSEMBLY		BUS ACTIVITY
00036	02ED	MVI	M,43	4700<-43
00039	02EF	INR	L	
00040	02F0	MVI	M,40	4701<-40
00043	02F2	RST	6	42FF<-02 42FE<-F3
00046	0030	JMP	01CB	
00049	01CB	SHLD	44E7	44E7<-01 44E8<-47
00054	01CE	POP	H	42FE->F3 42FF->02
00057	01CF	INX	H	
00058	01D0	PUSH	H	42FF<-02 42FE<-F4
00061	01D1	PUSH	PSW	42FD<-FF 42FC<-00
00064	01D2	DCX	H	
00065	01D3	MOV	A,M	02F3->BA
00067	01D4	LXI	H,0208	
00070	01D7	ADD	A	

Position Cursor: f1 Cursor (f2): fast

- test 3

At the test-analyzer, set triggerword A: XXXX XXXX 0000 XX and triggerword B: XXXX XXXX 02F4 XX. Set trigger sequence to "A then B"



Start data acquisition and press the reset switch.
The test-analyzer must show the following data:

STATE	PC	DISASSEMBLY		BUS ACTIVITY
TRIG	02F4	MVI	A,05	
00002	02F6	STA	449C	449C<-05
00006	02F9	LXI	H,0064	
00009	02FC	SHLD	44CD	44CD<-64 44CE<-00
00014	02FF	LXI	H,4800	
00017	0302	SHLD	42B0	42B0<-00 42B1<-48
00022	0305	MVI	A,0D	
00024	0307	SIM		
00025	0308	EI		
00026	0309	MVI	A,20	
00028	030B	STA	4701	4701<-20
00032	030E	RST	6	42FF<-03 42FE<-0F
00035	0030	JMP	01CB	
00038	01CB	SHLD	44E7	44E7<-00 44E8<-48

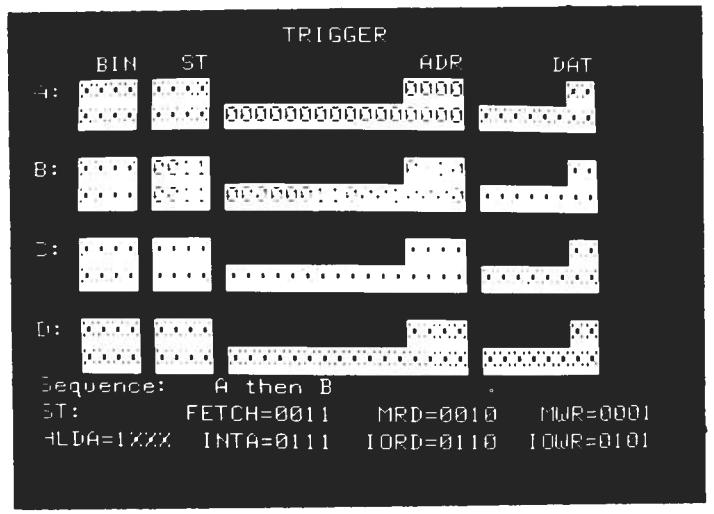
Position Cursor: f1 Cursor (f2): slow

STATE	PC	DISASSEMBLY		BUS ACTIVITY
00043	01CE	POP	H	42FE->0F 42FF->03
00046	01CF	INX	H	
00047	01D0	PUSH	H	42FF<-03 42FE<-10
00050	01D1	PUSH	PSW	42FD<-20 42FC<-54
00053	01D2	DCX	H	
00054	01D3	MOV	A,M	030F->D0
00056	01D4	LXI	H,0208	
00059	01D7	ADD	A	
00060	01D8	JNC		
00062	01DB	LXI	H,603C	
00065	01DE	ADD	L	
00066	01DF	MOV	L,A	
00067	01E0	JNC	01E4	
00070	01E4	MOV	A,M	60DC->57

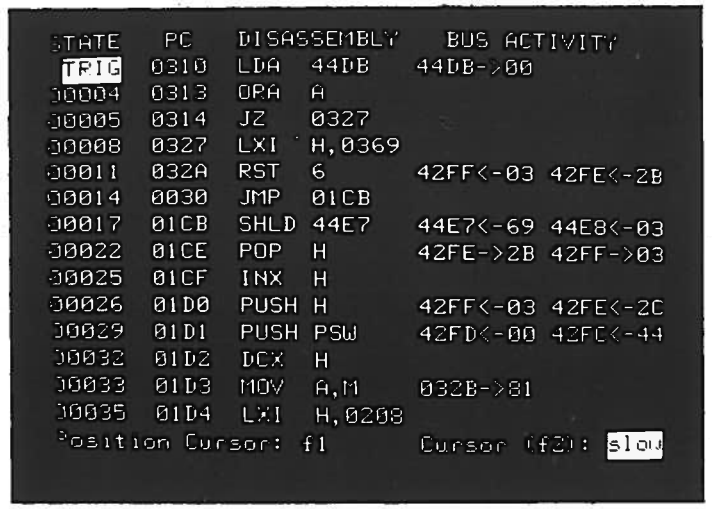
Position Cursor: f1 Cursor (f2): fast

- test 4

At the test-analyzer, set triggerword A: XXXX XXXX 0000 XX and triggerword B: XXXX 0011 0310 XX. Set trigger sequence to "A then B"

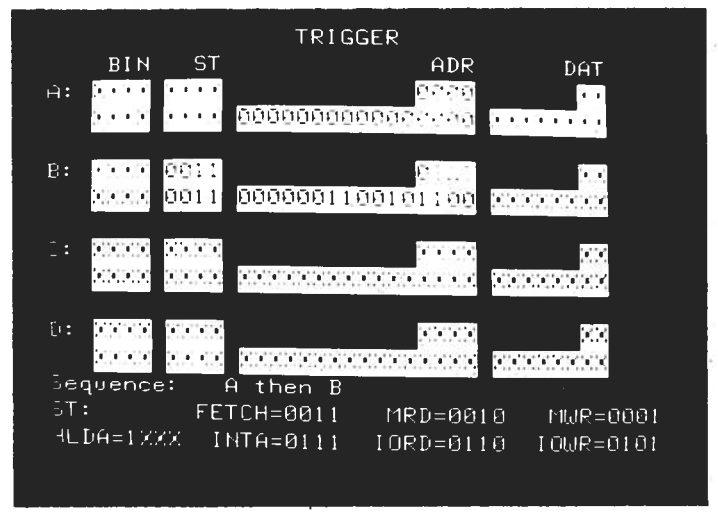


Start data acquisition and press the reset switch.
The test-analyzer must show the following data:



- test 5

At the test-analyzer, set triggerword A: XXXX XXXX 0000 XX and triggerword B: XXXX 0011 032C XX. Set trigger sequence to "A then B"

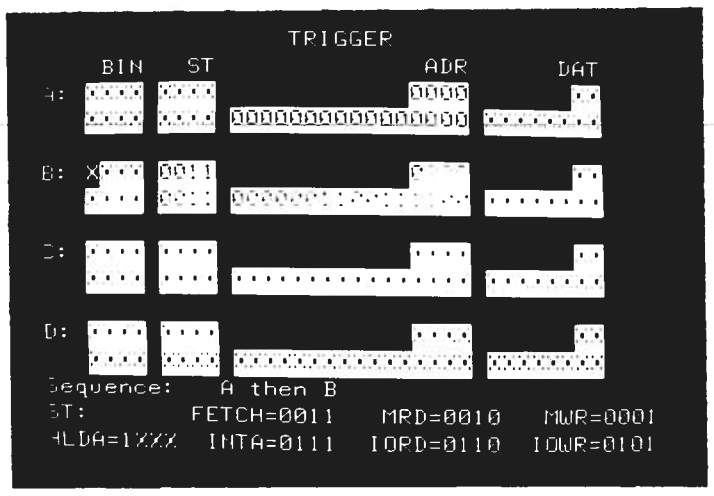


Start data acquisition and press the reset switch.
The test-analyzer must show the following data:

```
STATE   PC    DISASSEMBLY    BUS ACTIVITY
 TRIG  032C  MVI  A,FF
00002  032E  STA  44CC    44CC<-FF
00006  0331  STA  43CF    43CF<-FF
00010  0334  STA  43CE    43CE<-FF
00014  0337  STA  43DC    43DC<-FF
00018  033A  RST  6       42FF<-03 42FE<-3B
00021  0030  JMP  01CB
00024  01CB  SHLD 44E7    44E7<-76 44E8<-03
00029  01CE  POP  H       42FE->3B 42FF->03
00032  01CF  INX  H
00033  01D0  PUSH H       42FF<-03 42FE<-3C
00036  01D1  PUSH PSW     42FD<-FF 42FC<-54
00039  01D2  DCX  H
00040  01D3  MOV  A,M     033B->32
Position Cursor: f1       Cursor (f2): slow
```

- test 6

At the test-analyzer, set triggerword A: XXXX XXXX 0000 XX and triggerword B: XXXX 0011 033C XX. Set trigger sequence to "A then B"



Start data acquisition and press the reset switch.
The test-analyzer must show the following data:

```
STATE   PC    DISASSEMBLY    BUS ACTIVITY
 TRIG  033C  LDA  44C7    44C7->00
00004  033F  ANI  40
00006  0341  JZ   0349
00009  0349  LDA  44A6    44A6->00
00013  034C  STA  44DF    44DF<-00
00017  034F  CALL 0436    42FF<-03 42FE<-52
00022  0436  XRA  A
00023  0437  STA  4300    4300<-00
00027  043A  MVI  A,10
00029  043C  STA  5403    5403<-10
00033  043F  IN   FF        FF->07
00036  0441  ANI  7F
00038  0443  STA  43AB    43AB<-07
00042  0446  CALL 04D3    42FD<-04 42FC<-49
Position Cursor: f1       Cursor (f2): slow
```

```
STATE   PC    DISASSEMBLY    BUS ACTIVITY
00047  04D3  CPI  7F
00049  04D5  RZ
00050  04D6  CPI  08
00052  04D8  JNZ  04E1
00055  04E1  ANI  03
00057  04E3  MOV  C,A
00058  04E4  MVI  A,80
00060  04E6  RLC
00061  04E7  DCR  C
00062  04E8  JP   04E6
00065  04E6  RLC
00066  04E7  DCR  C
00067  04E8  JP   04E6
00070  04E6  RLC
Position Cursor: f1       Cursor (f2): fast
```

```
STATE   PC   DISASSEMBLY   BUS ACTIVITY
00071  04E7  DCR  C
00072  04E8  JP   04E6
00075  04E6  RLC
00076  04E7  DCR  C
00077  04E8  JP
00079  04EB  MVI  B,00
00081  04ED  DCR  A
00082  04EE  MOV  C,A
00083  04EF  JZ
00085  04F2  IN   80        80->F5
00088  04F4  ANI  F8
00090  04F6  ORA  C
00091  04F7  OUT  80        80<-F7
00094  04F9  CALL 050C    42FB<-04 42FA<-FC
Position Cursor: f1       Cursor (f2): fast
```

```
STATE   PC   DISASSEMBLY   BUS ACTIVITY
00099  050C  LDA  8000    8000->AA
00103  050F  XPI  AA
00105  0511  PNZ
00106  0512  INP  B
00107  0513  PUSH D        42F9<-40 42F8<-0D
00110  0514  PUSH B        42F7<-01 42F6<-07
00113  0515  LDA  8001    8001->03
00117  0518  LXI  H,0400
00120  051B  DAD  H
00121  051C  DCR  A
00122  051D  JP   051B
00125  051B  DAD  H
00126  051C  DCR  A
00127  051D  JP   051B
Position Cursor: f1       Cursor (f2): fast
```

```
STATE   PC   DISASSEMBLY   BUS ACTIVITY
00130  051B  DAD  H
00131  051C  DCR  A
00132  051D  JP   051B
00135  051B  DAD  H
00136  051C  DCR  A
00137  051D  JP
00139  0520  LXI  D,8000
00142  0523  XCHG
00143  0524  RST  6       42F5<-05 42F4<-25
00146  0030  JMP  01CB
00149  01CB  SHLD 44E7    44E7<-00 44E8<-80
00154  01CE  POP  H       42F4->25 42F5->05
00157  01CF  INX  H
00158  01D0  PUSH H       42F5<-05 42F4<-26
Position Cursor: f1       Cursor (f2): fast
```

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5.4.4. PM8891 spare parts

NOTE: None of the PM8891 boards are available or repairable via Concern Service.

POSITION NUMBER	DESCRIPTION	ORDERING CODE
8085/Z80 target		
U6	8085A uP	5322 209 86035
U3	74LS373	5322 209 86062
U7	Z80A uP	5322 209 14716
U1	74F00	5322 209 81534
U4	74LS244	5322 209 86017
U2	74LS163	5322 209 85863
Y1	50 MHz osc.	5322 209 71206
VR1	LM340T5	5322 209 84841
CR1	1N914B	5322 130 31487
32 channel test board		
U12,U14,U18,U20	74F244	5322 209 81128
U11,U10,U16,U17	74F138	5322 209 81541
U3	74F109	5322 209 81669
U4	74F00	5322 209 81534
U7	74LS377	5322 209 86258
U2,U9,U23	74F161	5322 209 82001
U6	7407N	5322 209 84761
U15,U13,U19,U21	74F240	5322 209 81127
U8	50 MHz osc.	5322 209 71206
U1	RELAY	5322 280 70267
CR1	1N914B	5322 130 31487

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6. DISASSEMBLY AND RE-ASSEMBLY

WARNING: Before beginning any PM 3632 disassembly:
** Switch-off unit.*
** Disconnect unit from power source (unplug power cord).*
** Disconnect all accessories (pods, rs232c devices etc.).*

- Required tools:
a. Phillips head screw driver.
b. normal screw driver.

When disassembling the PM 3632, you have to proceed in the order given. Re-assembly of the unit is done by following the instructions in the opposite way.

Proceed as follows:

- Remove front and rear panel rims (8 phillips head screws).
- Lift top cabinet plate.

The following subsections describe how to remove the several parts from the PM 3632 mainframe.

To remove the option cards (see figure 6.1) :

- Remove the four phillips head screws that fasten the option card retainer to the mainframe.
- Pull the option cards out of the option slots.

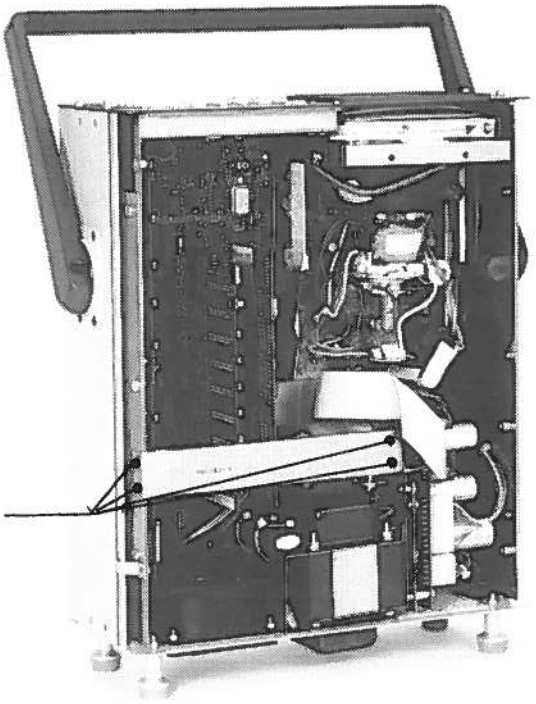

Figure 6.1: Removing the option cards.

To remove frontpanel (see figure 6.2) :

- Remove the four phillips head screws that fasten the keyboard to the sides of the mainframe.
- Disconnect the 16-pin connector which connects the keyboard to the microcomputer board.
- Remove the 2 screws -at the back of the panel- which attach the keyboard to the small bracket inside the mainframe.

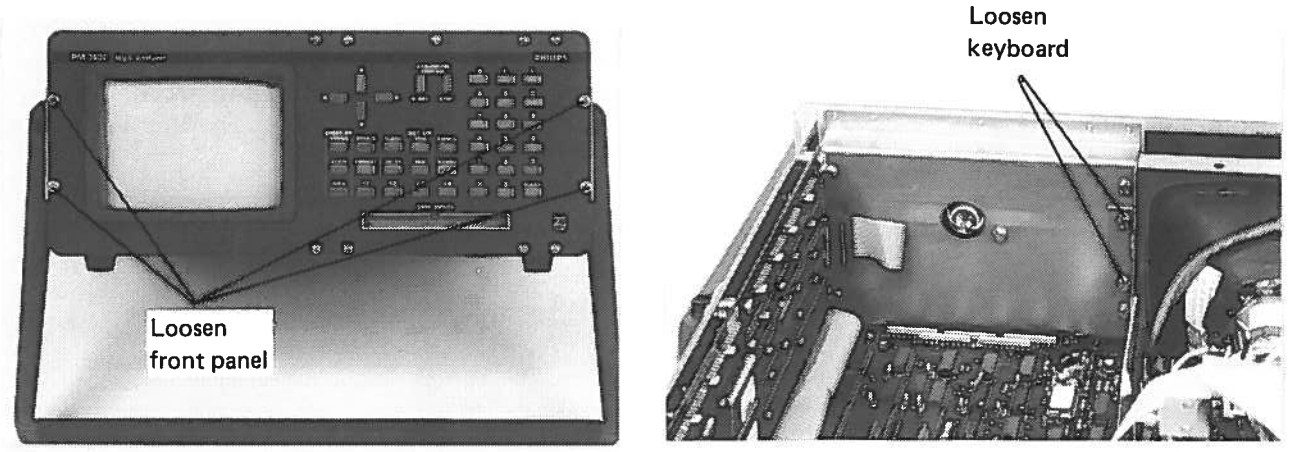

Figure 6.2: Removing the keyboard.

To remove the capture board (see figure 6.3):

- Remove the front panel.
- Remove the option cards (if not installed, only remove option card retainer).

NOTE: Do not mix-up the screws that fasten the capture board to the side of the mainframe with those that fasten the capture board to the bottom of the mainframe.

- Remove all the screws that fasten the capture board (microcomputer part) to the side of the mainframe.
- Remove all the screws that fasten the capture board (data acquisition part) to the bottom of the mainframe.
- Carefully shift the capture board to the front of the PM 3632, until it comes out.

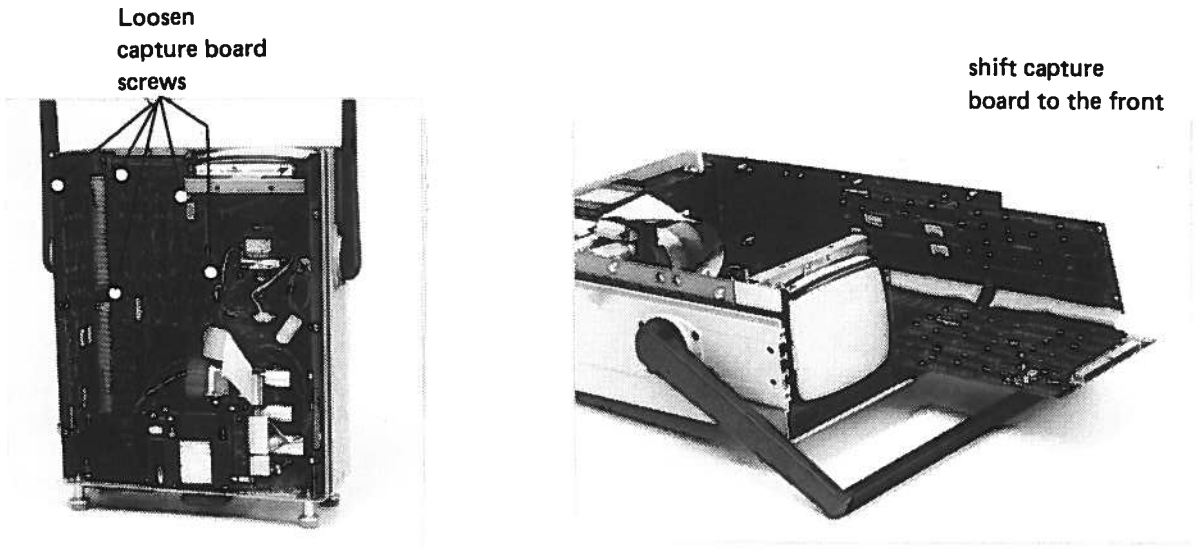

Figure 6.3: Removing the capture board.

Removing the CRT unit (see figure 6.4) :

- Remove the four screws that fasten the four feet of the PM 3632 to the bottom.
- Remove the bottom cover.
- Remove the four screws that fasten the CRT unit to the bottom of the mainframe.
- Shift the CRT unit to the front till you can reach the connector at the end of the unit.
- Remove the connector from the CRT unit.
- Shift the CRT unit further to the front of the PM 3632 until it comes out.

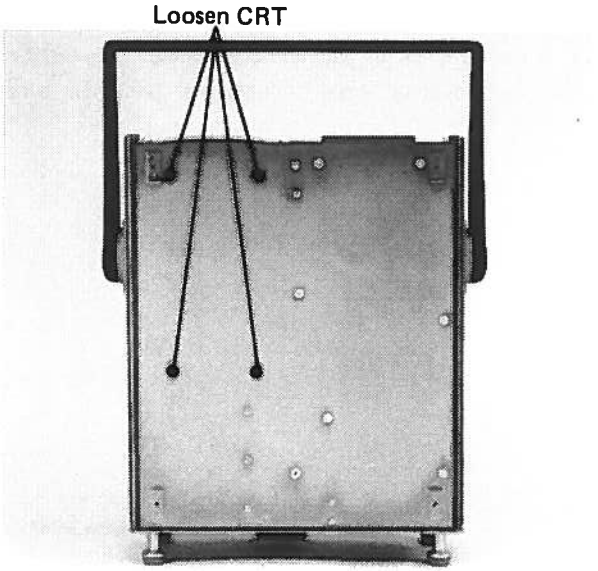

Figure 6.4: Removing the CRT unit.

Removing the back panel + power supply (see figure 6.5.) :

- Remove the four screws that fasten the four feet of the PM 3632 to the bottom.
- Remove the bottom cover.
- Loosen the five screws that fasten the back panel + transformer to the bottom of the mainframe.
- Remove the four phillips head screws that fasten the back panel to the sides of the mainframe.
- Loosen the green/yellow earth wire from the bottom plate of the mainframe.

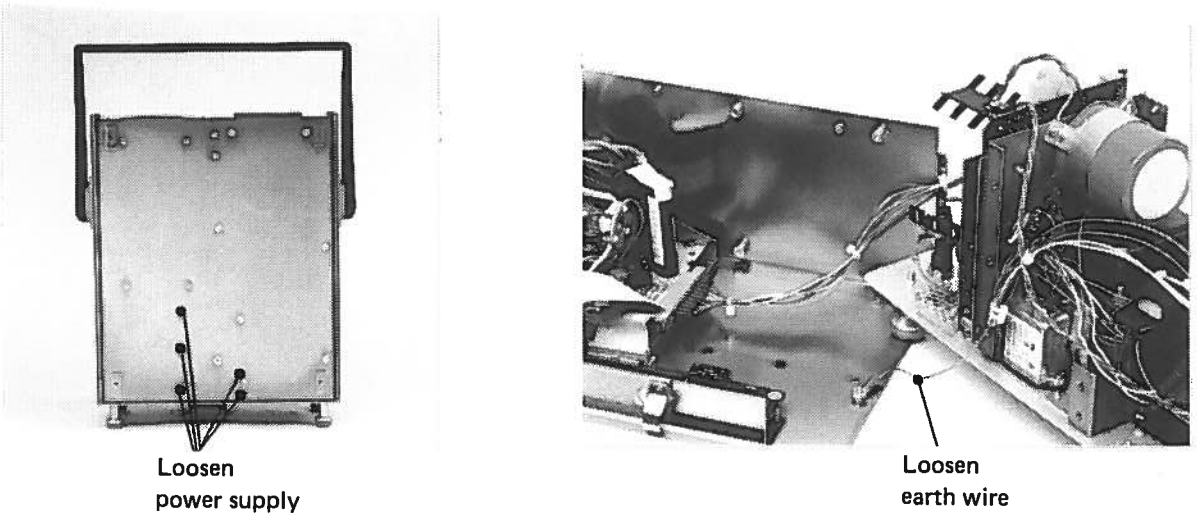

Figure 6.5: Removing the back panel + power supply.

Removing the power supply from the back panel (see figure 6.6.) :

- Remove back panel + power supply from the mainframe.
- Loosen connectors J1, J2 and J3 at the power board.
- Remove the four screws that fasten the power board to the power control board.
- Remove one screw that fastens the power control board to the transformer.
- Take the two power supply boards apart (these boards are only connected to each other by J4).

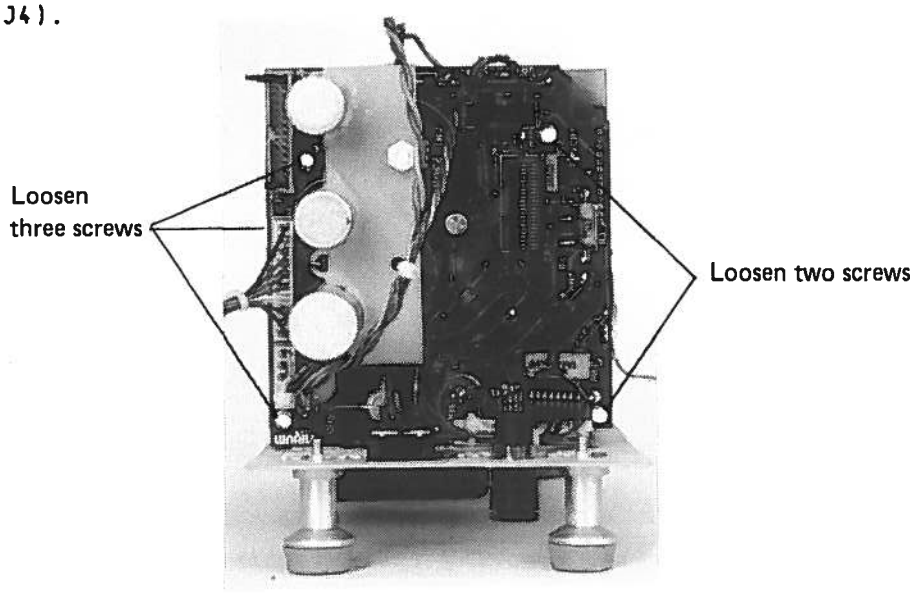

Figure 6.6: Removing the power supply from the back panel.

Removing the back panel from the mainframe (see figure 6.7.) :

- Remove the four phillips head screws that fasten the back panel to the sides of the mainframe.
- Remove the two screws that fasten the back panel to the transformer.
- Carrefully pull the back panel out from the unit.

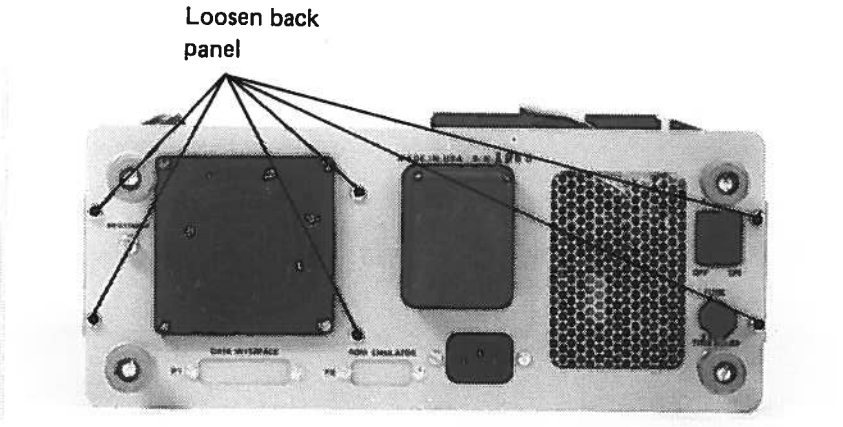

Figure 6.7: Removing the back panel.

Removing the transformer :

- Remove the back panel + power supply from the mainframe.
- Remove the two screws that fasten the transformer to the back panel (see figure 6.7).

Removing the fan from the back panel (see figure 6.8) :

- Remove the back panel from the mainframe.
- Remove the four screws that fasten the fan to the back panel.

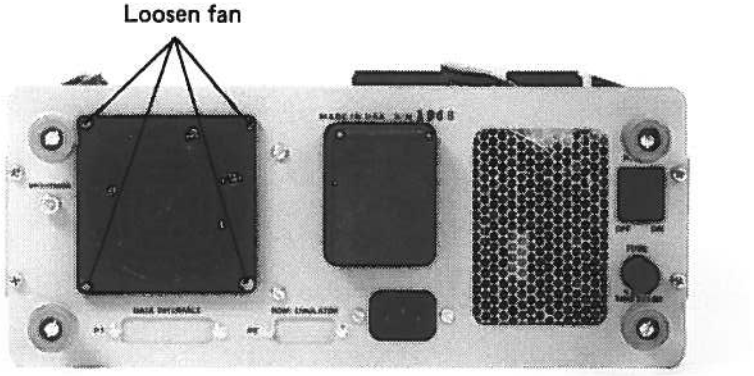

Figure 6.8: Removing the fan.

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7. *INSTALLATION INSTRUCTIONS*

7.1 PREPARATIONS FOR USE

Mains Voltage

The PM 3632 as it is, has been provided for two mains voltages: 220 V and 240 V.

Setting for the mains voltage is done with two Faston colored-wire connections, located near the power supply transformer in the instrument.

220V

White/brown --><-- Blue

White/orange --><-- White

240V

White/brown --><-- White

White/orange --><-- Blue

(the white wire is a non-connected dummy wire)

If required the PM 3632 can be adopted for the voltages 100, 110, 120, 127, 200 or 250 V. These settings however are more difficult to change, because all connections are crimped conections.
To set the PM 3632 to one of these settings, proceed as follows:

- switch-off the instrument.
- remove the top and bottom covers (4 screws)
- remove back panel (4 screws in back panel, 5 screws in bottom of mainframe and one earth wire).
- refer to figure 7.1 for exact color codes of the transformer wires.

WARNING: WHEN CHANGING THE SETTINGS TO ONE WHICH CAN NOT BE ACCOMPLISHED USING THE FASTONS (220V or 240V), YOU MUST USE CRIMPED CONNECTIONS AGAIN!!

- After changing the settings, re-assemble the mainframe again.

Mains frequency

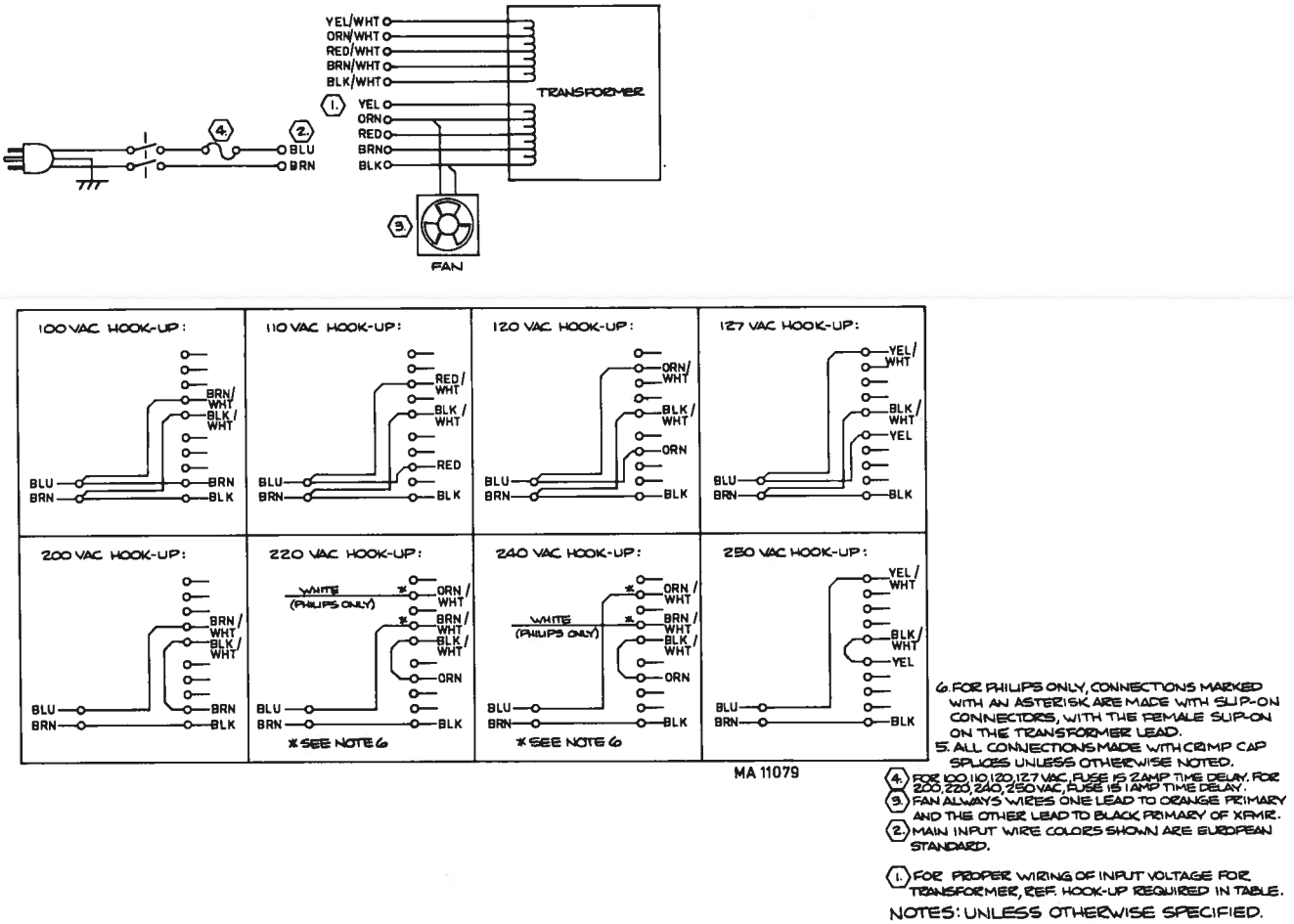
There are two jumpers depending on the mains frequency; they are both located on the main p.c.board.
Because there are two different p.c. board revisions in the field, the jumper setting is described in two figures (7.2 and 7.3).

Note: instruments with a serial number 1850 or higher, and instruments which have been in a workshop for repair are set to 50 Hz mains always. This can not be changed anymore by changing the two jumpers. If necessary, a hardware modification can be done: to set the instrument to a 60 Hz mains, just exchange the option and video frequencies at jumper JP2 and set jumper JP1 to the 60 Hz position. (see also fig. 2.7).

Mains fuse

The value of the mains fuse is depending on the mains voltage:
  110...127V : 2 Amps (delayed) 5x20mm, glass tube.
  200...250V : 1 Amp (delayed) 5x20mm, glass tube.
This fuse is located in the rear panel of the instrument.

NOTE: When removing the fuse, first switch-off the instrument!



6. FOR PHILIPS ONLY, CONNECTIONS MARKED WITH AN ASTERISK ARE MADE WITH SLIP-ON CONNECTORS, WITH THE FEMALE SLIP-ON ON THE TRANSFORMER LEAD.
5. ALL CONNECTIONS MADE WITH CRIMP CAP SPLICES UNLESS OTHERWISE NOTED.
4. FOR 100,110,120,127 VAC, FUSE IS 2AMP TIME DELAY. FOR 200,220,240,250 VAC, FUSE IS 1 AMP TIME DELAY.
3. FAN ALWAYS WIRES ONE LEAD TO ORANGE PRIMARY AND THE OTHER LEAD TO BLACK PRIMARY OF XFMR.
2. MAIN INPUT WIRE COLORS SHOWN ARE EUROPEAN STANDARD.
1. FOR PROPER WIRING OF INPUT VOLTAGE FOR TRANSFORMER, REF. HOOK-UP REQUIRED IN TABLE.

NOTES: UNLESS OTHERWISE SPECIFIED.

Figure 7.1: Mains voltage setting.

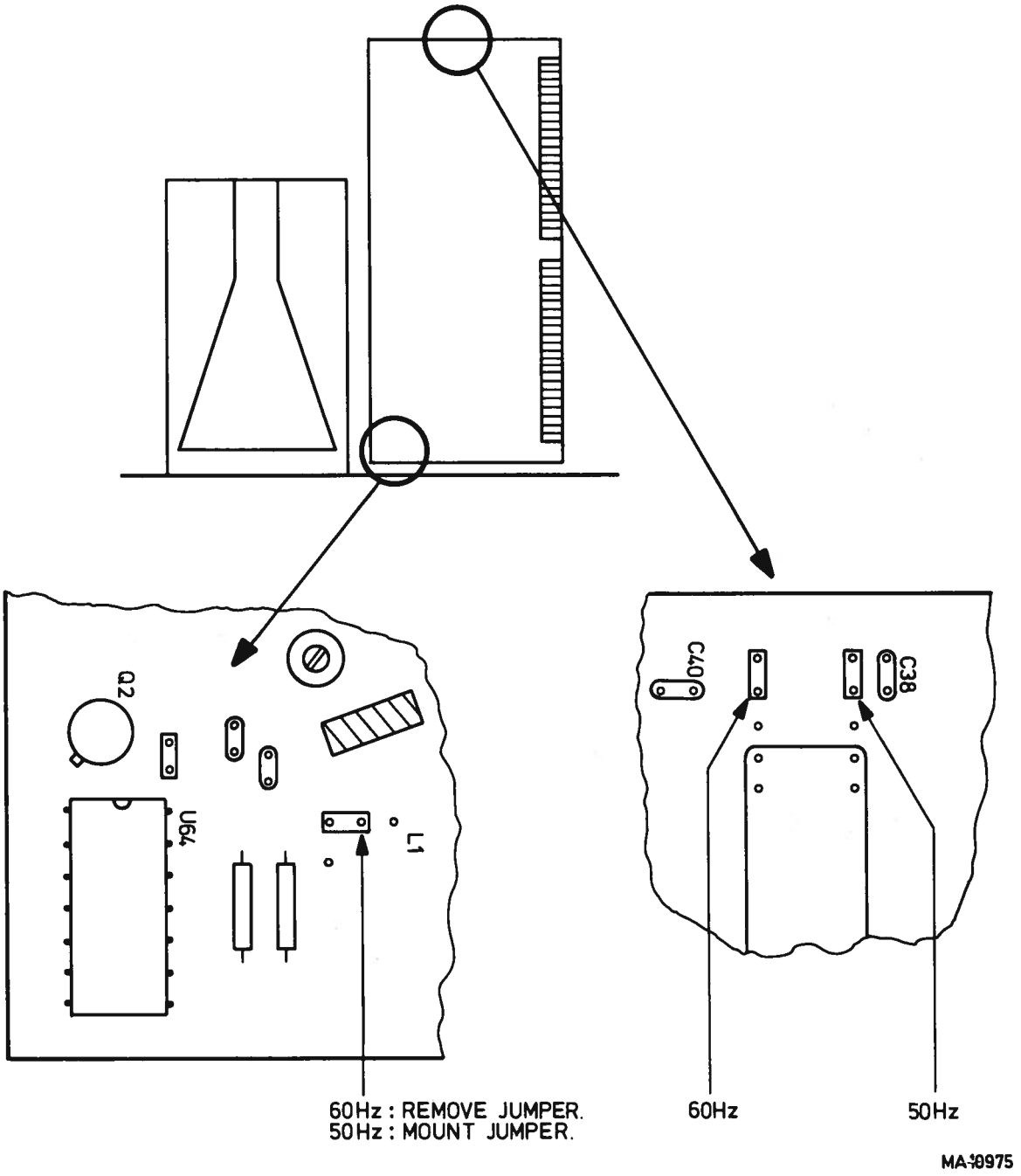


Figure 7.2: Jumper settings related to the mains frequency. (board rev. 8).

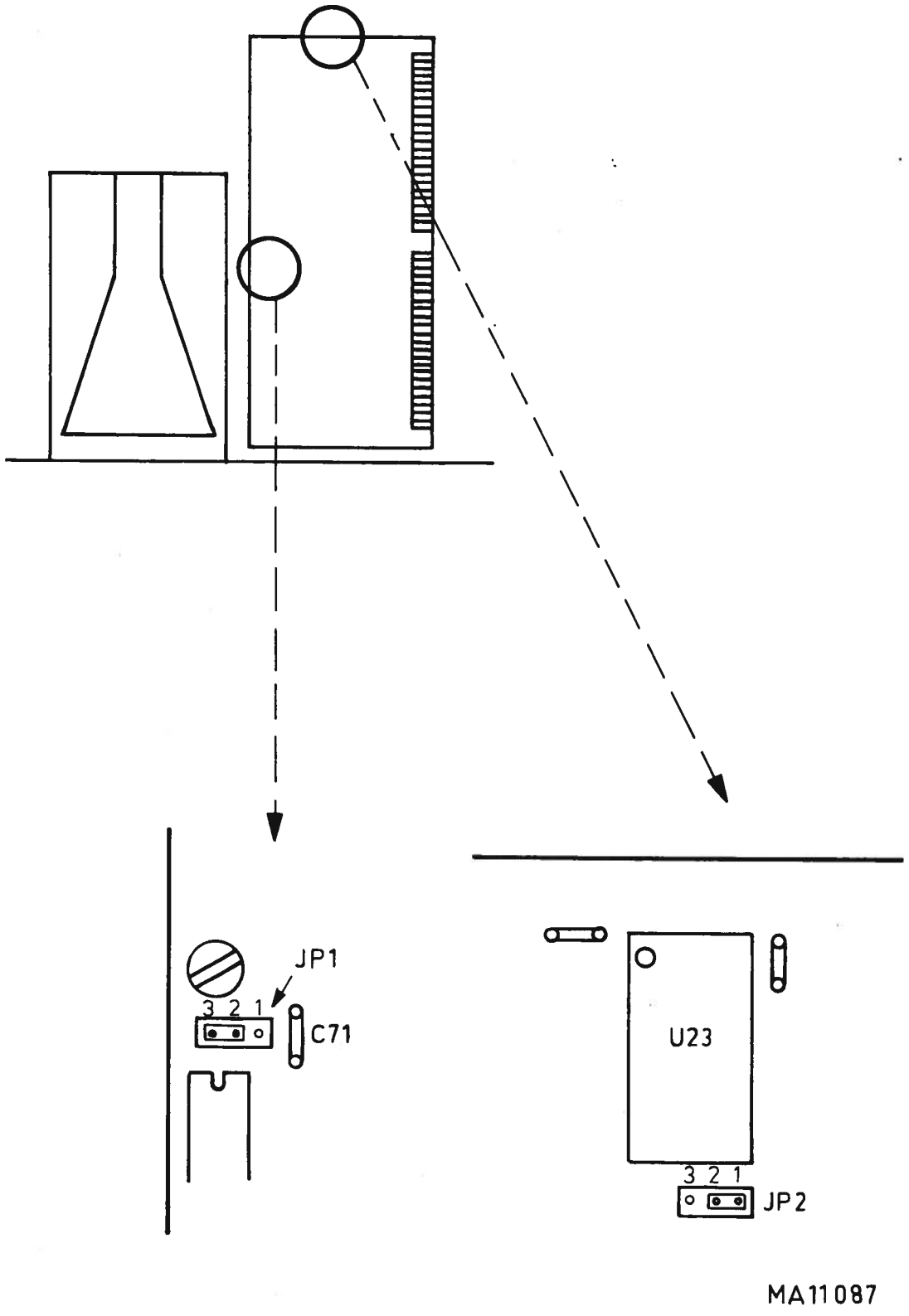


Figure 7.3: Jumper settings related to the mains frequency. (board rev. C).

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7.2 BUILDING-IN THE OPTIONS

Inside the PM 3632 on the main p.c.board there are three slots to accomodate the option boards.
Be sure to disconnect the instrument from the mains voltage before any building-in action is taken.

General Procedure

- Remove both, the front panel- and the rear panel rims (eight screws).
- Lift the top cabinet plate.
- Remove the retainer bracket which is mounted over the main p.c. board, above the option slots (4 screws).
- install option board (see below).
- Mount the bracket to secure the option unit(s).
- Fix the top cabinet plate.
- Fix both the front panel- and the rear panel rims.

NOTE: However any option can be installed in any slot, the installation instructions below give a preferred location for every option card.

RS-232C Communication Card PM 8880/20

This card, which is used with Data-Transfer and with Rom-Emulation, is not field-installable.
Also the PM 8880/00, which consists of the Rom Emulator Pod and the RS 232-C Communication card is not field-installable.
For this option, two flat cables have to be built-in; one 15 pole (for rom emulator) and one 25 pole (for RS232C transfers).
When building-in this card, proceed as follows:
- remove the back panel from the mainframe (6 screws).
- remove the P1 and P2 protection plates from the back panel.
- put the 15 pole flat cable under the transformer, as shown in figure 7.4.
- fasten the 15 pole connector in P2 (2 screws).
- fasten the 25 pole connector in P1 (2 screws).
- fasten the back panel to the mainframe again.
- put the 40 pole connector that combines the 15 and 25 pole flat cables in connector J2 on the RS232C control card.
- install the RS232C control card in the most left-hand slot (when standing in front of the PM 3632).
- follow the general procedure as described above.

Disassembly Rom board PM 8880/30

Mount this unit in the right-hand side slot on the main p.c. board (when standing in front of the PM 3632).
- follow the general procedure as described above.

For each specific Microprocessor Pod the corresponding Disassembly Prom must be located on this unit.

Microprocessor Prom

Included with each Microprocessor Pod is a Prom used for disassembly.
These Proms must be located on the Disassembly Rom board (PM 8880/30).
Prom location:
Proms type 2732 and type 2764 may be located in any socket (U1--8) on this board.
Proms type 27128 may only be located in sockets U5--8..

Set-up/and Data memory board PM 8880/40/50

Mount this unit in the centre slot on the main p.c. board.
- follow the general procedure as described above.

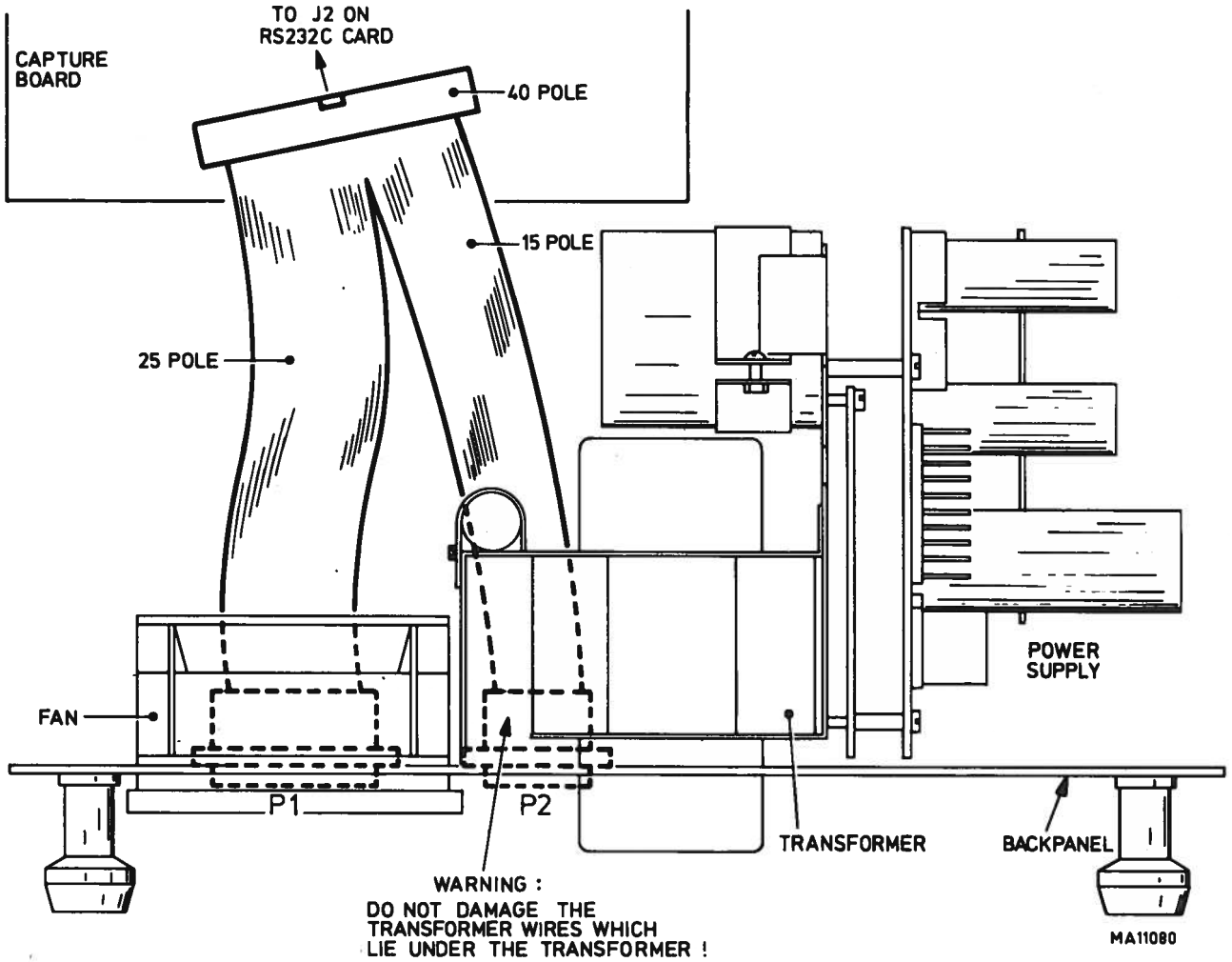

Figure 7.4: RS232C control card installation.

7.3 BUILDING-IN THE VIDEO OUTPUT

This card, which is used to generate a composite video signal, is not field installable. It has to be done in the workshop.

For this, you need the following tools:

- screw driver (normal)
- screw driver (Phillips head)
- spanner 8 mm
- spanner 10 mm
- drilling machine
- drill 13 mm

Proceed as follows:

1. Switch-off the instrument.
2. Remove both, the front- and rear panel rims (8 screws).
3. Lift the top cabinet plate.
4. Remove the retainer bracket which is mounted above the option boards (4 screws, see figure 7.5).

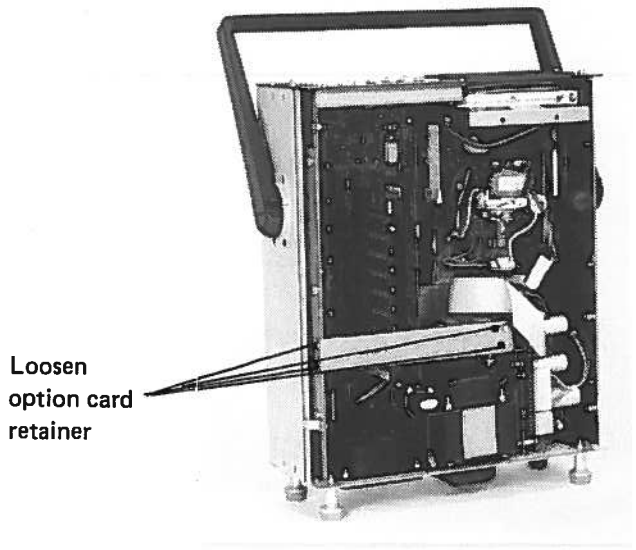

Figure 7.5: Removing the option card retainer.

5. Remove the option boards from the option slots.
6. Remove the bottom cover (4 screws + feet).
7. Remove the rear panel (5 screws in bottom plate (see figure 7.6).

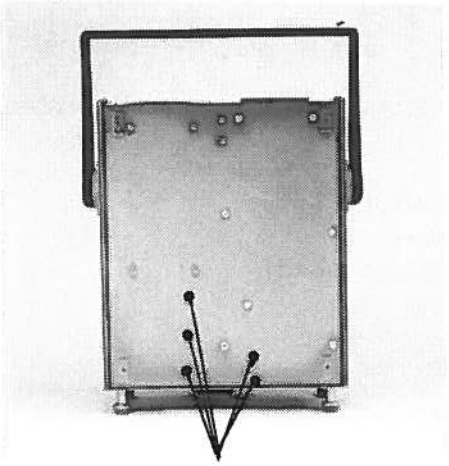

Figure 7.6: Removing the rear panel.

8. Loosen the earth wire that connects the power supply to the bottom of the mainframe (see figure 7.7).

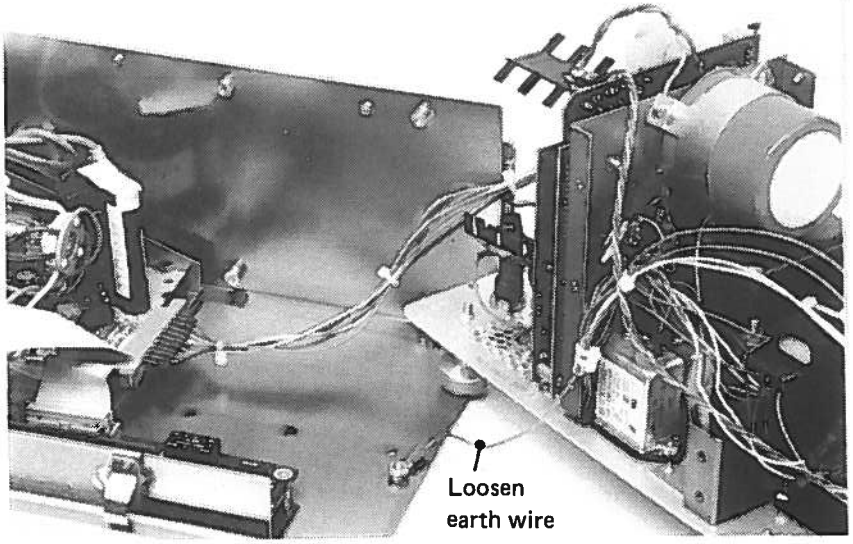

Figure 7.7: Loosen the earth wire.

9. Disconnect, on both sides, the connector that connects the power supply to the CRT

10. Drill a 13 mm hole in the rear plate, just under the external brightness potentiometer (see figure 7.8). REMOVE ALL METAL RESTS!!!

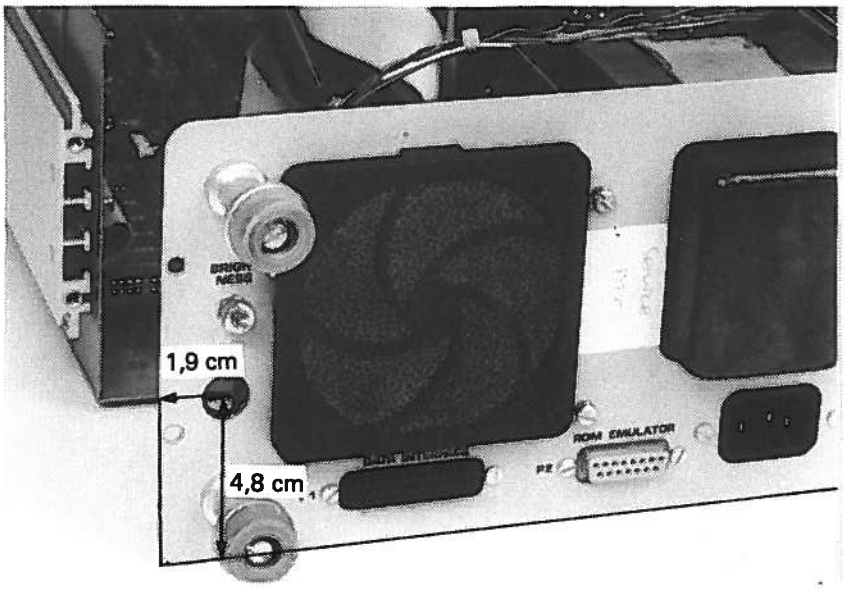

Figure 7.8: Position of new BNC plug.

11. When fastening the BNC plug in the rear plate, take care that the insulating rings insulate the BNC plug from the mainframe.
    Fasten the BNC plug.

12. When fastening the video output card, be careful not to squeeze any cables that lead to the transformer.
    Fasten the video output card to the bottom two holes of the fan (see figure 7.9)

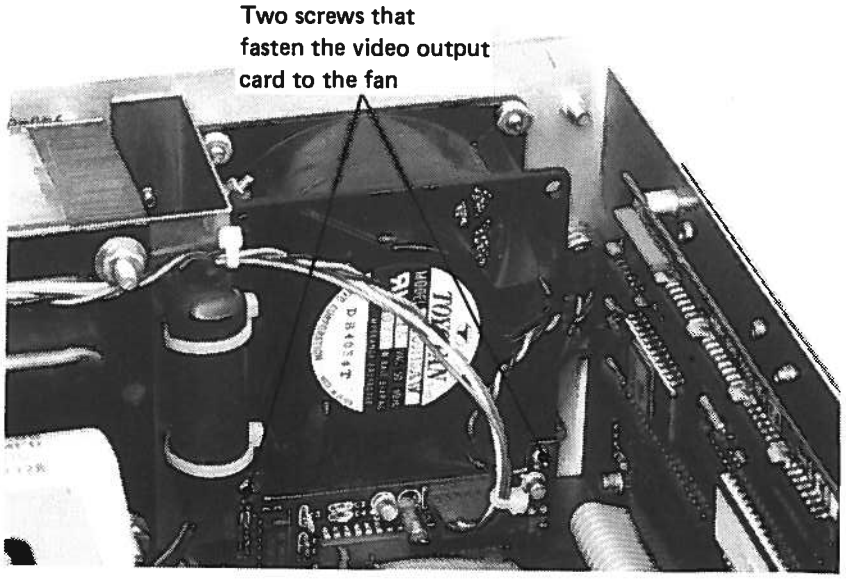

Figure 7.9: Position of video output card.

13. Solder the twisted wires (red and black) to the BNC connector (see figure 7.10):
    red = video signal out
    black = ground

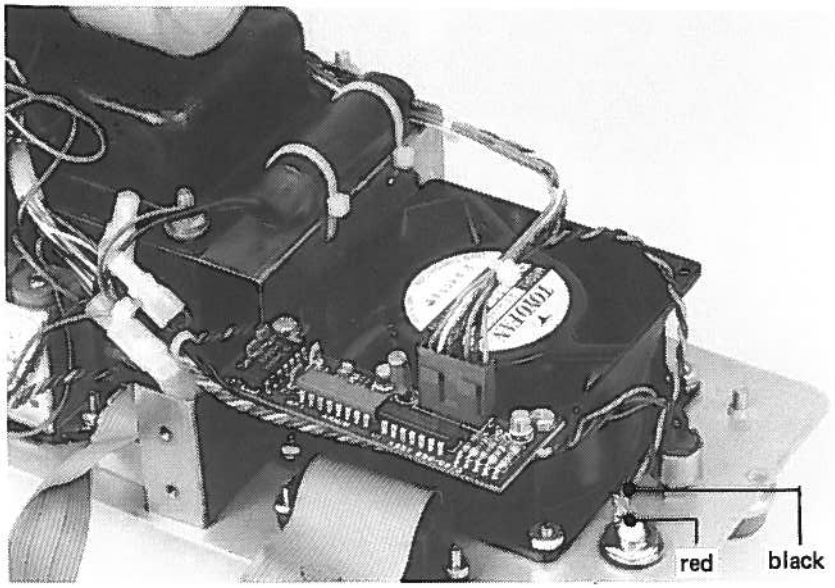

Figure 7.10: Connections to BNC plug.

14. Solder the twisted wires (grey and black) to the pins on the CRT connector that will connect these two wires to the grey and black wires that come from the power supply (see figure 7.11)
    grey = video input signal, must be connected to pin 8 of CRT board connector eventually
    black = ground, must be connected to pin 10 of the CRT board connector eventually

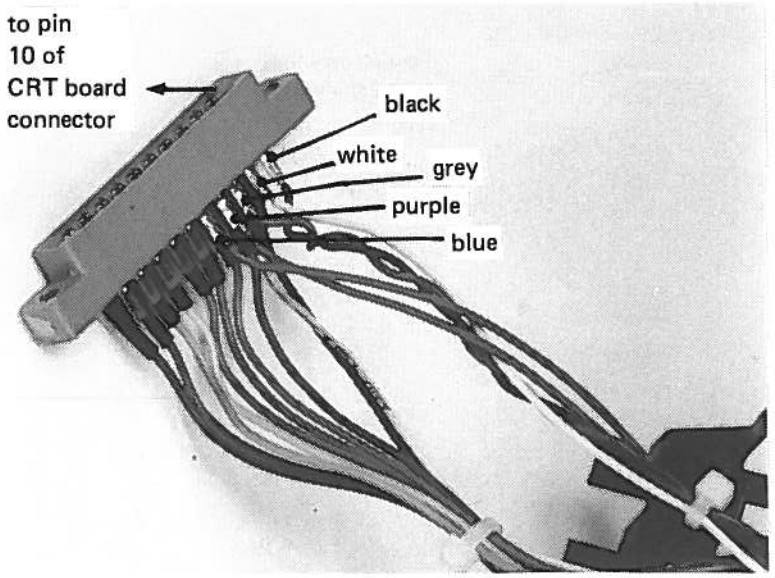

Figure 7.11: Connections from video output card to CRT connector.

15. Solder the white wire to the pin on the CRT connector that will connect this wire to the white wire that comes from the power supply (see figure 7.11)
    white = signal VRTC, must be connected to pin 9 of CRT board connector eventually

16. Solder the purple wire to the pin on the CRT connector that will connect this wire to the purple wire that comes from the power supply (see figure 7.11)
    purple = +12 V, must be connected to pin 7 of CRT board connector eventually

17. Solder the blue wire to the pin on the CRT connector that will connect this wire to the blue wire that comes from the power supply (see figure 7.11)
    blue = signal HRTC, must be connected to pin 6 of CRT board connector eventually

18. Fasten CRT connector to CRT board again (the black wire must connect to pin 12)

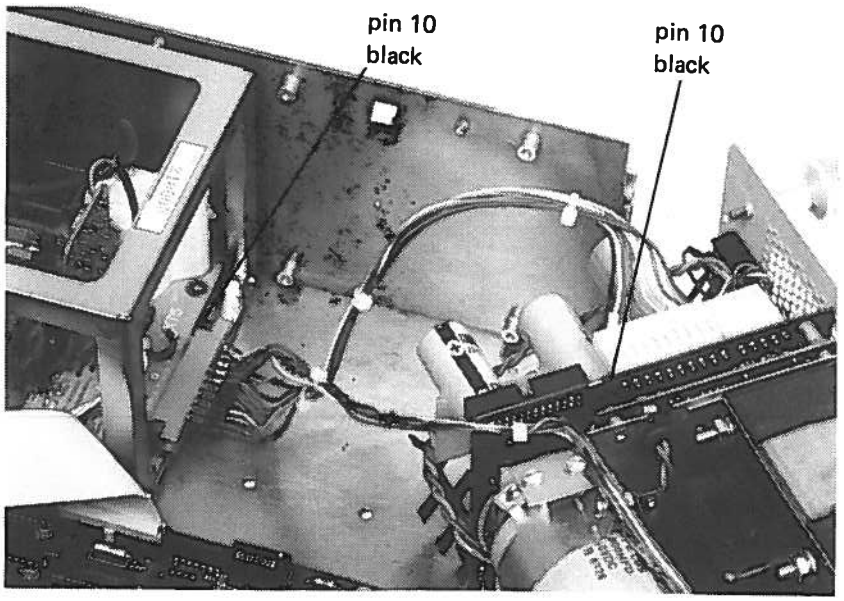

Figure 7.12: Position of CRT connector.

19. Fasten the other connector on this cable set to the power supply connector (J2, black is pin 12).

20. Connect the ground wire of the power supply to the bottom of the mainframe again.

21. When fastening the rear panel to the mainframe, be careful not to squeeze any wires which lie under the transformer.
    If the RS232C control card is installed, then the 25 pole flat cable must go under the video output card (see figure 7.13).
    Fasten the rear panel again to the mainframe (5 screws in bottom plate).

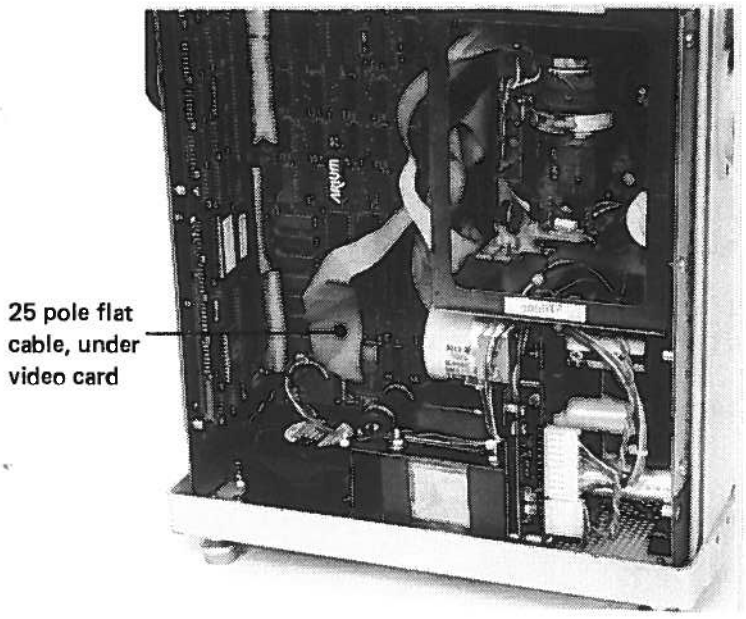

Figure 7.13: Fastening the rear panel.

22. Put the cable set of the video output card, that lead to the CRT, under the upper two screws of the transformer (see figure 7.14).

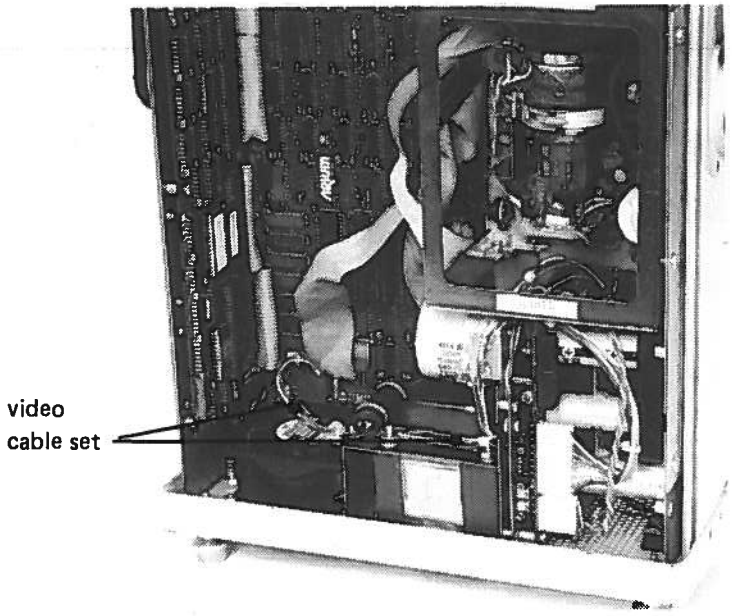

Figure 7.14: Fixing the video card cable set.

23. Connect any monitor which needs a composite video signal to the analyzer and switch-on. The status menu must be visible on the monitor now. If the status menu does not appear, then check all the connections which you have just made. If these are correct, check video output card.

24. Switch-off the instrument.

25. Fasten the bottom cover to the mainframe again (4 screws + feet)

26. Install option cards again

27. Fasten the option card retainer again (4 screws).

28. Put top cover back on instrument.

29. Fasten front and rear panel rims again (4 screws).

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NOTES:

NOTES:

APPENDIX A

List of checksums of all proms used in the PM 3632 mainframe and options.

Indication on proms:				Checksum:
Mainframe, english	Software revision	K	; PH K0 and K81 4100	F528 and 16C1
		L	; M4P00-L and M4P01-L	A261 and 5B86
Mainframe, french	Software revision	L	; M4F00-L and M4F01-L	3EB8 and 3F5A
Character gen.	Software revision	F	; REV. F, BIGCHR	69DD
		G	; MCH01-G	69DD
Set up memory,	Software revision	B	; REV. B, SM080	A6B7
		B	; MSM00-B	A6B7
Setup Data memory,	Software revision	B	; REV. B, AB032	A5B8
		B	; MA800-B	A5B8
		C	; MA800-C	BDDD
RS 232C comm. card,	Software revision	G	; REV. G, ROMEMU	C08C
		H	; REV. H, ROMEMU	2193
		H	; MRE00-H	2193
PM 8865 disa,	Software revision	E	; REV. E, NDISIN	3787
		E	; MIN00-E	3787
		F	; MIN00-F	EF30
PM 8866 disa,	Software revision	B	; REV. B, DS6800	F91B
		B	; M6800-B	F91B
		C	; M6800-C	F8F8
PM 8867 disa,	Software revision	D	; REV. D, DS6809	35BA
		D	; M6900-D	35BA
		E	; M6900-E	25D5
		F	; M6900-F	9F45
PM 8868 disa,	Software revision	C	; REV. C, DS6502	6E17
		C	; M6500-C	6E17
PM 8869 disa,	Software revision	H	; REV. H, Z80	996C
		J	; REV. J, Z80	863B
		J	; MZ800-J	863B
		K	; MZ800-K	F24A
PM 8870 disa,	Software revision	A	; REV. A, NSC800	00A8
		A	; M8N00-A	00A8
PM 8874	Software revision	B	; M6K00-B	2F70
PM 8876	Software revision	A	; M8600-A	E58B
Triggerprom for 16-bit disa's, revision		A	; MT600-A	D2F3

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APPENDIX B

This appendix contains the checking procedures to check proper working of the PM 3632 and its options.

Necessary tools:

- Pulse generator
  - 50 MHz
  - Minimum pulse: 5 nsec
- Wordgenerator
  - 50 MHz
  - 8 channels
- Oscilloscope (100 MHz)
- Multimeter
- Prom programmer with rs232c communication facility
- 8085/Z80 demo unit (included in PM 8891, diagnostic tool kit)

PM 3632 MAINFRAME

1. Initial set-up:
   - A. Connect 8085 disa pod to PM 3632 and switch-on.
   - B. On format screen, set — pod mode = 8085
   - C. On trigger screen, set — A: STS = 0011 ADR = 004E
   - D. On sequence screen, set — Seq = "A" (0)
   - E. On configuration screen, set — data qaulification = off

2. State data capture and trigger:
   - A. Connect 8085 disa pod to 8085 uP on demo unit.

   NOTE: Instead of the 8085/Z80 demo unit, any other target system can be used. For other targets however, you must adopt the state lists shown in these checking procedures.

   - B. Switch-on 8085/Z80 demo unit.
   - C. On demo unit, press switch 1, once
     switch 2, twice
   - D. Press START.
   - E. On demo unit, pres switch 1, once.
   - F. The PM 3632 must trigger now.
   - G. Press STATE.

H. The display must show the following data:

ADR	DAT
004E	C3
004F	00
0050	01
0100	0B
0101	00
0000	FF
0102	E6
0103	01
0104	CA
0105	2A
0107	0B
0108	00
0000	FF
0109	E6

I. On trigger screen, set B: ADR = 004F
C: ADR = 0050
D: ADR = 0100

J. On sequence screen, set Seq = "E" (A then B then C then D).

K. Press START.

L. On demo unit, press switch 1 twice.

M. The display must show the following data:

ADR	DAT
0100	0B
0101	00
0000	FF
0102	E6
0103	01
0104	CA
0105	2A
0107	0B
0108	00
0000	FF
0109	E6
010A	02
010B	C2
010C	80

N. On sequence screen, set Seq = "A" (0)

O. On configuration screen, set Data qual = "Comb"
Combi qual = "Only"
"0"

P. On trigger screen, set D: ADR = 01XX

Q. Press START.

R. On demo unit, press switch 1 twice.

S. The display must show the following data:

ADR	DAT
0100	00
0100	D8
0101	00
0102	E6
0103	01
0104	CA
0105	2A
0107	DB
0108	00
0109	E6
010A	02
010B	C2
010C	80
0100	01

T. On configuration screen, set Combi qual = "all but"

U. On trigger screen, set 0: STS = 0011 ADR = 0100

V. Press START.

W. On demo unit, press switch 1 twice.

X. The display must show the following data:

ADR	DAT
004E	C3
004F	00
0050	01
0101	00
0000	FF
0102	E6
0103	01
0104	CA
0105	2A
0107	DB
0108	00
0000	FF
0109	E6
010A	02

Y. On configuration screen, set Data qual = "state"
State qual enable on = "C"
disable on = "D"

Z. On trigger screen, set C: STS = 0011 ADR = 0104

AA. Press START.

AB. On demo unit, press switch 1 twice.

AC. The display must show the following data:

ADR	DAT
004E	C3
004F	00
0050	01
0100	D8
0104	CA
0105	2A
0107	DB
0108	00
0000	FF
0109	E6
010A	02
010B	C2
010C	80
0100	01

3. Timing data capture and trigger

A. Switch-off the PM 3632, and connect PM 8860 32-channel logic pod.

NOTE: When connecting the 32-channel logic pod to the word generat data channels 0, 1, 2 and 3 and the clock and qualifier chan must be twisted with a ground lead.

B. Connect the 32 channels to the word generator, in the following way:

channels:	word gen. output:
0, 8, 16, 24	1
1, 9, 17, 25, qualifier	2
2, 10, 18, 26	3
3, 11, 19, 27	4
4, 12, 20, 28	5
5, 13, 21, 29	6
6, 14, 22, 30	7
7, 15, 23, 31	8
Clock	clock
6 ground leads	ground

C. Set the clock of the word generator to a repetition time of 80 nsec.

D. Set the word generator to generate the following pattern:

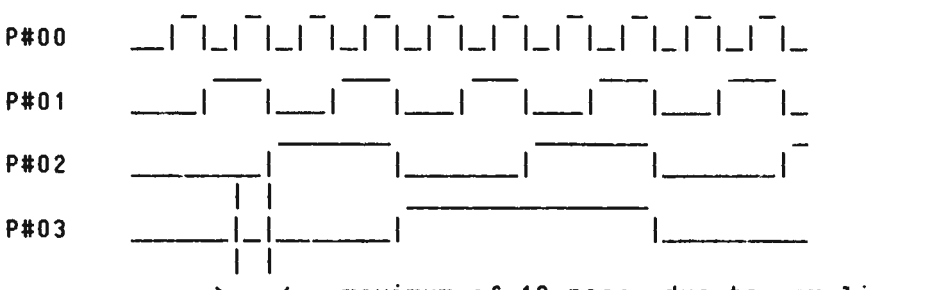
0000 0000
0001 0001
0010 0010
0011 0011
0100 0100
0101 0101
0110 0110
0111 0111
1000 1000
1001 1001
1010 1010
1011 1011
1100 1100
1101 1101
1110 1110
1111 1111

E. On delay screen, set Delay = 1000

F. On clock screen, set Period = 10 nsec

G. Press START.

H. On channels 0 ... 3, a counter pattern must be visible.

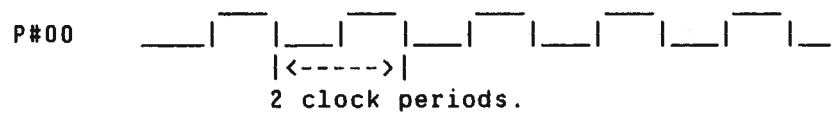


I. On clock screen, set Source = external
Edge = rising

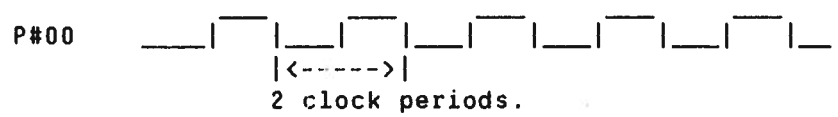
J. Press START.

K. Press f3 on PM 3632.

L. Channel 0 (P#00) must be a square wave, with two sampling clocks in one period.



M. On clock screen, set Edge = falling
N. Press START.
O. Channel 0 (P#00) must be a square wave, with two sampling clocks in one period.



P. On clock screen, set Edge = falling
Qual = low
Q. Press START.
R. On probe 1 (P#01), the dispayed signal must be low continously.
S. On clock screen, set Qual = high
T. Press START.
U. On probe 1 (P#01), the displayed signal must be high continously.
V. Set word generator to generate the following pattern (walking zero):
Repetition time for clock = 80 nsec.

```
11111110
11111101
11111011
11110111
11101111
11011111
10111111
01111111
11111110
```

W. On format screen, set Pod = LOGIC32
X. Press START.
Y. Check for walking zero on all 32 channels.
Z. Set word generator to generate the following pattern (walking ones):
Repetition time for clock = 80 nsec

```
00000001
00000010
00000100
00001000
00010000
00100000
01000000
10000000
00000001
```

AA. Press START.
AB. Check for walking one on all 32 channels.
AC. Run selftest programs (special functions 1).
The PM 3632 must pass for all tests.
AD. Measure the threshold voltage at pin 19 of the 20 pole pod connector.
The voltage must be:
In TTL position: 1.4 V +/- 0.1 V
In VAR position: -9 V ... +9 V selectable

1. Initial setting.

   A. Connect PM 8860 to PM 3632 and switch-on.

   B. Set word generator to generate the following pattern:
   Repetition time for clock = 20 nsec.

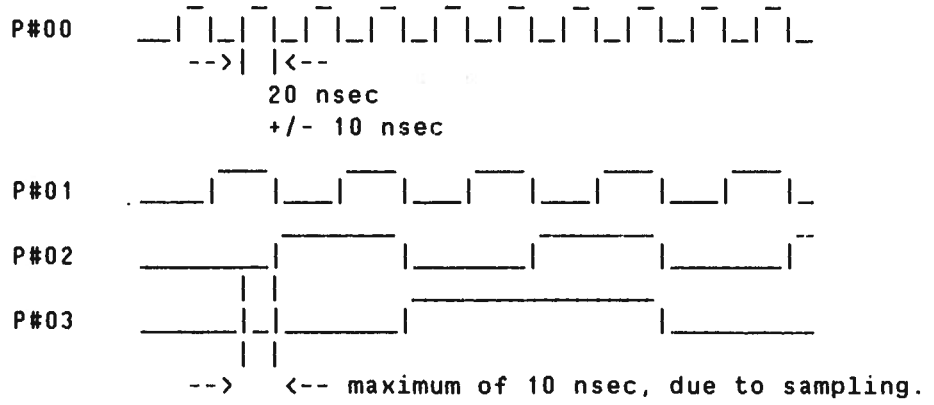
```
0001 0001
0010 0010
0011 0011
0100 0100
0101 0101
0110 0110
0111 0111
1000 1000
1001 1001
1010 1010
1011 1011
1100 1100
1101 1101
1110 1110
1111 1111
0000 0000
```

   C. Connect PM 3632 to the word generated, as shown in the PM 3632 test 3.B.

2. Data capture and triggering.

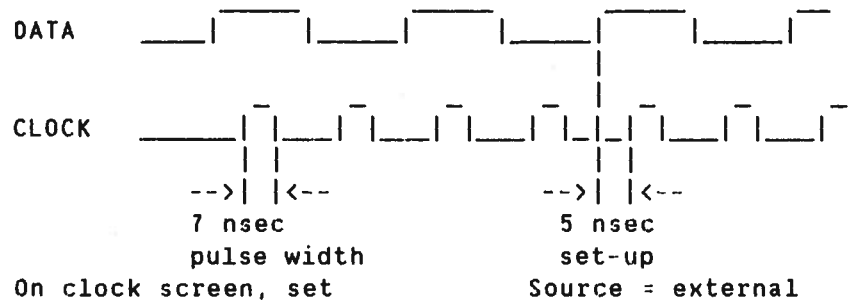
   A. Press Start

   B. On channels 0 ... 3, a counter pattern must be visible.



   Remark: Channel P#00 can be unstable.

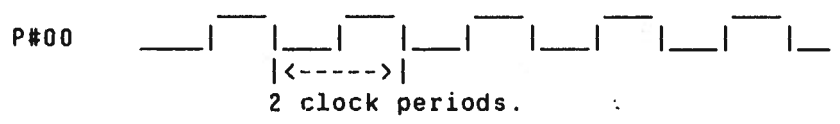
   C. Set word generator clock to 80 nsec repetetion time (12.5 MHz).
   The set-up time for the clock is 5 nsec.



   D. On clock screen, set Source = external
   Edge = rising

E. Press START.

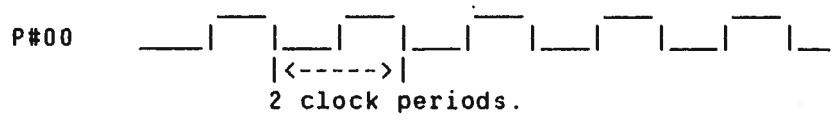
F. Channel 0 (P#00) must be a square wave, with two sampling clocks in one period.



G. On clock screen, set Edge = falling

H. Press START.

I. Channel 0 (P#00) must be a square wave, with two sampling clocks in one period.



J. On clock screen, set Edge = rising
Qual = low

K. Press START.

L. On probe 1 (P#01), the dispayed signal must be low continously.

M. On clock screen, set Qual = high

N. Press START.

O. On probe 1 (P#01), the displayed signal must be high continously.

P. Set word generator to generate the following pattern (walking zero):

```
11111110
11111101
11111011
11110111
11101111
11011111
10111111
01111111
11111110
```

Q. On format screen, set Pod = LOGIC32

R. Press START.

S. Check for walking zero on all 32 channels.

T. Set word generator to generate the following pattern (walking ones):

```
00000001
00000010
00000100
00001000
00010000
00100000
01000000
10000000
00000001
```

U. Press START.

V. Check for walking one on all 32 channels.

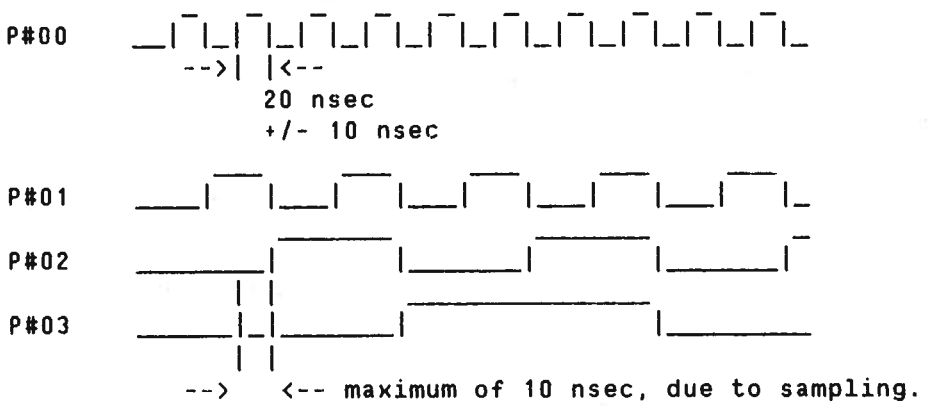
W. Measure the threshold voltage at pin 19 of the 20 pole pod connector.
The voltage must be:
In TTL position: 1.4 V +/- 0.1 V
In VAR position: -9 V ... +9 V selectable

1. Initial set-up
   A. Connect PM 8862 to PM 3632 and switch-on.
   B. Set word generator to generate the following pattern:
      Repetition time for clock = 20 nsec.

```
0001 0001
0010 0010
0011 0011
0100 0100
0101 0101
0110 0110
0111 0111
1000 1000
1001 1001
1010 1010
1011 1011
1100 1100
1101 1101
1110 1110
1111 1111
0000 0000
```

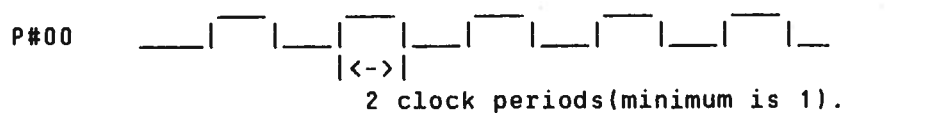
   C. Connect PM 3632 to the word generated, as shown in the PM 3632 test 3.8 (only channels 0 ... 3, clock and qualifier).

2. Data capture and triggering.
   A. Press Start
   B. On channels 0 ... 3, a counter pattern must be visible.



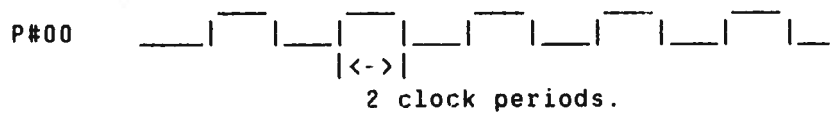
      Remark: Channel P#00 can be unstable.

   C. On clock screen, set Source = external
      Edge = rising
   D. Press START.
   E. Channel 0 (P#00) must be a square wave, with two sampling clocks in one period.



   F. On clock screen, set Edge = falling
   G. Press START.

H. Channel 0 (P#00) must be a square wave, with two sampling clocks in one period.



I. On clock screen, set Edge = rising
Qual = low

J. Press START.

K. On probe 1 (P#01), the dispayed signal must be low continously.

L. On clock screen, set Qual = high

M. Press START.

N. On probe 1 (P#01), the displayed signal must be high continously.

O. Set the pulse generator to generate a pulse of 5 nsec, measured at threshold + 0.40 V (= 1.44 V).
Repetition time = 30 usec.

P. Connect channels 0 ... 3 of the PM 8862 to the pulse generator.

Q. On clock screen, set Source = internal
Clock = 10 nsec

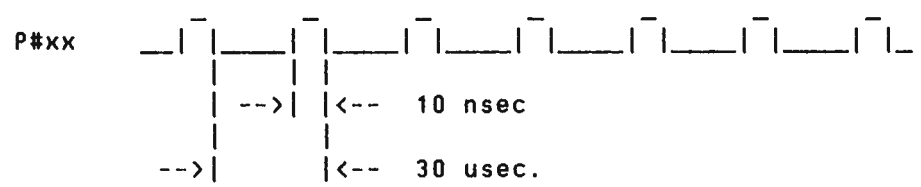
R. Press START.

S. At all 4 channels, the display is unstable.

T. On format screen, set Mode = glitch

U. Press START.

V. At all 4 channels, there must be a regular square wave.



W. Measure the threshold voltage at the molex connector of the pod.
In TTL position: 1.4 V +/- 0.1 V
In VAR position: -7.9 V ... +7.9 V selectable

PM 8865 uP POD

NOTE: Instead of the 8085/Z80 demo unit, any other target system can be used. For other targets however, you must adopt the state lists shown in these checking procedures.

1. Initial set-up

A. Switch-off the PM 3632.

B. Connect the PM 8865 pod to the PM 3632.

C. Connect the uP clip to the 8085 on the demo unit.

D. Switch-on the demo unit.

E. The PM 3632 must be furnished with a Disa rom board with 8085 disa prom.

F. Switch-on the PM 3632.

2. Operation

		BIN	STS	ADR	DAT
A.	On trigger screen, set A:	XXXX	XXXX	0000	F3

B. Press START.

C. After resetting the target, the display must show the following data:

STATE	PC	DISASSEMBLY		BUS ACTIVITY
TRIG	0000	DI		
00001	0001	LXI	H,AAAA	
00004	0004	MVI	M,04	AAAA<-04
00007	0006	LXI	H,5555	
00010	0009	MVI	M,04	5555<-04
00013	000B	IN	00	00->FF
00016	000D	ANI	01	
00018	000F	JZ		
00020	0012	IN	00	00->FF
00023	0014	ANI	02	
00025	0016	JNZ	0080	
00028	0080	MVI	H,55	
00030	0082	MVI	E,AA	
00032	0084	MVI	A,08	

Position cursor: f1 Cursor (f2):

3. Checksum calculation.

A. The checksum of the disa prom must be: 3787 (REV. E).
EF30 (REV. F).

PM 8866, PM 8867 and PM 8868 uP PODS

These pods can not be checked with the 8085/Z80 demo unit.
For checking these pods, any target system can be used to capture some data from, and view the diassembly list.
For checking these uP pods, use the procedure as described for the PM 8865 uP pod.

Checksum of disa proms:	PM 8866	F91B	(REV. B).
		FBF8	(REV. C).
	PM 8867	35BA	(REV. D).
		25D5	(REV. E).
		9F45	(REV. F).
	PM 8868	6E17	(RAV. C).

PM 8869 uP POD

NOTE: Instead of the 8085/Z80 demo unit, any other target system can be used. For other targets however, you must adopt the state lists shown in these checking procedures.

1. Initial set-up

A. Switch-off the PM 3632.

B. Connect the PM 8869 pod to the PM 3632.

C. Connect the uP clip to the Z80 on the demo unit.

D. Switch-on the demo unit.

E. The PM 3632 must be furnished with a Disa rom board with Z80 disa prom.
F. Switch-on the PM 3632.

2. Operation

		BIN	STS	ADR	DAT
A. On trigger screen, set	A:	XXXX	XXXX	0000	F3

B. Press START.
C. After resetting the target, the display must show the following data:

```
STATE   PC   DISASSEMBLY     BUS ACTIVITY

 TRIG  0000  RESET
 TRIG  0000  DI
00001  0001  LD   HL,AAAA
00004  0004  LD   (HL),04      AAAA<04
00007  0006  LD   HL,5555
00010  0009  LD   (HL),04      5555<04
00013  0008  IN   A,(00)         00>FF
00016  000D  AND  01
00018  000F  JP   Z,0035
00020  0012  IN   (A),00         00>FF
00023  0014  AND  02
00025  0016  JP   NZ,0080
00028  0080  LD   H,55
00030  0082  LD   E,AA
Position cursor: f1          Cursor  (f2):
```

3. Checksum calculation.
A. The checksum of the disa prom must be: 996C (REV. H).
8638 (REV. J).
F24A (REV. K).

PM 8870 uP POD

This pods can not be checked with the 8085/Z80 demo unit.
For checking this pod, any target system can be used to capture some data from, and view the diassembly list.
For checking this uP pod, use the procedure as described for the PM 8865 uP pod.

Checksum of disa proms: PM 8870 00A8 (REV. A).

PM 8874 uP POD

This pods can not be checked with the 8085/Z80 demo unit.
For checking this pod, any target system can be used to capture some data from, and view the diassembly list.
For checking this uP pod, use the procedure as described for the PM 8865 uP pod.

Checksum of disa proms: PM 8874 2F70 (REV. B).
Checksum of trigger prom: 02F3 (REV. A).

PM 8876 uP POD

This pods can not be checked with the 8085/Z80 demo unit.
For checking this pod, any target system can be used to capture some data from, and view the diassembly list.
For checking this uP pod, use the procedure as described for the PM 8865 uP pod.

Checksum of disa proms: PM 8876 E58B (REV. A).
Checksum of trigger prom: 02F3 (REV. A).

PM 8880/00 ROM EMULATOR MODULE (rom emulator pod and RS232C card)

NOTE: Instead of the 8085/Z80 demo unit, any other target system can be used. For other targets however, you must adopt the state lists shown in these checking procedures.

1. Initial set-up
   - A. Switch-off the PM 3632.
   - B. Connect RS232C control card to prom programmer.
   - C. Connect rom emulator pod to RS232C control card.
   - D. Connect 8085 uP pod to PM 3632.
   - E. Clip 8085 uP pod to 8085 on demo unit.
   - E. Switch-on the PM 3632.

2. Download from prom programmer to PM 3632 (port A).
   - A. Set promprogrammer transfer format to INTEL hex.
   - B. Load contents of prom (2716 from 8085/Z80 demo unit) in prom programmer (checksum 38F6).
   - C. On PM 3632, set RS232C configuration:

9600 baud	
parity off	
char lenght 8 bits	
delay 00 msec	
delay 000 msec	
EOT char 00	
CR after LF	no
recog XON & XOFF	no
recog CTS	no

   - D. Set rom emulator configuration to: 2716
     A: 0000
   - E. Set rom emulator transfer screen:

Rom emulator pod	1 st
Emulator transfer low address	0000
Emulator transfer high address	07FF
Transfer format	INTEL

   - F. Press 1 twice (at hex keypad).
     The analyzer is noa wauting for the prom programmer to send data).
   - G. On prom programmer, send data out to output port.
   - H. The PM 3632 beeps when data transfer is done.
     The data is now in the ROM emulator pod.

2. Rom emulator port A.

A. Connect rom emulator cable between port A and prom socket on 8085 demo unit.

B. On trigger screen, set

	BIN	STS	ADR	DAT
A:	XXXX	XXXX	0000	XX

C. Press START.

D. Reset 8085 demo unit.

E. The following data must be on the display.

STATE	BIN	STS	ADR	DAT
TRIG	0000	0011	0000	F3
00001	0000		0001	21
00002	0000		0002	AA
00003	0000		0003	AA
00004	0000		0004	36
00005	0000		0005	04
00006	0000		AAAA	04
00007	0000		0006	21
00008	0000		0007	55
00009	0000		0008	55
00010	0000		0009	36
00011	0000		000A	04
00012	0000		5555	04
00013	0000		0008	08

3. Download from prom programmer to PM 3632 (port B).

A. Set rom emulator configuration screen:

	2716
A:	0000
B:	0800

B. Set rom emulator transfer screen:

Rom emulator pod	1 st
Emulator transfer low address	0800
Emulator transfer high address	0BFF
Transfer format	INTEL
	IDLE

C. Press 1 twice (at hex keypad).
The PM 3632 is now waiting for the prom programmer to send data.

D. On prom programmer, send data out to output port.

E. The PM 3632 beeps when data transfer is done.
The data is now in the ROM emulator pod.

4. Rom emulator port B.

A. Connect rom emulator cable to port B.

B. Press START.

C. Reset 8085 demo unit.

D. The following data must be on the display.

STATE	BIN	STS	ADR	DAT
TRIG	0000	0011	0000	F3
00001	0000		0001	21
00002	0000		0002	AA
00003	0000		0003	AA
00004	0000		0004	36
00005	0000		0005	04
00006	0000		AAAA	04
00007	0000		0006	21
00008	0000		0007	55
00009	0000		0008	55
00010	0000		0009	36
00011	0000		000A	04
00012	0000		5555	04
00013	0000		0008	08

5. Download from prom programmer to PM 3632 (port C).

A. Set rom emulator configuration screen:

```
                                    2716
                                A:  0000
                                B:  0800
                                C:  1000
```

B. Set rom emulator transfer screen:

```
        Rom emulator pod                1 st
        Emulator transfer low address   1000
        Emulator transfer high address  17FF
        Transfer format                 INTEL
                                        IDLE
```

C. Press 1 twice (at hex keypad).
The PM 3632 is now waiting for the prom programmer to send data.

D. On prom programmer, send data out to output port.

E. The PM 3632 beeps when data transfer is done.
The data is now in the ROM emulator pod.

6. Rom emulator port C.

A. Connect rom emulator cable to port C.

B. Press START.

C. Reset 8085 demo unit.

D. The following data must be on the display.

STATE	BIN	STS	ADR	DAT
TRIG	0000	0011	0000	F3
00001	0000		0001	21
00002	0000		0002	AA
00003	0000		0003	AA
00004	0000		0004	36
00005	0000		0005	04
00006	0000		AAAA	04
00007	0000		0006	21
00008	0000		0007	55
00009	0000		0008	55
00010	0000		0009	36
00011	0000		000A	04
00012	0000		5555	04
00013	0000		0008	08

7. Download from prom programmer to PM 3632 (port D).

A. Set rom emulator configuration screen:

```
                                        2716
                                   A: 0000
                                   B: 0800
                                   C: 1000
                                   D: 1800
```

B. Set rom emulator transfer screen:

```
        Rom emulator pod                1 st
        Emulator transfer low address   1800
        Emulator transfer high address  1BFF
        Transfer format                 INTEL
                                        IDLE
```

C. Press 1 twice (at hex keypad).
The PM 3632 is now waiting for the prom programmer to send data.

D. On prom programmer, send data out to output port.

E. The PM 3632 beeps when data transfer is done.
The data is now in the ROM emulator pod.

8. Rom emulator port D.

A. Connect rom emulator cable to port D.

B. Press START.

C. Reset 8085 demo unit.

D. The following data must be on the display.

STATE	BIN	STS	ADR	DAT
TRIG	0000	0011	0000	F3
00001	0000		0001	21
00002	0000		0002	AA
00003	0000		0003	AA
00004	0000		0004	36
00005	0000		0005	04
00006	0000		AAAA	04
00007	0000		0006	21
00008	0000		0007	55
00009	0000		0008	55
00010	0000		0009	36
00011	0000		000A	04
00012	0000		5555	04
00013	0000		0008	08

9. Upload from PM 3632 to prom programmer.
   A. Set prom programmer to receive data from PM 3632, and start.
      The prom programmer is now waiting for the PM 3632 to send data.
   B. Set rom emulator transfer screen:

Rom emulator pod	1 st
Emulator transfer low address	1800
Emulator transfer high address	1BFF
Transfer format	INTEL
	IDLE

   C. Press 2 twice (at hex keypad).
      The PM 3632 beeps when data transfer is finished.
      The data is now in the prom programmer.

PM 8080/30 Disa ROM BOERD

A. For testing this board, take the 8085 uP test.
   If the 8085 uP test is passed, the the disa rom board is ok.

PM 8080/40 SETUP MEMORY

NOTE: Instead of the 8085/Z80 demo unit, any other target system can be used. For other targets however, you must adopt the state lists shown in these checking procedures.

A. Switch-off the PM 3632.
B. Connect a 8085 uP pod to the PM 3632.
C. Clip the uP pod over the 8085 at the 8085/Z80 demo unit.
D. Switch-on the PM 3632.
E. On trigger screen, set

	BIN	ST	ADR	DAT
A:	XXXX	XXXX	0000	F3

F. On sequence screen, set seq: A
G. Enter set-up directory screen: special function 7
H. Put cursor in ACTION field.
I. Press f1 twice.
J. Make 7 different settings and store each of these in one of the 7 available set-up files (files 2 ... 8).
Do this in the way described in E ... I.

```
2:      Triggerword A:  ADR = 0000  DAT = F3
                    B:  ADR = 0009  DAT = 36
        Sequence    :   A then B (4)
3:      Triggerword A:  ADR = 0000  DAT = F3
                    B:  ADR = 0009  DAT = 36
                    C:  ADR = 0080  DAT = 26
        Sequence    :   A then B then C (7)
4:      Triggerword A:  ADR = 0000  DAT = F3
                    B:  ADR = 0009  DAT = 36
                    C:  ADR = 0080  DAT = 26
                    D:  ADR = 0097  DAT = C3
        Sequence    :   A then B then C then D (E)
5:      Select menu 1
6:      Select menu 2
7:      Select menu 3
8:      Select menu 4
```

K. Check if the saved menus can be recalled again.
Press special functions 7.
Put cursor in ACTION field.
Press f2 twice.
L. Power-up file test.
Press special functions 7.
Put cursor on power-up file position and fill-in 4.
Switch-off the PM 3632.
Switch-on, and check if setting nr. 4 is loaded automatically after power-up.
M. Check if the name of a set-up file can be altered.
For this, put the cursor in the NAME field, and use the f1 and f2 keys.

PM 8880/50 SET-UP AND DATA MEMORY

1. Set-up memory test.
A. Refer to the PM 8880/40 tests.

2. Data memory test.
A. Switch-off the PM 3632.
B. Connect a 8085 uP pod to the PM 3632.
C. Clip the uP pod over the 8085 at the 8085/Z80 demo unit.
D. Switch-on the PM 3632.
E. Press special functions 8.
F. Put cursor on 8 memory configuration field, and fill-in 4.
G. On trigger screen, set

```
                    BIN    ST   ADR   DAT
              A:    XXXX  XXXX  0000   F3
```

H. On sequence screen, set seq: A
I. Press START.
J. Press special functions 8.

K. Press X, then f2 (copy data from A to B memory).
L. Put cursor on ACTION field (file 1).
M. Press f1 twice.
N. Do L and M for the other 3 B memory files.
O. Check if the just stored files can be recalled.
Put cursor in ACTION field and press f2 twice.
A * indicates that a file is recalled.

3. B memory edit test.
A. Press special functions B.
B. Put cursor on first position by means of f1 key.
C. Press f3.
D. Fill data field with 55.
E. Put cursor on last position by means of f1 key.
F. Press f3.
The complete B memory must be filled with 55 now.
G. Repeat tests B ... F with data AA.
The complete B memory must be filled with AA now.
H. Press special functions B.
I. Put cursor on ACTION field of file 1.
J. Press f2 twice (file 1 is recalled).
K. Press special functions B.
L. Check if the following data is in B memory.

```
F3
21
AA
AA
36
|
|
etc.
```

APPENDIX C

Calibration procedure for PM 3632 mainframe.

Necessary equipment

100 MHz frequency counter.
Multimeter.

100 Mhz timing oscillator:

1. Switch-off the instrument.
2. Remove the front and rear rims (4 screws).
3. Lift the top cover.
4. Connect the probe of the frequency counter to pin 8 of U63 at the capture board.
5. Switch-on the instrument.
6. Measure the clock frequency at pin 8 of U63 at the capture board.
7. If the frequency is not 100 MHz, then adjust it to 100 MHz exactly, with trimmer C4 (at the capture board).
8. Switch-off the instrument.
9. Fix the top cover and the rims again.

Switching power supply

1. Switch-off the instrument.
2. Remove the front and rear rims (4 screws).
3. Lift the top cover.
4. Disconnect the 5 and 10 pole molex connectors from the power board.
   Disconnect the 26 transition connector from the power board.
5. Switch-on the instrument.
6. Measure the voltage between pins 1 and 2 (ground) at the 5 pole (female) molex connector.
   This must be 20 ... 27 Vdc.
7. Switch-off the instrument and discharge the 8800 uF capacitor with a 100 ... 500 ohm resistor (a few seconds).
8. Connect the 5 pole molex connector to the power board again.
9. Using clip leads, attach a 4.7 ohm, 5 W resistor between the anode of CR5 (ground) and the cathode of CR7 (on the power board).
10. Switch-on the instrument.
11. Measure the voltage across the 4.7 ohm resistor.
    It must be 5.0 Vdc (adjustable with R2 on the power control board).
12. Switch-off the instrument, and disconnect the clip leads from the power board.
13. Using clip leads, connect a 7.5 ohm, 10 W resistor between the anode of CR3 and the anode (ground) of CR5 (on the power board).
14. Switch-on the instrument.
15. Measure the voltage acrosss the 7.5 ohm resistor.
    It must be -8.5 Vdc (adjustable with R3 on the power control board).

16. Measure the voltage between the upper side of coil L5 (on the power board) and the anode (ground) of CR5 (on the power board).
    It should be 12.0 Vdc +/- 0.5V (not adjustable; if not correct, check VR1).
17. Switch-off the instrument and disconnect the clip leads.
18. Connect the 10 pole molex connector and the 26 transition connector again.
19. Connect a PM 8860 32-channel standard pod to the PM 3632.
20. Switch-on the instrument.
21. Measure the voltage across C46 on the capture board.
    If necessary, readjust R2 (on power control board) to get 5.0 Vdc +/- 0.1 V.
22. Fix top cover and rims to the mainframe again.

APPENDIX D

Program listing of 8085/Z80 demo unit.

```
1                                       NAME    MLTEST
2       0000                            ASEG
3                               ;
4                               ;       THIS HIGHLY COMPLICATED PROGRAM WILL PROBABLY TAKE THE EXPERIENCED
5                               ;       PROGRAMMER SEVERAL HOURS TO COMPREHEND. PRESS SWITCH 1, GOTO STATE 1.
6                               ;       PRESS SWITCH 2, GOTO STATE 2. PRESS EITHER SWITCH ONCE AND THE OTHER
7                               ;       SWITCH TWICE AND GOTO STATE 0.
8                               ;
9                               ;       BREAKPOINTS FOR STATES:
10                              ;
11                              ;               STATE0 -   0H
12                              ;               STATE1 - 100H
13                              ;               STATE2 - 200H
14                              ;
15                              ;       STATE 0
16                              ;
17      0000                            ORG     0
18                              ;
19 0000 F3              STATE0: DI                      ;DISABLE INTERRUPTS
20 0001 21      AAAA            LXI     H,0AAAAH        ;MAKE SURE ALL BITS GO DIFFERENT WAYS
21 0004 36      04              MVI     M,H
22 0006 21      5555            LXI     H,5555H
23 0009 36      04              MVI     M,H
24 000B DB      00              IN      0               ;READ INPUT SWITCH PORT
25 000D E6      01              ANI     1               ;MASK SWITCH 1
26 000F CA      0035            JZ      A10             ;IF PRESSED THEN JUMP ELSE
27 0012 DB      00              IN      0               ;READ INPUT SWITCH PORT
28 0014 E6      02              ANI     2               ;MASK SWITCH 2
29 0016 C2      0080            JNZ     MULTA           ;IF NOT PRESSED THEN JUMP ELSE
30 0019 21      03E8            LXI     H,1000          ;DEBOUNCE SWITCH
31 001C 74              A5:     MOV     M,H             ;PUT MSB OF CTR ON ADDRESS BUS FOR DISASSEMBLY
32 001D 75                      MOV     M,L             ;PUT LSB OF CTR ON ADDRESS BUS
33 001E 2B                      DCX     H               ;DECREMENT CTR
34 001F 7C                      MOV     A,H             ;IS DEBOUNCE TIME OVER
35 0020 B5                      ORA     L
36 0021 C2      001C            JNZ     A5              ;IF NOT THEN LOOP ELSE
37 0024 DB      00              IN      0               ;IS SWITCH STILL PRESSED?
38 0026 E6      02              ANI     2
39 0028 C2      0000            JNZ     STATE0          ;IF NOT THEN IGNORE SWITCH ELSE
40 002B DB      00      A8:     IN      0               ;WAIT FOR SWITCH TO BE RELEASED
41 002D E6      02              ANI     2
42 002F CA      002B            JZ      A8              ;LOOP IF STILL PRESSED ELSE
43 0032 C3      0200            JMP     STATE2          ;JUMP TO STATE2
44                              ;
45 0035 21      03E8    A10:    LXI     H,1000          ;DEBOUNCE SWITCH
46 0038 74              A15:    MOV     M,H             ;PUT MSB OF CTR ON ADDRESS BUS FOR DISASSEMBLY
47 0039 75                      MOV     M,L             ;PUT LSB OF CTR ON ADDRESS BUS
48 003A 2B                      DCX     H               ;DECREMENT CTR
49 003B 7C                      MOV     A,H             ;IS DEBOUNCE TIME OVER
50 003C B5                      ORA     L
51 003D C2      0038            JNZ     A15             ;IF NOT THEN LOOP ELSE
52 0040 DB      00              IN      0               ;IS SWITCH STILL PRESSED?
53 0042 E6      01              ANI     1
54 0044 C2      0000            JNZ     STATE0          ;IF NOT THEN IGNORE SWITCH ELSE
55 0047 DB      00      A18:    IN      0               ;WAIT FOR SWITCH TO BE RELEASED
56 0049 E6      01              ANI     1
57 004B CA      0047            JZ      A18             ;LOOP IF STILL PRESSED ELSE
```

```
1 004E   C3    0100          JMP     STATE1          ;JUMP TO STATE1
2                      ;
3                      ;       8X8 MULTIPLY. OPERANDS IN H & E. ANSWER IN HL
4                      ;
5        0080                  ORG     80H
6                      ;
7 0080   26    55      MULTA:  MVI     H,055H          ;SET OPERANDS
8 0082   1E    AA              MVI     E,0AAH
9 0084   3E    08              MVI     A,8             ;SET LOOP CTR
10 0086  2E    00              MVI     L,0             ;PUT MULTIPLIER IN HL
11 0088  55                    MOV     D,L             ;ZERO D
12 0089  29            MULT1:  DAD     H               ;SHIFT MULTPLIER AND ANSWER TO LEFT
13 008A  74                    MOV     M,H             ;PUT PARTIAL ANSWER ON BUS
14 008B  75                    MOV     M,L
15 008C  D2    0092            JNC     MULT2           ;IF NO MULTIPLIER BIT SHIFTED OUT THEN JUMP ELSE
16 008F  19                    DAD     D               ;ADD MULTIPLICAND TO ANSWER
17 0090  74                    MOV     M,H             ;PUT PARTIAL ANSWER ON BUS
18 0091  75                    MOV     M,L
19 0092  3D            MULT2:  DCR     A               ;DECREMENT LOOP CTR
20 0093  77                    MOV     M,A             ;PUT LOOP CTR OUT ON BUS
21 0094  C2    0089            JNZ     MULT1           ;LOOP IF NOT DONE ELSE
22 0097  C3    0000.           JMP     STATE0          ;LOOP AND CHECK FOR SWITCHES AGAIN
23                     ;
24                     ;       STATE 1
25                     ;
26       0100                  ORG     100H
27                     ;
28 0100  DB    00      STATE1: IN      0               ;READ INPUT SWITCH PORT
29 0102  E6    01              ANI     1               ;MASK SWITCH 1
30 0104  CA    012A            JZ      A23             ;IF PRESSED THEN JUMP ELSE
31 0107  DB    00              IN      0               ;READ INPUT SWITCH PORT
32 0109  E6    02              ANI     2               ;MASK SWITCH 2
33 010B  C2    0180            JNZ     MULTB           ;IF NOT PRESSED THEN JUMP ELSE
34 010E  21    03E8            LXI     H,1000          ;DEBOUNCE SWITCH
35 0111  74            A19:    MOV     M,H             ;PUT MSB OF CTR ON ADDRESS BUS FOR DISASSEMBLY
36 0112  75                    MOV     M,L             ;PUT LSB OF CTR ON ADDRESS BUS
37 0113  2B                    DCX     H               ;DECREMENT CTR
38 0114  7C                    MOV     A,H             ;IS DEBOUNCE TIME OVER
39 0115  B5                    ORA     L
40 0116  C2    0111            JNZ     A19             ;IF NOT THEN LOOP ELSE
41 0119  DB    00              IN      0               ;IS SWITCH STILL PRESSED?
42 011B  E6    02              ANI     2
43 011D  C2    0100            JNZ     STATE1          ;IF NOT THEN IGNORE SWITCH ELSE
44 0120  DB    00      A20:    IN      0               ;WAIT FOR SWITCH TO BE RELEASED
45 0122  E6    02              ANI     2
46 0124  CA    0120            JZ      A20             ;LOOP IF STILL PRESSED ELSE
47 0127  C3    0200            JMP     STATE2          ;JUMP TO STATE2
48                     ;
49 012A  21    03E8    A23:    LXI     H,1000          ;DEBOUNCE SWITCH
50 012D  74            A25:    MOV     M,H             ;PUT MSB OF CTR ON ADDRESS BUS FOR DISASSEMBLY
51 012E  75                    MOV     M,L             ;PUT LSB OF CTR ON ADDRESS BUS
52 012F  2B                    DCX     H               ;DECREMENT CTR
53 0130  7C                    MOV     A,H             ;IS DEBOUNCE TIME OVER
54 0131  B5                    ORA     L
55 0132  C2    012D            JNZ     A25             ;IF NOT THEN LOOP ELSE
56 0135  DB    00              IN      0               ;IS SWITCH STILL PRESSED?
57 0137  E6    01              ANI     1
```

```
 1 0139  C2    0100          JNZ     STATE1          ;IF NOT THEN IGNORE SWITCH ELSE
 2 013C  DB    00    A28:    IN      0               ;WAIT FOR SWITCH TO BE RELEASED
 3 013E  E6    01            ANI     1
 4 0140  CA    013C          JZ      A28             ;LOOP IF STILL PRESSED ELSE
 5 0143  C3    0000          JMP     STATE0          ;JUMP TO STATE0
 6                     ;
 7                     ;       8X8 MULTIPLY. OPERANDS IN H & E. ANSWER IN HL
 8                     ;
 9       0180                  ORG     180H
10                     ;
11 0180  26    34    MULTB:  MVI     H,034H          ;SET OPERANDS
12 0182  1E    56            MVI     E,056H
13 0184  3E    08            MVI     A,8             ;SET LOOP CTR
14 0186  2E    00            MVI     L,0             ;PUT MULTIPLIER IN HL
15 0188  55                  MOV     D,L             ;ZERO D
16 0189  29           MULT1B: DAD     H               ;SHIFT MULTPLIER AND ANSWER TO LEFT
17 018A  74                  MOV     M,H             ;PUT PARTIAL ANSWER ON BUS
18 018B  75                  MOV     M,L
19 018C  D2    0192          JNC     MULT2B          ;IF NO MULTIPLIER BIT SHIFTED OUT THEN JUMP ELSE
20 018F  19                  DAD     D               ;ADD MULTIPLICAND TO ANSWER
21 0190  74                  MOV     M,H             ;PUT PARTIAL ANSWER ON BUS
22 0191  75                  MOV     M,L
23 0192  3D           MULT2B: DCR     A               ;DECREMENT LOOP CTR
24 0193  77                  MOV     M,A             ;PUT LOOP CTR OUT ON BUS
25 0194  C2    0189          JNZ     MULT1B          ;LOOP IF NOT DONE ELSE
26 0197  C3    0100          JMP     STATE1          ;LOOP AND CHECK FOR SWITCHES AGAIN
27                     ;
28                     ;       STATE 2
29                     ;
30       0200                  ORG     200H
31                     ;
32 0200  DB    00    STATE2: IN      0               ;READ INPUT SWITCH PORT
33 0202  E6    01            ANI     1               ;MASK SWITCH 1
34 0204  CA    022A          JZ      A40             ;IF PRESSED THEN JUMP ELSE
35 0207  DB    00            IN      0               ;READ INPUT SWITCH PORT
36 0209  E6    02            ANI     2               ;MASK SWITCH 2
37 020B  C2    0280          JNZ     MULTC           ;IF NOT PRESSED THEN JUMP ELSE
38 020E  21    03E8          LXI     H,1000          ;DEBOUNCE SWITCH
39 0211  74           A35:    MOV     M,H             ;PUT MSB OF CTR ON ADDRESS BUS FOR DISASSEMBLY
40 0212  75                  MOV     M,L             ;PUT LSB OF CTR ON ADDRESS BUS
41 0213  2B                  DCX     H               ;DECREMENT CTR
42 0214  7C                  MOV     A,H             ;IS DEBOUNCE TIME OVER
43 0215  B5                  ORA     L
44 0216  C2    0211          JNZ     A35             ;IF NOT THEN LOOP ELSE
45 0219  DB    00            IN      0               ;IS SWITCH STILL PRESSED?
46 021B  E6    02            ANI     2
47 021D  C2    0200          JNZ     STATE2          ;IF NOT THEN IGNORE SWITCH ELSE
48 0220  DB    00    A38:    IN      0               ;WAIT FOR SWITCH TO BE RELEASED
49 0222  E6    02            ANI     2
50 0224  CA    0220          JZ      A38             ;LOOP IF STILL PRESSED ELSE
51 0227  C3    0000          JMP     STATE0          ;JUMP TO STATE0
52                     ;
53 022A  21    03E8    A40:  LXI     H,1000          ;DEBOUNCE SWITCH
54 022D  74           A45:    MOV     M,H             ;PUT MSB OF CTR ON ADDRESS BUS FOR DISASSEMBLY
55 022E  75                  MOV     M,L             ;PUT LSB OF CTR ON ADDRESS BUS
56 022F  2B                  DCX     H               ;DECREMENT CTR
57 0230  7C                  MOV     A,H             ;IS DEBOUNCE TIME OVER
```

```
 1 0231  55                      ORA     L
 2 0232  C2      022D            JNZ     A45             ;IF NOT THEN LOOP ELSE
 3 0235  DB      00              IN      0               ;IS SWITCH STILL PRESSED?
 4 0237  E6      01              ANI     1
 5 0239  C2      0200            JNZ     STATE2          ;IF NOT THEN IGNORE SWITCH ELSE
 6 023C  DB      00      A48:    IN      0               ;WAIT FOR SWITCH TO BE RELEASED
 7 023E  E6      01              ANI     1
 8 0240  CA      023C            JZ      A48             ;LOOP IF STILL PRESSED ELSE
 9 0243  C3      0100            JMP     STATE1          ;JUMP TO STATE1
10                      ;
11                      ;
12                      ;       8X8 MULTIPLY. OPERANDS IN H & E. ANSWER IN HL
13                      ;
14      0280                    ORG     280H
15                      ;
16 0280  26     DC      MULTC:  MVI     H,0DCH          ;SET OPERANDS
17 0282  1E     23              MVI     E,023H
18 0284  3E     08              MVI     A,8             ;SET LOOP CTR
19 0286  2E     00              MVI     L,0             ;PUT MULTIPLIER IN HL
20 0288  55                     MOV     D,L             ;ZERO D
21 0289  29             MULT1C: DAD     H               ;SHIFT MULTPLIER AND ANSWER TO LEFT
22 028A  74                     MOV     M,H             ;PUT PARTIAL ANSWER ON BUS
23 028B  75                     MOV     M,L
24 028C  D2     0292            JNC     MULT2C          ;IF NO MULTIPLIER BIT SHIFTED OUT THEN JUMP ELSE
25 028F  19                     DAD     D               ;ADD MULTIPLICAND TO ANSWER
26 0290  74                     MOV     M,H             ;PUT PARTIAL ANSWER ON BUS
27 0291  75                     MOV     M,L
28 0292  3D             MULT2C: DCR     A               ;DECREMENT LOOP CTR
29 0293  77                     MOV     M,A             ;PUT LOOP CTR OUT ON BUS
30 0294  C2     0289            JNZ     MULT1C          ;LOOP IF NOT DONE ELSE
31 0297  C3     0200            JMP     STATE2          ;LOOP AND CHECK FOR SWITCHES AGAIN
32                      ;
33                      END
```