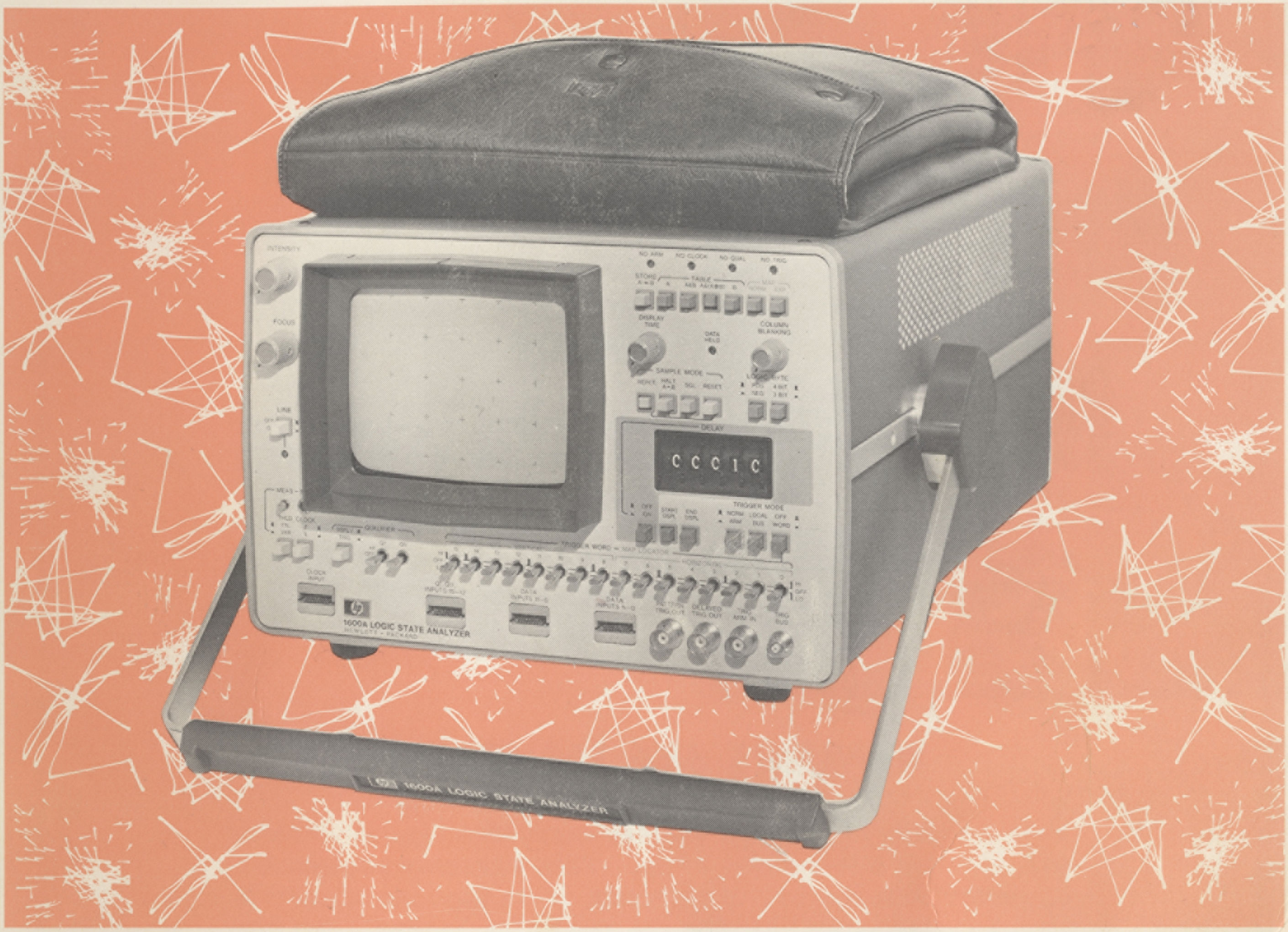
HP 1600A

1600A LOGIC STATE ANALYZER OPERATING AND SERVICE MANUAL



1600A

LOGIC STATE ANALYZER

PRELIMINARY OPERATING AND SERVICE MANUAL

HEWLETT hp PACKARD

COLORADO SPRINGS DIVISION

HP 1600A

CERTIFICATION

The Hewlett-Packard Company certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory. The Hewlett-Packard Company further certifies that its calibration measurements are traceable to the U.S. National Bureau of Standards to the extent allowed by the Bureau's calibration facility.

WARRANTY AND ASSISTANCE

This Hewlett-Packard product is warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products which prove to be defective during the warranty period provided they are returned to Hewlett-Packard. No other warranty is expressed or implied. We are not liable for consequential damages.

Service contracts or customer assistance agreements are available for Hewlett-Packard products that require maintenance and repair on-site.

PRELIMINARY

OPERATING AND SERVICE MANUAL

MODEL 1600A
LOGIC STATE ANALYZER

SERIALS PREFIXED: 1510A

Refer to Section VII for instruments with other Serial Prefixes.

HEWLETT-PACKARD COMPANY/COLORADO SPRINGS DIVISION
1900 GARDEN OF THE GODS ROAD, COLORADO SPRINGS, COLORADO, U.S.A.

Manual Part Number 01600-90902

PRINTED: JULY 1975

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the cathode-ray tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the instrument. Handling of the CRT shall be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont'd)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont'd)

LIST OF TABLES

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual provides operating and service information for the Hewlett-Packard Model 1600A Logic State Analyzer (figure 1-1).

1-3. This section of the manual contains performance specifications for the Model 1600A (table 1-1) and provides brief descriptive information on the instrument, accessories, and manual. Other sections provide information as follows:

Section II, Installation, contains information and procedures to perform an initial inspection, and to prepare the instrument for use, storage or shipment.

Section III, Operation, describes instrument controls, connectors, and panel features and provides operating checks and instructions.

Section IV, Principles of Operation, provides detailed descriptions and theory of instrument operation.

Section V, Maintenance, provides information required to verify that the instrument is performing in accordance with the specifications listed in table 1-1.

Section VI, Replaceable Parts, provides ordering information and a listing of replaceable parts.

Section VII, Manual Changes, provides manual change information (when applicable) to backdate this manual for use with instruments having serial prefix numbers lower than the one shown on the manual title page.

Section VIII, Service, provides information required to repair the instrument. Schematics, troubleshooting information, and service procedures are included.

1-4. On the title page of this manual, below the manual part number, is a "Microfiche" part number. This number can be used to order 4-by 6-inch microfilm transparencies of the manual. The microfiche package also includes the latest Manual Changes supplement.

1-5. DESCRIPTION.

1-6. The Model 1600A Logic State Analyzer is designed to aid in the analysis of digital systems which depend on sequences of logic states to control their operation. The Model 1600A provides a functional display of ones and zeros in tabular format of logic states at up to 16 variables in a digital system (up to 32 variables may be displayed when a Model 1607A Logic State Analyzer is used with the Model 1600A in the bus mode).

1-7. Tabular data is displayed in two tables of sixteen 16-bit words. Table A (left half of the CRT screen) is a display of A-memory data acquired from the circuit under test through the Model 1600A data input connectors. Table B (right half of the CRT screen) is a display of B-memory data (data transferred from A-memory by the STORE A→B pushbutton or Model 1607A input data when the Model 1600A is connected to a Model 1607A using a Model 10237A I/O Interface Cable), or a display of the exclusive-OR of A-memory and B-memory data.

1-8. In the map-display modes, the Model 1600A displays digital words up to sixteen bits in length as single dots whose location on the CRT screen identifies them uniquely. In the map mode, the Model 1600A can display up to 65 536 16-bit words (all possible states in a 16-bit state machine).

1-9. Data is synchronously loaded into the Model 1600A by the clock input transition corresponding to the selected clock slope. The Model 1600A will accept any convenient clock signal, such as a handshake signal on a data bus or other strobe or command lines, at rates up to 20 MHz. Selectable input thresholds, either fixed TTL or variable, enable the Model 1600A to interface with most logic families.

1-10. In the table display mode, a preset trigger word set on front-panel switches controls the reference of the sixteen-word display window to the input data stream. Depending on the trigger mode selected, the display starts at the trigger word, ends at the trigger word (negative-time data capture), or is delayed up to 99 999 input-clock pulses after the trigger word. In the map mode, the same front-panel switches that select the trigger word for the table display are used to position the map locator (cursor) on the CRT screen. In the normal map mode, the cursor is used to locate the display sector to be expanded in EXP mode. In the expand map mode, the cursor allows selection of a specific state (dot) to be the trigger word for the table display.

1-11. During repetitive operation, the display is repetitively updated by incoming data. To monitor infrequent or one-time-only events, the display can be set to a single-shot mode (SGL). In this mode, gathered data is retained and displayed until manually reset. In the HALT A ≠ B mode, the display is repetitively updated by incoming data until a difference between the data in the two displayed memories is detected. When a difference is detected, the data is retained and displayed until manually reset.

1-12. The Model 1600A has two qualifier channels that can function in either a trigger-qualified mode (TRIG) or a display-qualified mode (DSPLY). Trigger qualification allows the two qualifier channels to be used as additional undisplayed data channels, providing an 18-bit trigger word. Display qualification allows selective viewing of data by storing and displaying only those data words that occur on clock edges when qualifier conditions are true.

1-13. Other features of the Model 1600A include:

a. a trigger-arming circuit that allows sequential triggering;

b. a partial-display mode to permit data to be displayed as it is single-stepped into the Model 1600A;

c. arrangement of the displayed words in bytes of three bits each (octal format) or in bytes of four bits each (hexadecimal or BCD format);

d. intensification of the trigger word in table displays;

e. the capability of blanking unrequired columns of bits, starting with the leftmost column;

f. two front-panel trigger outputs, one generated when the selected trigger word is detected, and the other generated when the delay is complete.

Table 1-1. Specifications

CLOCK AND DATA INPUTS

REPETITION RATE: 0 to 20 MHz.
INPUT RC: 40 kΩ ±3 kΩ shunted by ≤14 pF.
INPUT BIAS CURRENT: ≤30 μA.
INPUT THRESHOLD: TTL, fixed at approx +1.5 V; variable, ±10 Vdc.
MAXIMUM INPUT
Level: —15 to +15 Vdc.
Swing: 15 V peak from threshold.
MINIMUM INPUT
Swing: 0.5 V +5% of p-p threshold voltage.
Clock Pulse Width: 20 ns at threshold.
Data Pulse Width: 25 ns at threshold.
Data Setup Time: time data must be present prior to clock transition, 20 ns.
Hold Time: time data must be present after clock transition, 0 ns.

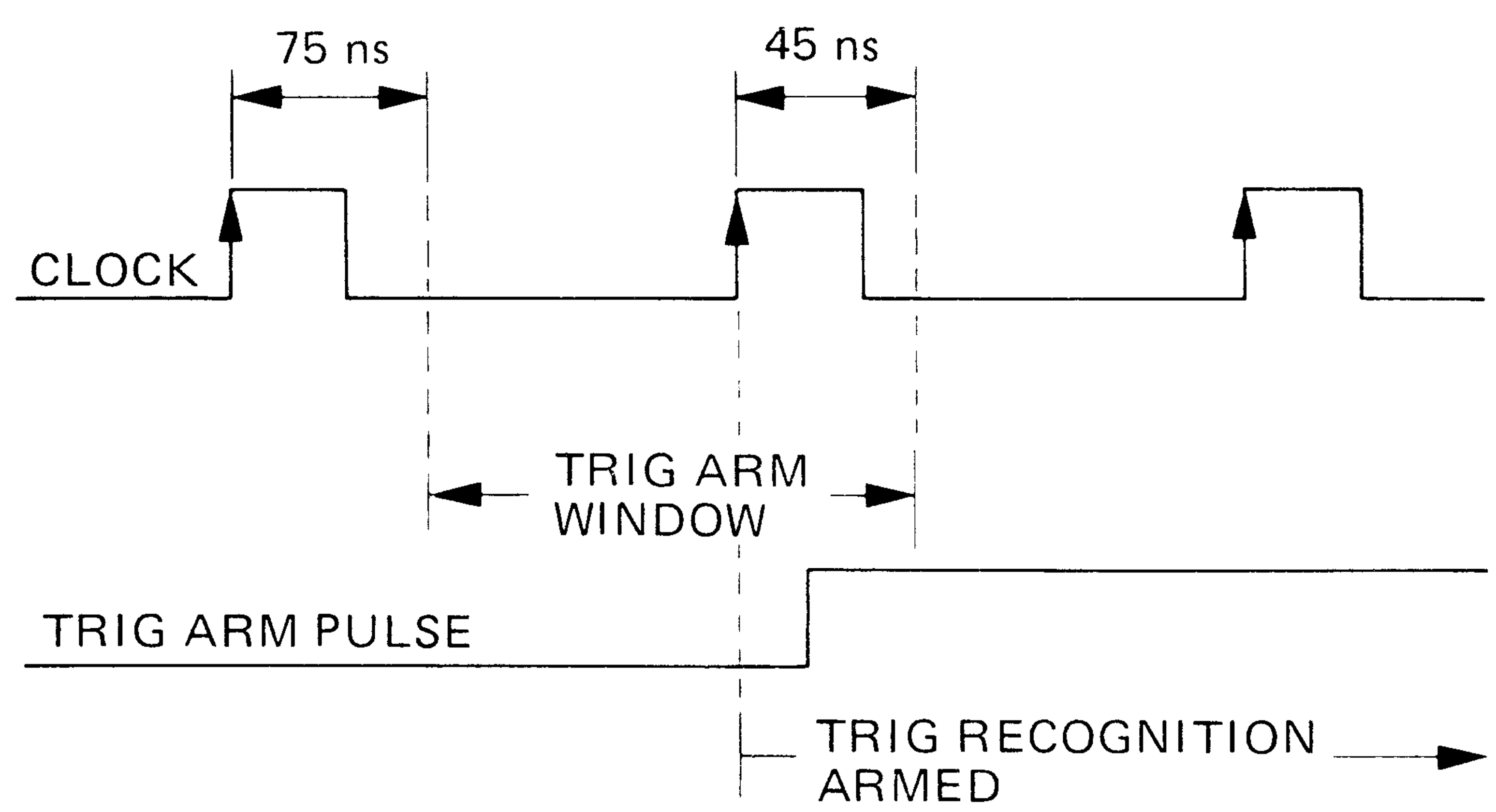
PATTERN AND DELAYED TRIGGER OUTPUTS

HIGH: ≥2 V into 50Ω (line driver interface).
LOW: ≤0.4 V into 50Ω (line driver interface).
PULSE DURATION
Delayed Trigger: approx 25 ns (RZ format) at 1 V level.
Pattern Trigger: approx 25 ns in RZ format at 1 V level with delay set to zero or off. With delay on and not set to zero, pattern trigger output starts on receipt of a pattern trigger signal and ends when the delay ends.

TRIGGER ARM INPUT

IMPEDANCE: 50Ω.
LEVEL: low state, 0 V to <0.4 V; high state, 2 V to <5 V.
PULSE WIDTH: 15 ns minimum at 1.5 V level.

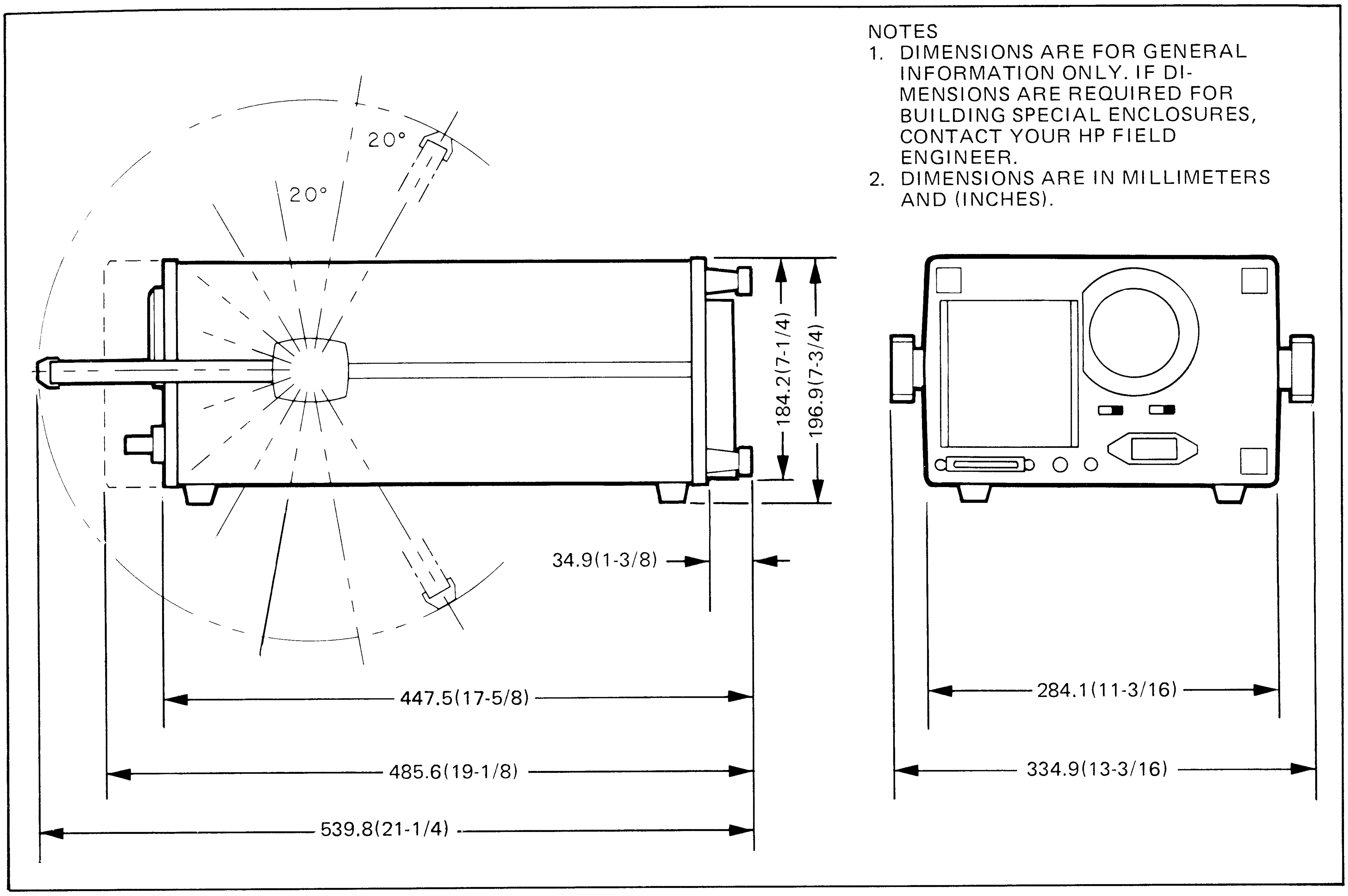
ARMING CONDITIONS: if the arming pulse positive edge occurs <45 ns after a clock, triggering occurs on the same clock cycle that it is armed. If the arming pulse positive edge occurs >75 ns after a clock, triggering occurs on the next clock cycle.



GENERAL

DISPLAY TIME: variable from <200 ms to >5 s.
POWER REQUIREMENTS: 100, 120, 220 or 240 Vac +6, —13%; 48 to 440 Hz, maximum power 120 VA (nominal 88 VA).
DIMENSIONS: see outline drawings.
WEIGHT: net 12.59 kg (27-1/8 lb); shipping, 15.31 kg (33-3/4 lb).
OPERATING ENVIRONMENT
Temperature: 0°C to +55°C.
Humidity: to 95% at 40°C.
Altitude: to 4600 m (15 000 ft).
Vibration: vibrated in three planes for 15 min. each with 0.254 mm (0.010 in.) excursion, 10 to 55 Hz.

Table 1-1. Specifications (Cont'd)



1-14. ACCESSORIES.

1-15. ACCESSORIES SUPPLIED. One Model 10230B Clock Probe and three Model 10231B Six Bit Data probes are supplied with the Model 1600A. The Model 10230B and Model 10231B are active probes providing complementary TTL (transistor-transistor logic) clock and data signals to the Model 1600A. Probe operating power is supplied by the Model 1600A. The probes connect to the Model 1600A front panel by means of 17-pin miniature snap-in connectors. Refer to the operating and service literature supplied with these probes for more detailed information.

1-16. ACCESSORIES AVAILABLE. A six-inch trigger interface cable (HP Model 10236A) and a 12-inch I/0 interface cable (HP Model 10237A) are available for use with the Model 1600A. These cables are required to interface the Model 1600A with a Model 1607A in the bus mode.

1-17. INSTRUMENT AND MANUAL IDENTIFICATION.

1-18. Instrument identification by serial number is located on the rear panel. Hewlett-Packard uses a two-section serial number consisting of a four-digit prefix and a five-digit suffix, separated by a letter designating the country in which the instrument was manufactured. (A = U.S.A.; G = West Germany; J = Japan; U = United Kingdom.)

1-19. This manual applies to instruments with the serial numbers indicated on the title page. If changes have been made in the instrument since this manual was printed, a "Manual Changes" supplement supplied with the manual will define these changes. Be sure to record these changes in your manual. Backdating information in Section VII adapts the manual to instruments with serial numbers lower than that shown on the title page. Part numbers for the manual and the microfiche copy of the manual are also shown on the title page.

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains instructions for performing an initial inspection of the Model 1600A. Installation procedures and precautions are presented in step-by-step order. The procedures for making a claim for warranty repairs and for repacking the instrument for shipment are also described in this section.

2-3. INITIAL INSPECTION.

2-4. The instrument was inspected mechanically and electrically before shipment. Upon receipt, inspect it for damage that may have occurred in transit. Check for broken knobs, bent or broken connectors, and dents or scratches. If damage is found, refer to the claims paragraph in this section. Retain the packing material for possible future use.

2-5. Check the operation of the instrument immediately after receipt. Refer to Section III for the operator's checks and adjustments. The operator's check will determine whether or not the instrument is operating properly. If the instrument does not operate properly, refer to the claims paragraph in this section.

2-6. PREPARATION FOR USE.

WARNING

Read the Safety Summary at the front of this manual before installing or operating the instrument.

2-7. POWER REQUIREMENTS. The instrument requires a source of 100-, 120-, 220-, or 240-volts ac +6, —13%, single-phase, 48 to 440 Hz that can deliver approximately 120 volt-amperes. The instrument is normally shipped from the factory to operate from a 120-volt ac power source. The LINE SELECTOR slide switches on the rear panel select either 100-, 120-, 220-, or 240-volt operation. To check or change the position of the LINE SELECTOR switches, see figure 2-1 and proceed as follows:

a. Turn off instrument power and remove power cord from rear-panel connector.

b. For 100- or 120-volt operation, set LINE SELECTOR switches to 100 V or 120 V and install 1-ampere, time-delay fuse for F1.

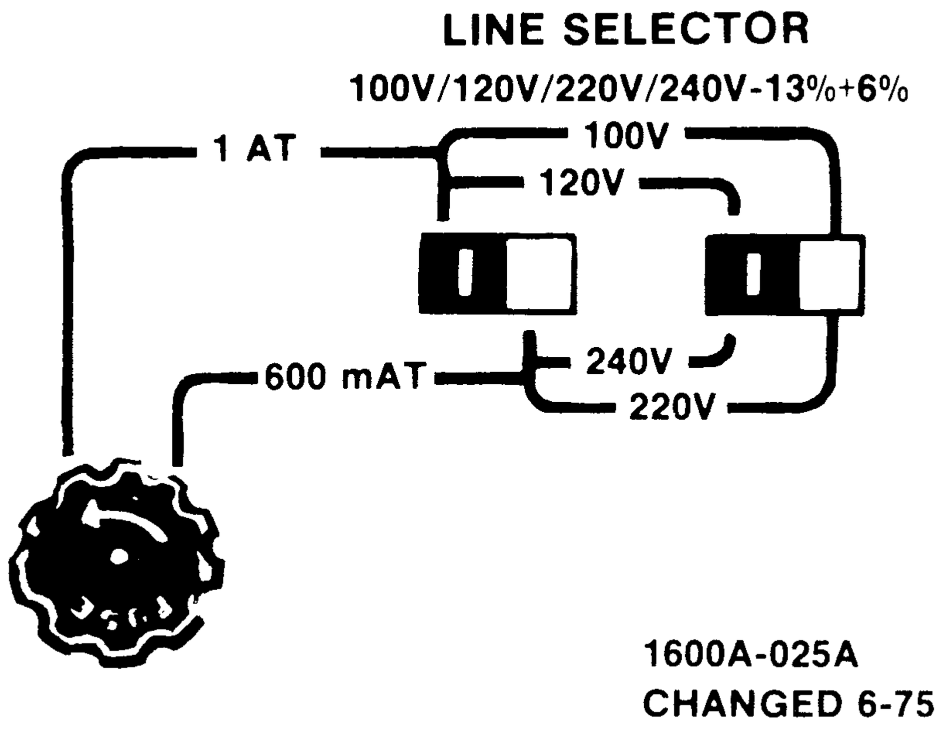


Figure 2-1. Line Voltage Selection

c. For 220- or 240-volt operation, set LINE SELECTOR switches to 220 V or 240 V and install 600-mA, time-delay fuse for F1.

d. Reconnect power cord.

2-8. THREE-CONDUCTOR POWER CABLE. This instrument is equipped with a three-conductor power cable that, when connected to an appropriate receptacle, grounds the instrument through the offset pin. The power cable required depends on the ac input voltage, and the country in which the instrument is to be used. Figure 2-2 illustrates the standard power receptacle (wall outlet) configurations that are used throughout the United States and in other countries. The HP part number shown adjacent to each receptacle drawing is the part number for a power cable equipped with a mating plug for that receptacle. If the appropriate power cable is not included with the instrument, notify the nearest Hewlett-Packard Sales/Service Office and a replacement cable will be provided.

2-9. INSTRUMENT COOLING. The instrument is adequately cooled by normal air circulation. Install the Model 1600A in a location that provides at least 1.5 inches of clearance at the rear and one-inch clearance on both sides of the cabinet.

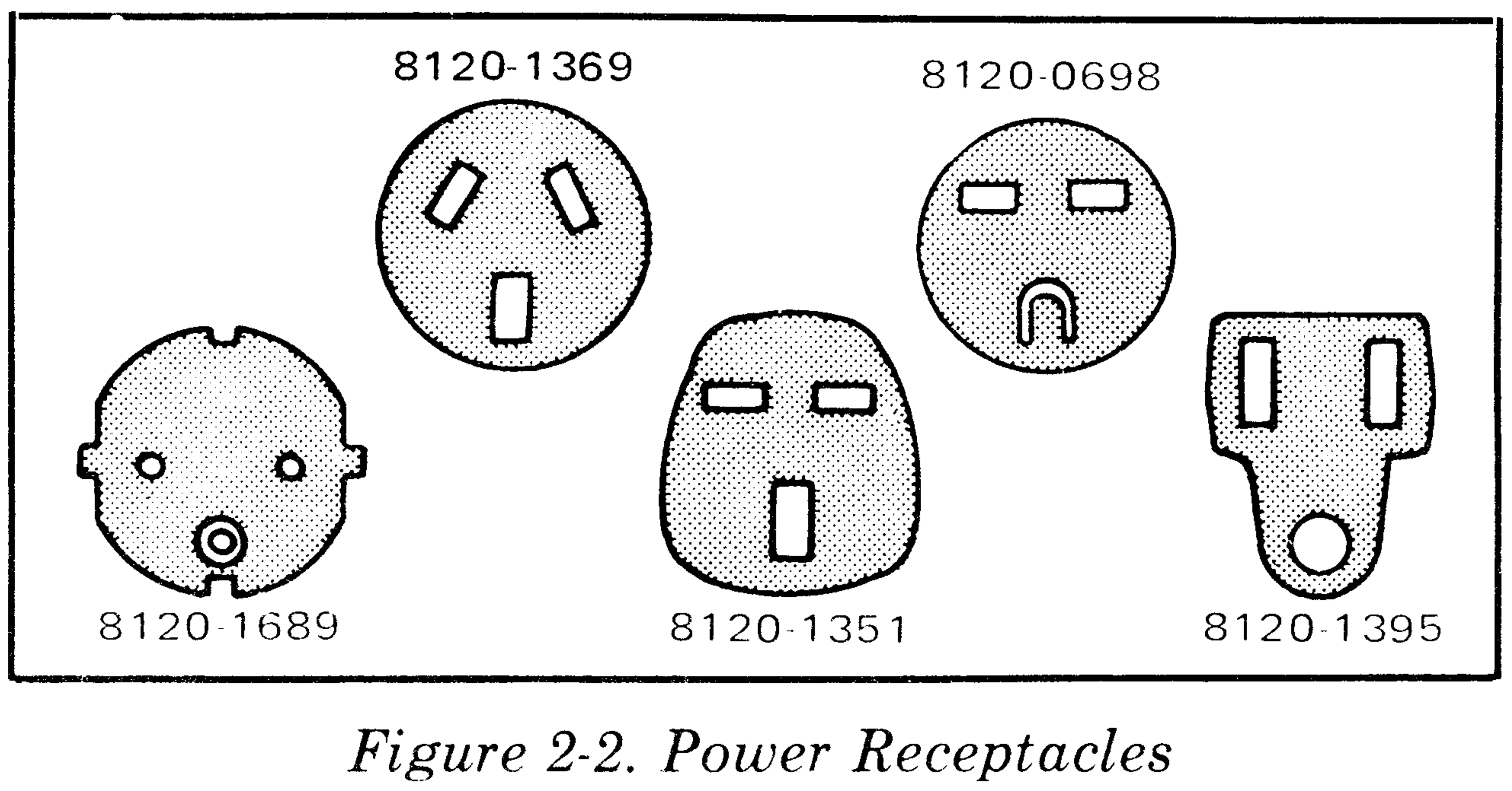


Figure 2-2. Power Receptacles

2-10. CLAIMS.

2-11. The warranty statement applicable to this instrument is printed inside the front cover of this manual. If physical damage is found or if operation is not as specified when the instrument is received, notify the carrier and nearest HP Sales/Service Office immediately (refer to the list in back of this manual for addresses). The HP Sales/Service Office will arrange for repair or replacement without waiting for settlement of the claim with the carrier.

2-12. REPACKING FOR SHIPMENT.

2-13. If the Model 1600A is to be shipped to an HP Sales/Service Office for service or repair, attach a tag showing owner (with address), complete instrument serial number, and a description of the service required.

2-14. Use the original shipping carton and packing material. If the original packing material is not available, the Hewlett-Packard Sales/Service Office will provide information and recommendations on materials to be used.

SECTION III

OPERATION

3-1. INTRODUCTION.

3-2. This section contains an explanation of the Model 1600A operating controls, modes of operation, operator's checks and adjustments, and operating instructions for most applications.

3-3. CONTROLS AND CONNECTORS.

3-4. Figure 3-1 shows the Model 1600A front and rear panels and provides functional descriptions of operating controls, connectors, and indicators.

3-5. CLOCK, DATA, AND QUALIFIER INPUTS.

3-6. Clock, data and qualifier inputs to the Model 1600A are supplied by monitor probes which connect to the front-panel clock and data input connectors. Each monitor probe comprises connecting devices and buffer amplifier-comparators. Input threshold levels for the buffer amplifier-comparators are supplied by the Model 1600A. One clock probe and three six-channel data probes are required to operate the Model 1600A. Refer to the operating and service literature supplied with the probes for further information.

3-7. DISPLAY MODES.

3-8. TABLE DISPLAYS. The Model 1600A has four table display modes; A, A & B, A & (A⊕B), and B. In the table formats, the Model 1600A displays one's and zero's in one or two tables consisting of sixteen 16-bit words each. Table A (left half of the CRT screen) is a display of A-memory data acquired from the circuit under test through the Model 1600A data input connectors. Table B (right half of the CRT screen) is a display of B-memory data (data transferred from A-memory by STORE A→B or Model 1607A input data when the Model 1600A is connected to a Model 1607A using a Model 10237A I/O Interface Cable), or a display of the exclusive-OR of A data and B data.

3-9. In display modes where table A is displayed, the STORE A→B pushbutton duplicates the contents of A-memory in B-memory. This feature allows table B to be used as a reference field enabling analysis on a comparison basis. When the Model 1600A is connected to a Model 1607A through the I/O interface cable, STORE A→B is disabled and table B becomes an active display of Model 1607A input data.

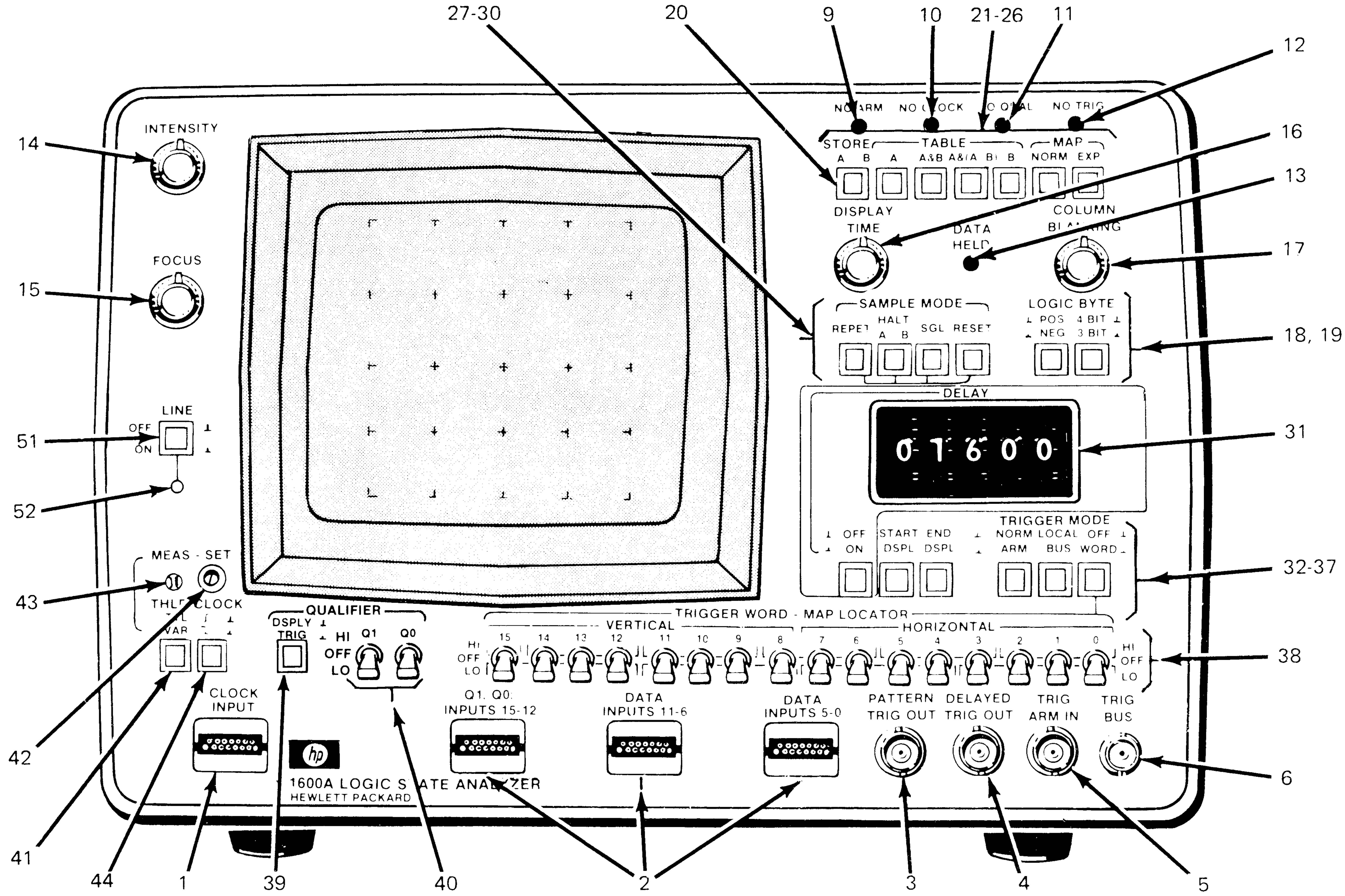
3-10. With A & (A ⊕ B) selected, table B displays the bit-by-bit exclusive-OR of A-memory with B-memory. Bit differences are displayed as intensified one's and bit correlation is displayed as zero's.

3-11. Partial Displays. The partial-display mode permits display of less than 16 words and allows viewing of data as it is single-stepped into the Model 1600A. The Model 1600A will go into a partial-display mode any time the display qualifier rate is less than approximately 30 bits/second. A slow display qualifier rate can be either a low-frequency clock or a high-frequency clock with infrequent display qualification. In the partial-display mode, the Model 1600A displays data words on the CRT as they are received, not waiting until a complete 16-word data block is in memory.

3-12. In START DSPL, the CRT is blanked until the trigger word is found. The trigger word is then displayed and the following words are added to the display with subsequent clocks. In END DSPL, data words are displayed as they are acquired. After 16 words are displayed, each additional clock shifts the display up one word until the trigger word is displayed. The trigger word is intensified and the display is held for the length of time set by DISPLAY TIME. When A & (A ⊕ B) is selected both tables are incremented together in partial-display operation.

3-13. MAP DISPLAYS. The map display provides an overview of A-memory with data words displayed as dots on the CRT screen. All possible states in a 16-bit state machine (up to 65 536 16-bit words) can be displayed in the map mode. In the map display mode, the Model 1600A acquires data randomly, i.e., in a free-run sample mode. However, the pattern- and delayed-trigger outputs function the same in map display modes as they do in table display modes. The DSPLY qualifier mode can be used in map to selectively map input data. In map display modes, the Model 1600A requires repetitive input data with a clock rate or display qualifier rate greater than 100 kHz. At clock rates less than 100 kHz, it is possible that some logic states may not be displayed.

3-14. The position of each dot on the CRT screen uniquely identifies its address or state value. The eight most-significant bits of a 16-bit word determine its vertical position on the CRT screen and the eight least-significant bits determine the horizontal position of the word. The all-zero state is displayed in the upper-left corner of the screen and the all-ones state is displayed in the lower-right corner of the screen (POS logic).



INPUTS/OUTPUTS

1. **CLOCK INPUT.** Clocking signal input connector.

2. **Q1, Q0, INPUTS 15-12; DATA INPUTS 11-6; DATA INPUTS 5-0.** Monitored-data input connectors. Each connector supplies six parallel data channels.

3. **PATTERN TRIG OUT.** Output connector for trigger pulse generated when the input data meets triggering requirements. The trigger pulse remains high until the delay generator produces a pulse on DELAYED TRIG OUT.

4. **DELAYED TRIG OUT.** Output connector for trigger pulse delayed from PATTERN TRIG OUT by the number of display-qualified clock pulses selected by DELAY.

5. **TRIG ARM IN.** Input connector for trigger recognition arming signal.

6. **TRIG BUS.** Connector for trigger bus signal. Connect TRIG BUS to TRIG BUS on a Model 1607A only.

7. **I/O PORT.** Connector for bidirectional data and control signal interface cable between the Model 1600A and a Model 1607A.

8. **LOGIC PROBE.** +5 V power connector for use with logic probes requiring less than 100 mA.

INDICATORS

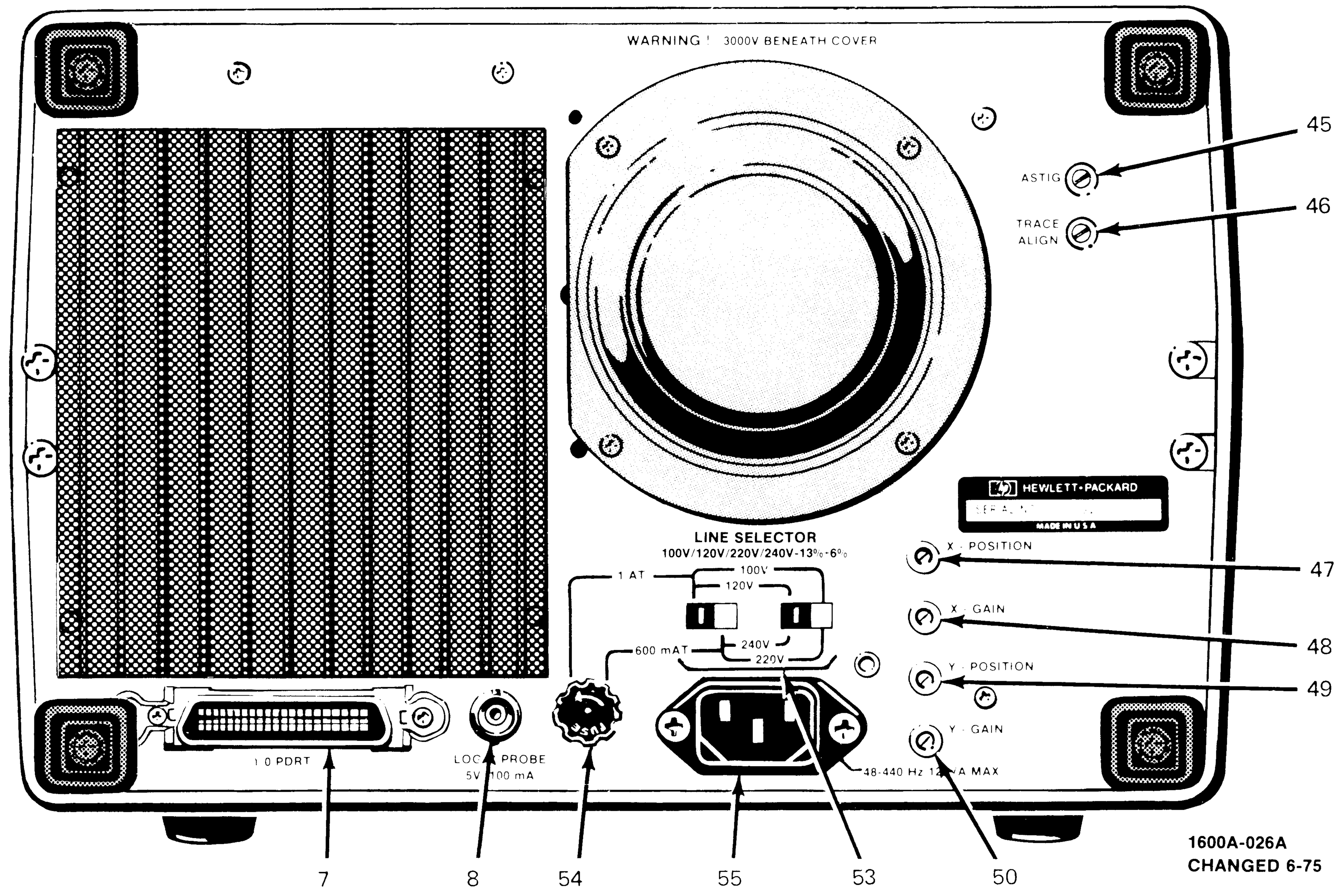
9. **NO ARM.** Indicator light showing when the Model 1600A has remained unarmed for more than approximately 0.1 second.

10. **NO CLOCK.** Indicator light showing that the Model 1600A has not received a clock for more than approximately 0.1 second.

11. **NO QUAL.** Indicator light showing that the Model 1600A has not received a display qualifier for more than approximately 0.1 second. NO QUAL is disabled when the qualifier DSPLY/TRIG pushbutton is set to TRIG or the NO CLOCK light is on.

12. **NO TRIG.** Indicator light showing that the Model 1600A has not received a trigger for

Figure 3-1. Front- and Rear-Panel Controls, Connectors and Indicators



REAR VIEW

more than approximately 0.1 second. NO TRIG is disabled if NO ARM, NO CLOCK or NO QUAL are lit.

13. **DATA HELD.** Indicator light showing that the Model 1600A data has been displayed for more than approximately 0.3 second without being updated.

DISPLAY

14. **INTENSITY.** Controls brightness of display.

15. **FOCUS.** Control for adjusting focus of display.

16. **DISPLAY TIME.** Control to adjust the length of time a display is retained on the CRT before being updated in the REPET and HALT A ≠ B modes.

17. **COLUMN BLANKING.** Control for blanking unused columns. Blanking begins with the most significant bit and the least significant bit cannot be blanked.

18. **LOGIC POS/NEG.** Matches sense of displayed characters to desired logic polarity. POS for positive logic (the most positive level is a 1), or NEG for negative logic (the most negative level is a 1).

19. **BYTE 4 BIT/3 BIT.** 4 BIT groups the 16-bit word format into bytes of 4 bits each. 3 BIT groups the 16-bit word format into bytes of 3 bits each with the MSB left over.

20. **STORE A→B.** Control to load the contents of the A-memory into the B-memory each time the button is pushed. This control functions only when A-memory is displayed as a table.

DISPLAY MODE

21. **TABLE A.** Selects data stored in A-memory (Model 1600A input data) for display on the left side of the CRT screen.

22. **TABLE A & B.** Selects contents of both A-memory and B-memory (auxilliary memory) for display.

23. **TABLE A & (A ⊕ B).** Selects contents of A-memory for display on the left side of the CRT screen and the bit-by-bit exclusive-ORing of the contents of A-memory and B-memory for display on the right side of the CRT screen. The differences between A-memory and B-memory are always displayed as intensified ones, regardless of the LOGIC switch setting.

24. **TABLE B.** Displays data stored in B-memory on right side of CRT screen.

25. **MAP NORM.** Selects the six most-significant vertical bits (bits 15-10) and the six most-significant horizontal bits (bits 7-2) of A-memory data for map display.

26. **MAP EXP.** When set to in position, expands sector of NORM map selected by two most-significant vertical bits (bits 15 and 14) and two most-significant horizontal bits (bits 7 and 6) to full screen display with six least-significant vertical bits (bits 13-8) and six least-significant horizontal bits (bits 5-0) mapped on the display.

SAMPLE MODE

27. **REPET.** With REPET (repetitive) selected, displayed data is updated every 200 ms to five seconds, depending on the setting of DISPLAY TIME.

28. **HALT A ≠ B.** With HALT A ≠ B selected, data is repetitively acquired and displayed as long as the data in A- and B-memories agree. Whenever the data in A-memory is different from the data in B-memory, the Model 1600A goes into a single-sample mode. Data acquisition is resumed when RESET is pushed or REPET is selected. HALT A ≠ B functions only in display modes where A-memory data is displayed.

29. **SGL.** In SGL (single), data is acquired once each time RESET is pressed. The acquired data is displayed until RESET is pressed again.

30. **RESET.** RESET causes the Model 1600A to return immediately to the beginning of a data acquisition cycle.

TRIGGER MODE

31. **DELAY.** IN START DSPL, DELAY sets the number of display-qualified clock pulses the first displayed word is delayed from the trigger word. In END DSPL, DELAY sets the number of display-qualified clock pulses the last displayed word is delayed from the trigger word. In either mode, DELAY sets the number of display-qualified clock pulses DELAYED TRIG OUT is delayed from the trigger word.

32. **DELAY ON/OFF.** Turns the delay generator on or off. The OFF position has the same effect as setting all DELAY thumbwheels to zero.

33. **START DSPL.** When selected, the trigger word is the first (top) displayed word and the next 15 qualified input clocks enter the remaining 15 displayed words in memory. (DELAY off).

34. **END DSPL.** When selected, trigger word is last (bottom) word displayed with preceding 15 qualified words displayed above.

35. **NORM/ARM.** In ARM position, the trigger recognition circuit cannot produce a trigger until it has been armed by a positive-going transition on the TRIG ARM input. In NORM position, a trigger is produced any time trigger word and qualifier conditions are met.

36. **LOCAL/BUS.** In LOCAL position the Model 1600A will trigger whenever the incoming data meets the Model 1600A local triggering requirements, regardless of the status of other instruments on the trigger bus. In BUS position, a trigger is generated only when the incoming data on both bussed instruments match the settings of their combined TRIGGER WORD switches. When trigger bus cable is disconnected, Model 1600A functions in local mode regardless of switch setting.

37. **OFF/WORD.** In a table display mode, the OFF position (out) disables the 16 TRIGGER WORD switches (equivalent to placing all TRIGGER WORD switches in the off position). In a map display mode, the OFF position removes the cursor (map locator) from the CRT screen and allows only the upper left sector (LOGIC set to POS) or lower right sector (LOGIC set to NEG) of the map to be expanded. OFF/WORD has no effect on qualifier channels.

38. **TRIGGER WORD-MAP LOCATOR.** Control switches for selecting trigger word in table display modes or for locating the cursor (map locator) on the CRT screen in map display modes. OFF is a "don't care" position in table display modes and a LO or zero position in map display modes. Switches select trigger word for PATTERN TRIG OUT and DELAYED TRIG OUT in both table and map display modes.

QUALIFIER

39. **DSPLY/TRIG.**
    a. DSPLY. Prohibits Model 1600A from displaying data or generating a trigger unless the conditions set by Q0 and Q1 are true when the clock edge occurs.
    b. TRIG. Prohibits the Model 1600A from generating a trigger unless the conditions set by Q0 and Q1 are true.

40. **Q0, Q1.** Control switches for setting the pattern that the qualifier bits must match for data to be displayed or a trigger to be generated. OFF is a "don't care" position.

THRESHOLD

41. **THLD TTL/VAR.**
    a. TTL. Sets input threshold of the clock and data probes to +1.5 V.
    b. VAR. Allows input threshold of the clock and data probes to be varied from —10 V to +10 V.

42. **SET.** Screwdriver adjustment for adjusting the probe input threshold voltage over a range of ±10 V.

43. **MEAS.** Test point for monitoring SET threshold level.

44. **CLOCK.** Pushbutton selection of clock transition triggering. Out position selects positive-going transition and in position selects negative-going transition.

CRT ADJUSTMENTS

45. **ASTIG.** Screwdriver adjustment for roundness of writing spot.

46. **TRACE ALIGN.** Screwdriver adjustment for aligning display with horizontal graticule.

47. **X-POSITION.** Screwdriver adjustment for adjusting horizontal position of display.

48. **X-GAIN.** Screwdriver adjustment for gain of horizontal display circuitry output.

49. **Y-POSITION.** Screwdriver adjustment for adjusting vertical position of display.

50. **Y-GAIN.** Screwdriver adjustment for gain of vertical display circuitry output.

POWER

51. **LINE.** Model 1600A line power switch.

52. **Line Lamp.** Lights when instrument is on.

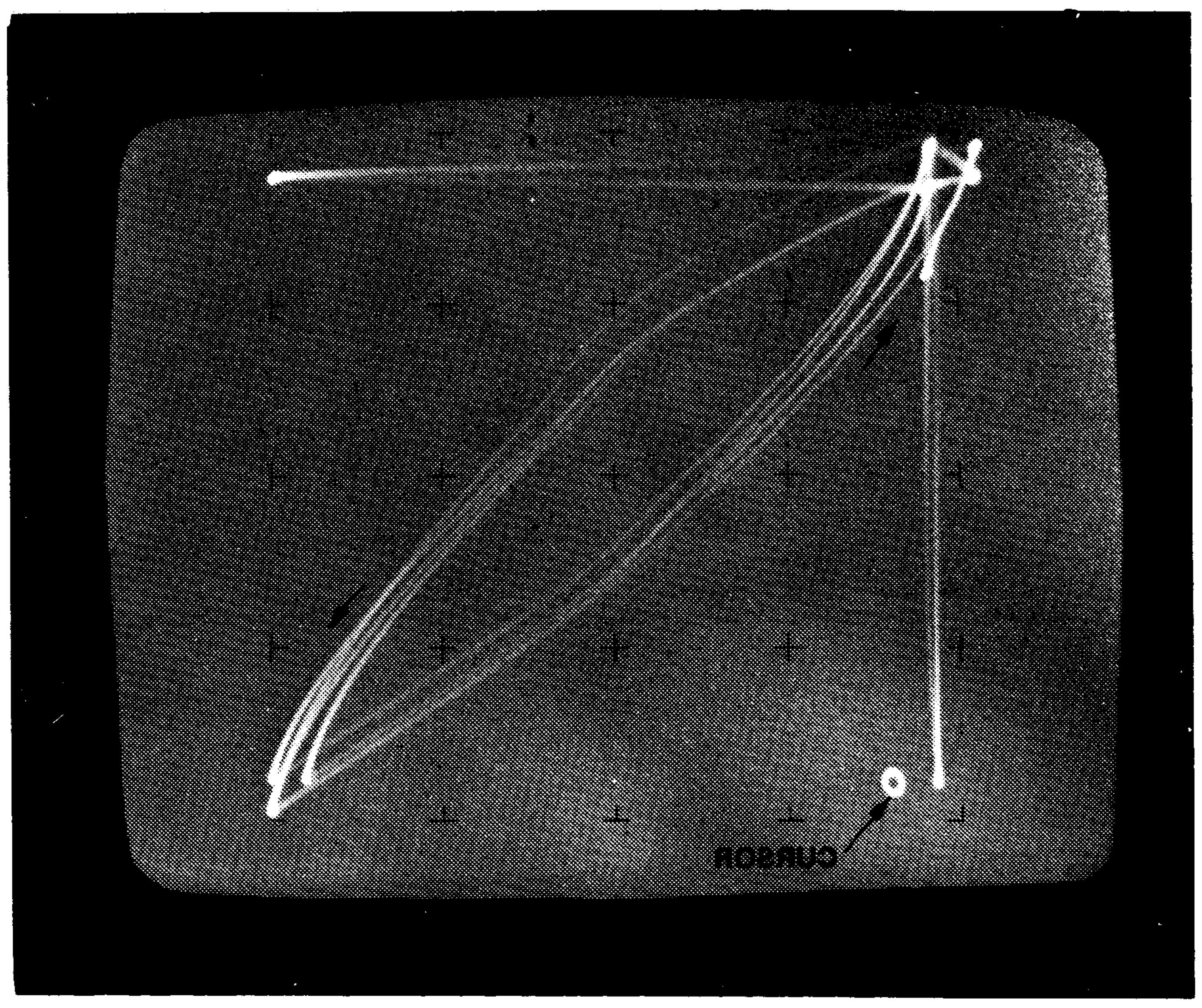
53. **LINE SELECTOR.** Slide switches for selecting 100-, 120-, 220-, or 240-Vac line operation.

54. **FUSE.** 1-A time-delay fuse for 100- or 120-Vac operation, 600-mA time-delay fuse for 220- or 240-Vac operation.

55. **Power Input.** Power cable connector.

Figure 3-1. Front- and Rear-Panel Controls, Connectors, and and Indicators (Cont'd)

3-15. The intensity of a dot indicates the relative frequency of occurrence of that logic state. The vector traced between dots indicate direction of logic flow in the machine. The brightened or intensified end of the vector indicates the "go to" state. The vectors are non-linear so that when logic flow occurs in opposite directions between two logic states, the vectors will not overlap and obscure useful information. Figure 3-2 shows a typical map display.

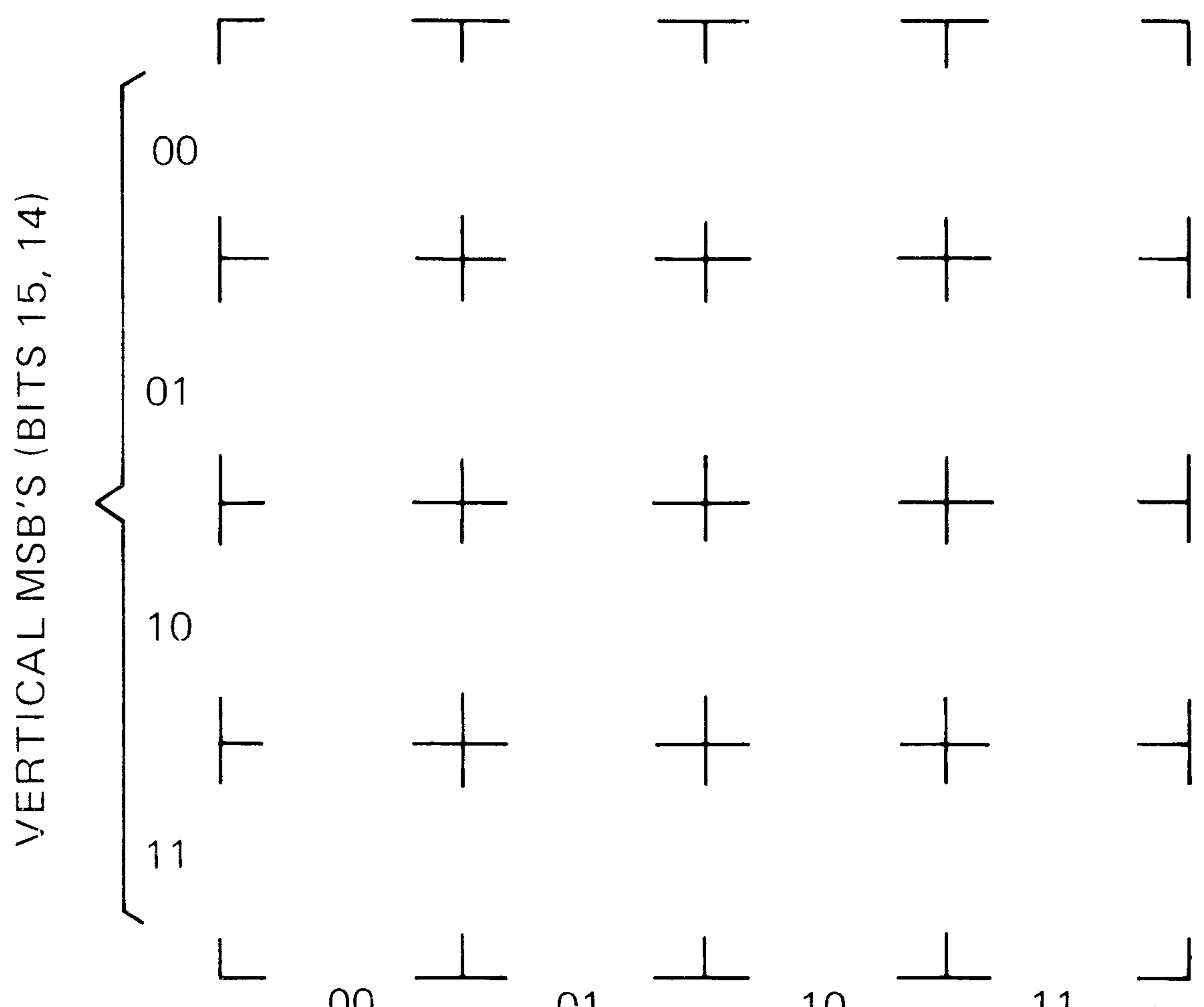


1600A-027

Figure 3-2. Map Display

3-16. NORM/EXP. With Norm selected, the six most-significant vertical bits (bits 15-10) and the six most-significant horizontal bits (bits 7-2) of a data word are mapped on the CRT. In EXP, the sector of the NORM map selected by the two most-significant vertical bits (bits 15 and 14) and the two most-significant horizontal bits (bits 7 and 6) is expanded to full screen. The six least-significant vertical bits (bits 13-8) and the six least-significant horizontal bits of the input data words are mapped on the display in EXP. EXP provides a X4 magnification of the expanded NORM map sector.

3-17. CURSOR. In the map mode, the TRIGGER WORD switches control the location of a cursor (a zero displayed on the CRT screen). In NORM, the cursor is used to select one of 16 sectors to be expanded in EXP. TRIGGER WORD switches 15 and 14 control vertical sector selection; switches 7 and 6 control horizontal sector selection (see figure 3-3). The sector containing the cursor is expanded in EXP. In EXP, the cursor can be used to select a specific state to be the trigger word in a table display. The cursor is positioned about a single dot using the six least-significant vertical and the six least-significant horizontal TRIGGER WORD switches. The setting on the switches give the address or state of the selected dot. Selecting one of the table modes where table A is displayed returns the Model 1600A to a table display with the selected logic state becoming the trigger word.



1600A-032

Figure 3-3. Expanded Map Sector Selection

NOTE

Changing the setting of the two most-significant vertical or two most-significant horizontal TRIGGER WORD switches while in EXP will cause a different sector of the NORM map to be displayed.

3-18. SAMPLE MODES.

3-19. In the repetitive (REPET) sampling mode displayed data is periodically updated approximately every 200 milliseconds to five seconds depending on the setting of the DISPLAY TIME control. In the single-shot (SGL) sampling mode new data is not displayed until the RESET button is pushed. Then new data is acquired and displayed until RESET is pushed again.

NOTE

If control settings are changed in SGL mode, the intensified word may not necessarily be the trigger word.

3-20. In the HALT A ≠ B mode, data is repetitively acquired and displayed as long as the data in A- and B-memories are the same. Whenever the data stored in A-memory differs from the data stored in B-memory, the Model 1600A locks in a display cycle. The Model 1600A then displays the acquired data until reset. Data acquisition is resumed when RESET is pushed or REPET is selected. HALT A ≠ B functions only in modes where table A is displayed. This sample mode frees the operator from watching for very infrequent or intermittent logic sequence errors.

3-21. TRIGGER MODES.

3-22. START DISPLAY. IN START DSPL, the triggering word (the input data word matching the TRIGGER WORD settings) is positioned at the top of the display with the next 15 input data words positioned in order below the triggering word when zero delay is selected.

3-23. END DISPLAY. In END DSPL, the 15 input data words preceding the triggering word are displayed in order from the top of the display with the triggering word positioned at the bottom when zero delay is selected.

3-24. DELAY. With DELAY ON/OFF in the ON position any 16-word data block from 0 to 99 999 qualified input clock pulses following the triggering word can be selected for display. In START DSPL, DELAY sets the number of qualified clock pulses the first displayed word is delayed from the trigger word. In END DSPL, DELAY sets the number of qualified clock pulses the last displayed word is delayed from the trigger word. In either mode, DELAY sets the number of qualified clock pulses the DELAYED TRIG OUT pulse is delayed from the trigger word. Setting DELAY ON/OFF to OFF is equivalent to setting all DELAY thumbwheels to zero.

3-25. NORM/ARM. In NORM position, a trigger is produced any time the Model 1600A trigger word and qualifier conditions are met. In ARM position, the Model 1600A trigger generator cannot produce a trigger pulse until it has been armed by a positive-going transition on the TRIG ARM input. NORM/ARM permits selection of a trigger point that is dependent upon previously specified conditions (sequential triggering). EXAMPLE: The TRIG ARM input could be the PATTERN TRIG OUT or DELAYED TRIG OUT pulse from another Model 1600A or a Model 1607A.

3-26. LOCAL/BUS. In LOCAL position, the Model 1600A will trigger whenever the incoming data meets Model 1600A triggering requirements. In BUS position, a trigger is generated only when the incoming data on both instruments connected to the trigger bus match the settings of their respective TRIGGER WORD switches. This feature allows two instruments to be bussed together to form up to a 32-bit-wide trigger (36-bits wide with TRIG qualification selected) enabling larger word-size machines to be analyzed.

3-27. QUALIFIER MODES.

3-28. Display qualification prohibits the Model 1600A from recognizing any clock input unless the conditions set by Q0 and Q1 are true. On bus structures where data is being multiplexed such as in computers or microprocessors, display qualification permits selective viewing of data by ignoring unqualified clock edges. Trigger qualification prohibits the Model 1600A from generating a trigger unless the conditions set by Q0 and Q1 are true. With trigger qualification, Q0 and Q1 become two additional undisplayed channels, i.e., the trigger word becomes 18 bits wide.

3-29. When the DSPLY/TRIG switch is set to DSPLY, the Model 1600A will display only that data that is properly qualified when a clock occurs. When TRIG is selected, the instrument triggers on an 18-bit trigger word.

3-30. PATTERN TRIG OUT / DELAYED TRIG OUT.

3-31. PATTERN TRIG OUT and DELAYED TRIG OUT provide 50-ohm-compatible trigger outputs. PATTERN TRIG OUT provides a pulse when the Model 1600A input data meets triggering requirements. The PATTERN TRIG OUT pulse remains high until the delay generator produces a pulse on DELAYED TRIG OUT. DELAYED TRIG OUT is delayed from PATTERN TRIG OUT by the number of display-qualified clock pulses selected by the DELAY thumbwheels. With zero delay selected, the pattern trigger is an RZ pulse approximately 25 nanoseconds wide.

3-32. DISPLAY FEATURES.

3-33. The following controls enable the Model 1600A operator to select the most usable display for his application.

3-34. DISPLAY TIME. The DISPLAY TIME control determines the length of time a given 16-word data block is displayed on the CRT before being updated by new input data. The time between data block updates can be set from approximately 200 ms (fully ccw) to approximately five seconds (fully cw). DISPLAY TIME is used to reduce display flicker at low data acquisition rates.

3-35. COLUMN BLANKING. The COLUMN BLANKING control is adjusted to eliminate unused vertical columns on the display. Blanking begins with the most-significant-bit column. The least-significant bit cannot be blanked. EXAMPLE: When monitoring a series of eight-bit data words, the eight unused vertical columns can be removed from the CRT display by adjustment of COLUMN BLANKING.

3-36. LOGIC NEG/POS. The POS position (out) causes the most positive input voltage level to be displayed as a one, and the most negative level to be displayed as a zero. In NEG (in position), the most negative input level is displayed as a one, and the most positive level is displayed as a zero.

3-37. BYTE 4 BIT/3 BIT. In the 4 BIT (BCD or hexadecimal format) position (out) display data is arranged into four-bit bytes. In the 3-BIT (octal format) position (in) display data is arranged into three-bit bytes with the MSB left over.

3-38. BUS OPERATION.

NOTE

A Model 10236A Trigger Interface Cable and a Model 10237A I/O Interface Cable are required to bus the Model 1600A with a Model 1607A.

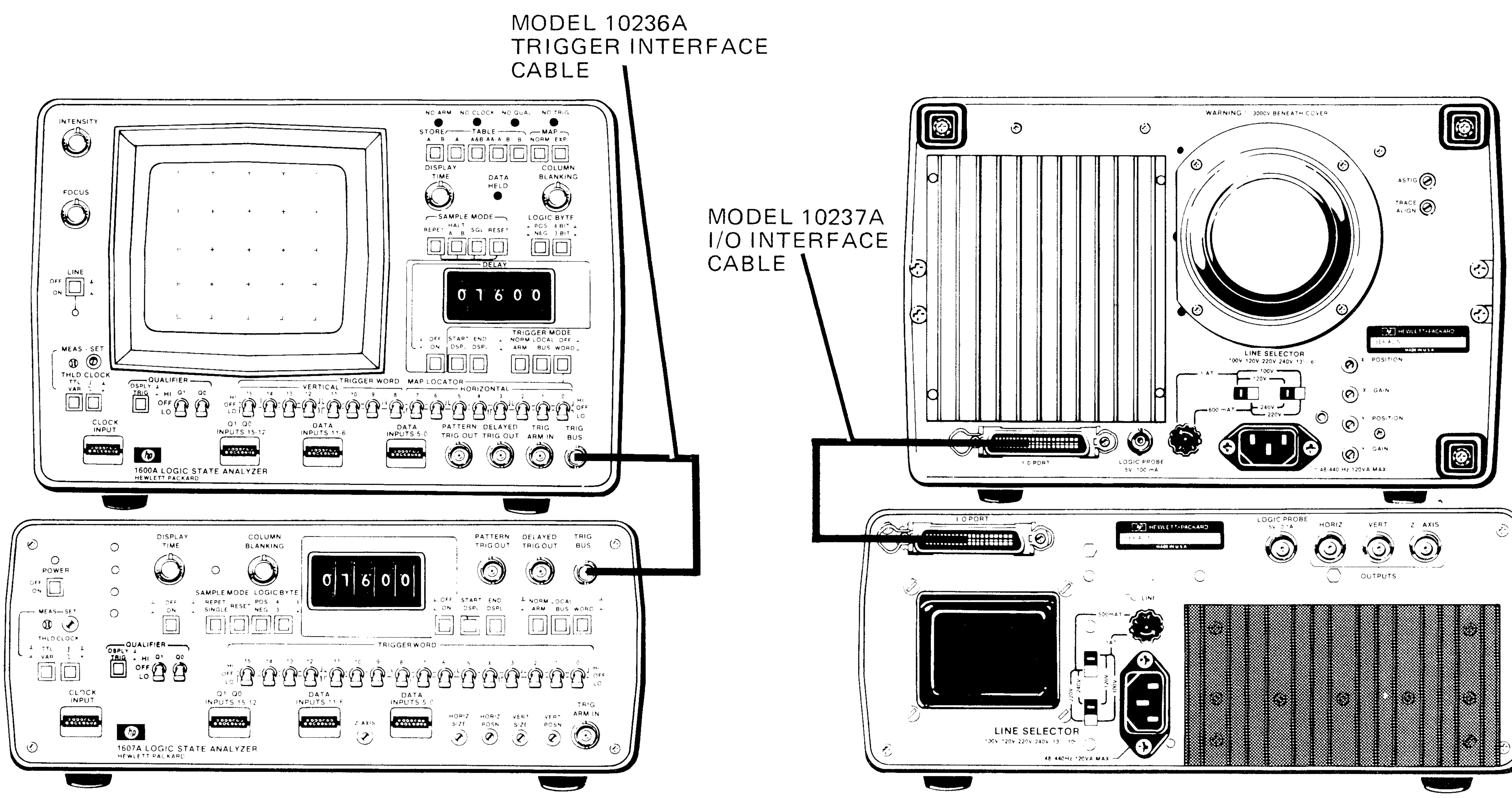
3-39. There are two buses in the Model 1600A and Model 1607A. The trigger bus (TRIG BUS) is used to expand triggering capability and the I/O bus (I/O PORT) is used to transfer and control display information. Figure 3-4 shows a Model 1600A and a Model 1607A configured for bus operation.

3-40. TRIGGER BUS. The trigger bus permits the Model 1600A and a Model 1607A to be connected together to form a 32 bit trigger word. Trigger-bus operation is controlled by the LOCAL/BUS switch. In LOCAL position, the instrument will trigger whenever the monitored data meets the instrument's local triggering requirements, regardless of the status of the other instrument on the bus. With LOCAL/BUS set to BUS, the instrument will generate a trigger only when the data monitored by both bused instruments is in agreement with their composite trigger word.

3-41. I/O BUS. Whenever the Model 1600A and Model 1607A are connected together with the I/O interface cable, they automatically go into I/O bus operation. In I/O bus operation, the combined instruments perform as a 32-bit logic state analyzer with table A data provided by the Model 1600A and table B provided by the Model 1607A. STORE A→B is disabled in I/O bus operation.

3-42. With the I/O bus connected, the combined instruments can be operated with either a single clock or two independent clocks. Using a single clock, the Model 1600A can display one table of sixteen 32-bit words or two tables of sixteen 16-bit words each. Thirty-two sequential 16-bit words can be displayed by setting LOCAL/BUS on both instruments to LOCAL and triggering the Model 1607A on the word occuring 16 clock pulses after the Model 1600A trigger word. With dual-clock operation, "handshake" operations between two independent machines can be observed on the same display with 16 channels devoted to each machine and independent clocks for each machine.

NOTE: DATA IS TRANSFERRED BETWEEN INSTRUMENTS ON MODEL 10237A DATA INTERFACE CABLE REGARDLESS OF LOCAL/BUS SWITCH POSITION.



A. TRIGGER BUS OPERATION SETUP

B. I/O BUS OPERATION SETUP

1600A-028A
CHANGED 6-75

CONNECT MODEL 10236A TRIGGER INTERFACE CABLE BETWEEN TRIG BUS CONNECTORS ON INSTRUMENT FRONT PANELS

CONNECT MODEL 10237A I/O INTERFACE CABLE BETWEEN I/O PORT CONNECTORS ON INSTRUMENT REAR PANELS.

Figure 3-4. Model 1600A/1607A Bus Configuration

3-43. BUS OPERATING MODES. Table 3-1 provides a summary of the operating modes available when the Model 1600A and Model 1607A are operated in the bus configuration. Either single or dual clocks can be used with any of operating modes listed.

3-44. FRONT-PANEL CONTROLS. The Model 1600A and Model 1607A controls and indicators function in the same manner in I/O bus operation as they do when the instruments are operated separately with the following exception: The Model 1600A DISPLAY TIME controls both instruments in the bus mode. Both completed tables must be displayed for the time set by DISPLAY TIME before they can be reset. With dual-clock operation, it is possible for one table to be displayed for an extended period of time while waiting for the other table to be completed. Upon completion of the second table, both tables are displayed for the time set by DISPLAY TIME before another data acquisition cycle begins.

3-45. RESET. As shipped from the factory, the Model 1600A RESET pushbutton controls only the Model 1600A. If it is desirable to control both the Model 1600A and the Model 1607A with the Model 1600A RESET, the Model 1607A may be modified by the user to accomplish this. A detailed procedure is provided in Section V of the Model 1607A Operating and Service Manual.

3-46. 32-BIT WORD DISPLAY. The Model 1600A displays two 16-bit wide tables in the A & B and A & (A ⊕ B) modes as shipped from the factory. If it is desirable to display one 32-bit wide table on the CRT in proper octal format (ten 3-bit bytes with the two MSB left over), see the procedure for modifying the Model 1600A provided in Section V.

3-47. OPERATOR'S CHECKS AND ADJUSTMENTS.

3-48. Perform the operator's preoperational checks and adjustments as follows:

NOTE

Clock and data probes need not be connected for this procedure.

a. Set Model 1600A controls as follows:

POWER	OFF
TRIGGER WORD - MAP LOCATOR	all switches OFF
Sample Mode	SGL
Display Mode	A & B
COLUMN BLANKING	full CCW
WORD	ON
Trigger Mode	START DSPL
DELAY ON/OFF	OFF
All Other Pushbuttons	out position

b. Apply Power. Display should show two 16-word tables of one's and zero's with first word in table A intensified.

c. Select A display mode. Observe that table A remains displayed and table B blanks.

Table 3-1. Model 1600A/Model 1607A Bus Modes

I/O BUS	TRIGGER BUS	LOCAL/BUS SETTING MODEL 1600A	LOCAL/BUS SETTING MODEL 1607A	MODEL 1600A TABLE DISPLAY A	MODEL 1600A TABLE DISPLAY B	TRIGGER REQUIREMENTS (TRIGGER WORD MATCH) MODEL 1600A	TRIGGER REQUIREMENTS (TRIGGER WORD MATCH) MODEL 1607A
No	Yes	LOCAL	BUS	1600A Data	Stored Data	1600A Word Only	1600A•1607A
No	Yes	BUS	LOCAL	1600A Data	Stored Data	1600A•1607A	1607A Word Only
No	Yes	BUS	BUS	1600A Data	Stored Data	1600A•1607A	1600A•1607A
Yes	Yes	LOCAL	BUS	1600A Data	1607A Data	1600A Word Only	1600A•1607A
Yes	Yes	BUS	LOCAL	1600A Data	1607A Data	1600A•1607A	1607A Word Only
Yes	Yes	BUS	BUS	1600A Data	1607A Data	1600A•1607A	1600A•1607A
Yes	Yes	LOCAL	LOCAL	1600A Data	1607A Data	1600A Word Only	1607A Word Only
Yes	No	NA*	NA*	1600A Data	1607A Data	1600A Word Only	1607A Word Only

*NA = Not Applicable

d. Select B display mode. Observe that table A blanks and table B is displayed.

e. Select A & (A ⊕ B). Observe that both tables are displayed, and table B displays intensified one's where A-memory and B-memory data differ. (If A- and B-memory data are the same, table B will display all zero's.)

f. Press STORE A→B. Observe that table B displays all zeros.

g. Select A & B display mode. Observe that table A and table B are identical.

h. Select NORM map display. Observe that intensified dots with inter-connecting lines are displayed on CRT screen. An oval (cursor) will be displayed in upper left corner with OFF/WORD in word position (in).

i. Verify that TRIGGER WORD switches 2 through 7 will move cursor horizontally and TRIGGER WORD switches 10 through 15 will move cursor vertically.

j. Use TRIGGER WORD switches to locate cursor on intensified dot or dots and depress map EXP.

k. Switch two least-significant vertical and horizontal TRIGGER WORD switches (bits 0, 1 and 8, 9) to locate cursor about one of intensified dots.

l. Set display mode to table A & B.

m. Set BYTE to 3 BIT and observe that display format changes from four-bit bytes to three-bit bytes.

n. Set LOGIC to NEG and observe that all zeros change to ones, and that all ones change to zeros.

o. Rotate COLUMN BLANKING cw and observe that vertical columns are blanked starting with most significant bit (MSB).

p. Rotate COLUMN BLANKING fully cw and observe that least-significant bit (LSB) column remains on CRT.

q. Rotate COMUMN BLANKING fully ccw.

r. Set trigger mode to START DSPL and observe that first word is intensified.

s. Set Trigger Mode to END DSPL and observe that last word is intensified.

t. Set DELAY ON/OFF to ON. Observe that setting DELAY thumbwheels from 0 to 15 will move intensified word on display. Observe that intensified word is not displayed for delays greater than 15.

3-49. OPERATING PROCEDURE.

3-50. The Model 1600A operating procedure is provided in a flow-diagram format in figure 3-5.

1. CONNECT CLOCK AND DATA MONITOR PROBES TO CIRCUITRY UNDER TEST.

2. SELECT CLOCK SLOPE.

SET CLOCK (44) TO MATCH CLOCK PULSE TRIGGERING REQUIREMENTS OF CIRCUITRY UNDER TEST: OUT POSITION FOR POSITIVE-EDGE TRIGGERING, IN POSITION FOR NEGATIVE-EDGE TRIGGERING.

3. SELECT THRESHOLD.

SET THLD (41) TO MATCH THRESHOLD OF CIRCUITRY UNDER TEST. SELECT TTL WHEN LOGIC THRESHOLD IS +1.5 V. FOR OTHER THRESHOLD LEVELS, SELECT VAR AND ADJUST SET TO THRESHOLD OF SYSTEM UNDER TEST USING DVM CONNECT TO MEAS OR ADJUST SET TO CENTER RANGE WHERE NO CLOCK LIGHT IS OUT.

4. ADJUST DISPLAY TIME AND COLUMN BLANKING CONTROLS FULLY CCW.

5. SELECT DISPLAY MODE

A 21
SELECT A TO DISPLAY MODEL 1600A INPUT DATA STORED IN A-MEMORY ON THE LEFT SIDE OF CRT SCREEN. B-MEMORY DISPLAY (RIGHT SIDE OF CRT SCREEN) IS BLANKED.

A & B 22
SELECT A & B TO DISPLAY A-MEMORY DATA ON THE LEFT SIDE OF THE CRT SCREEN AND B-MEMORY DATA ON THE RIGHT SIDE OF THE SCREEN. WHEN BUSSED WITH A MODEL 1607A LOGIC ANALYZER, MODEL 1607A DATA IS DISPLAYED IN THE RIGHTHAND TABLE.

A & (A⊙B) 23
SELECT A & (A⊙B) TO DISPLAY A-MEMORY DATA ON THE LEFT SIDE OF THE CRT SCREEN AND THE BIT-BY-BIT EXCLUSIVE ORING OF A- AND B-MEMORY DATA ON THE RIGHT SIDE OF THE CRT SCREEN. DIFFERENCES BETWEEN A- AND B-MEMORY CONTENTS ARE DISPLAYED AS INTENSIFIED ONE'S.

B 24
SELECT B TO DISPLAY B-MEMORY CONTENTS ON RIGHT SIDE OF CRT SCREEN. A-MEMORY DISPLAY (LEFT SIDE OF CRT SCREEN) IS BLANKED.

MAP NORM 25
SELECT NORM TO DISPLAY SIX MOST SIGNIFICANT VERTICAL BITS (BITS 15-10) AND SIX MOST SIGNIFICANT HORIZONTAL BITS (BITS 7-2) OF A-MEMORY DATA IN MAP FORMAT.

MAP EXP 26
SELECT EXP TO DISPLAY SIX LEAST SIGNIFICANT VERTICAL BITS (BITS 13-6) AND SIX LEAST SIGNIFICANT HORIZONTAL BITS (BITS 5-0) OF A-MEMORY DATA IN MAP FORMAT. EXP EXPANDS ONE-SIXTEENTH OF NORMAL MAP SELECTED BY TWO MSB OF VERTICAL (BITS 15, 14) AND HORIZONTAL (BITS 7, 6) DATA TO FULL SCREEN.

6. SELECT SAMPLE MODE.

REPET 27
SELECT REPET TO RESET DISPLAY REPETITIVELY AT A RATE SET BY DSPL TIME NEW DATA IS DISPLAYED WHEN SYSTEM UNDER TEST MEETS TRIGGERING REQUIREMENTS (WHEN INPUT DATA WORD MATCHES SELECTED TRIGGER WORD IN SYNC WITH A CLOCK INPUT AND QUALIFIER CONDITIONS ARE TRUE).

HALT A ≠ B 28
SELECT HALT A ≠ B TO CAUSE MODEL 1600A TO OPERATE IN REPET MODE UNTIL A DIFFERENCE IS DETECTED BETWEEN TABLE A AND TABLE B. THE MODEL 1600A THEN GOES INTO SINGLE SAMPLE MODE UNTIL RESET IS DEPRESSED.

SGL 29
SELECT SGL TO CAUSE MODEL 1600A TO ACQUIRE AND DISPLAY ONE 16-WORD BLOCK OF DATA UNTIL RESET IS DEPRESSED.

RESET 30
PUSH RESET TO CAUSE THE MODEL 1600A TO IMMEDIATELY RETURN TO THE BEGINNING OF A DATA ACQUISITION CYCLE.

7. SELECT TRIGGER MODE.

DELAY 31
SET NUMBER OF CLOCK PULSES DISPLAY AND DELAYED TRIG OUT ARE TO BE DELAYED FROM SELECTED TRIGGER WORD. IN START DSPL MODE, START OF DISPLAY IS DELAYED FROM TRIGGER WORD BY DELAY SETTING. IN END DSPL MODE, END OF DISPLAY IS DELAYED FROM TRIGGER WORD BY DELAY SETTING.

DELAY ON/OFF 32
SELECT IN POSITION TO TURN DELAY GENERATOR ON. OFF POSITION HAS SAME EFFECT AS SETTING ALL DELAY THUMBWHEEL SWITCHES TO ZERO.

START DSPL 33
SELECT START DSPL TO DISPLAY TRIGGERING WORD (POSITIONED AT TOP OF DISPLAY) AND FOLLOWING 15 INPUT DATA WORDS.

END DSPL 34
SELECT END DSPL TO DISPLAY TRIGGERING WORD (POSITIONED AT BOTTOM OF DISPLAY) AND PRECEDING 15 INPUT DATA WORDS.

NORM/ARM 35
SELECT NORM TO ALLOW TRIGGER GENERATOR TO PRODUCE A TRIGGER WHENEVER THE TRIGGER WORD AND QUALIFIER CONDITIONS ARE MET. SELECT ARM TO INHIBIT TRIGGER GENERATOR FROM PRODUCING A TRIGGER UNTIL IT HAS BEEN ARMED BY A POSITIVE-GOING TRANSITION ON THE TRIG ARM INPUT.

LOCAL/BUS 36
SELECT LOCAL TO OBTAIN A TRIGGER ANYTIME THE MODEL 1600A INPUT DATA MEETS TRIGGERING REQUIREMENTS. SELECT BUS WHEN THE MODEL 1600A IS TO BE USED WITH A MODEL 1607A. IN BUS, A TRIGGER IS GENERATED ONLY WHEN BOTH THE MODEL 1600A TRIGGER REQUIREMENTS AND THE MODEL 1607A TRIGGER REQUIREMENTS ARE MET.

WORD 37
SELECT ON POSITION TO ENABLE TRIGGER WORD SWITCHES. IN A TABLE MODE THE OFF POSITION EFFECTIVELY PLACES ALL TRIGGER WORD SWITCHES IN THE OFF OR DON'T CARE POSITION. IN A MAP MODE, THE OFF POSITION REMOVES THE CURSOR FROM THE CRT IN MAP AND ALLOWS ONLY THE UPPER LEFT (LOGIC SET TO POS) OR LOWER RIGHT (LOGIC SET TO NEG) SECTOR TO BE EXPANDED.

WORD ON

8. SELECT TRIGGER WORD OR MAP LOCATOR

TABLE MODES
SET SWITCHES TO MATCH REQUIRED TRIGGERING WORD OF INPUT DATA STREAM. HI TO RECOGNIZE A POSITIVE LOGIC STATE, LO TO RECOGNIZE A NEGATIVE LOGIC STATE, OR OFF FOR A NON-REQUIRED INPUT.

MAP MODES
USE THE TWO MOST SIGNIFICANT VERTICAL BITS (BITS 15, 14) AND TWO MOST SIGNIFICANT HORIZONTAL BITS (BITS 7, 6) TO SELECT ONE OF 16 SECTORS OF DISPLAY TO BE EXPANDED IN EXP MODE. USE REMAINING BITS TO LOCATE CURSOR ABOUT WORD OF INTEREST.

9. SELECT QUALIFIER MODE.

DSPLY 39
SELECT CLOCK (OUT POSITION) TO SELECTIVELY DISPLAY DATA WHEN THE TWO-BIT QUALIFIER CONDITION IS MET. IF THE QUALIFIER CONDITION IS NOT MET, THE MODEL 1600A IGNORES THE DATA FROM THE CIRCUIT UNDER TEST. THE DSPLY QUALIFIER ALLOWS COMPRESSION OF DATA FOR DISPLAY.

TRIG 39
SELECT TRIG (IN POSITION) TO USE QUALIFIER AS EXTERNAL SYNCHRONOUS TRIGGER OR TO EXPAND THE LENGTH OF THE TRIGGER RECOGNITION WORD TO 18 BITS.

10. SELECT QUALIFIER.

SET QUALIFIER SWITCHES Q0 AND Q1 TO MATCH REQUIRED TRIGGERING BITS OF INPUT DATA. HI TO RECOGNIZE A POSITIVE LOGIC STATE, LO TO RECOGNIZE A NEGATIVE LOGIC STATE, OR OFF FOR A NON-REQUIRED INPUT.

NOTE: NUMBERS FOLLOWING CONTROL NAMES REFER TO FIGURE 3-1 CALLOUTS.

11. SET UP DISPLAY FEATURES.

DISPLAY TIME 16
ADJUST FOR MAXIMUM USABLE FLICKER RATE. WHEN THE MODEL 1600A IS BUSSED WITH A MODEL 1607A, THE MODEL 1600A DISPLAY TIME CONTROL CONTROLS BOTH INSTRUMENTS.

COLUMN BLANKING 17
ADJUST TO BLANK OUT NON-REQUIRED VERTICAL COLUMNS. WHEN THE MODEL 1600A IS OPERATED WITH A MODEL 1607A IN THE I/O BUS MODE, TABLE A COLUMN BLANKING IS CONTROLLED BY THE MODEL 1600A AND TABLE B IS CONTROLLED BY THE MODEL 1607A.

LOGIC POS/NEG 18
SET TO POS TO DISPLAY MOST POSITIVE INPUT LOGIC LEVEL AS A 1. SET TO NEG TO DISPLAY MOST NEGATIVE INPUT LOGIC LEVEL AS A 1. WHEN THE MODEL 1600A IS OPERATED WITH A MODEL 1607A IN THE I/O BUS MODE, TABLE A LOGIC IS CONTROLLED BY THE MODEL 1600A AND TABLE B LOGIC IS CONTROLLED BY THE MODEL 1607A.

BYTE 4 BIT/3 BIT 19
SELECT 4 BIT (OUT POSITION) TO DISPLAY 4-BIT BYTES. SELECT 3-BIT (IN POSITION) TO DISPLAY 3-BIT BYTES (OCTAL FORMAT). WHEN THE MODEL 1600A IS OPERATED WITH A MODEL 1607A IN THE I/O BUS MODE, MODEL 1600A BYTE CONTROLS TABLE A, MODEL 1607A BYTE CONTROLS TABLE B.

STORE A→B 20
PRESS STORE A→B TO LOAD CONTENTS OF A-MEMORY INTO B-MEMORY. STORE A→B FUNCTIONS ONLY IN MODE WHERE A-MEMORY IS DISPLAYED AS A TABLE. STORE A→B IS DISABLED IN I/O BUS OPERATION.

1600A-031A
CHANGED 6-75

Figure 3-5.
Model 1600A Operating Procedure

SECTION IV

PRINCIPLES OF OPERATION

4-1. INTRODUCITON.

4-2. This section of the manual is divided into three major parts: (1) a functional description of the Model 1600A based on a simplified instrument algorithm and functional algorithms of the major section of the Model 1600A, (2) a functional block diagram description, and (3) a detailed circuit theory of operation.

4-3. The simplified algorithm presents the Model 1600A in its most basic form. The functional algorithms explain the operation of each section of the instrument. The functional block diagram description describes the purpose of each block on the block diagram in Section VIII (figure 8-8). Detailed block diagrams are included to help explain how each block functions. The detailed circuit description is limited to circuits that are unique or unusually complicated. No attempt is made to explain basic circuits.

4-4. BASIC INFORMATION.

4-5. The following paragraphs explain logic conventions that are used in describing the Model 1600A principles of operation.

4-6. LOGIC STATES. The terms HI and LO describe the output states of logic circuit elements. HI indicates the most positive dc level and LO indicates the most negative dc level produced by a given circuit element.

4-7. LOGIC CIRCUITRY. Most integrated circuits in the Model 1600A are in the TTL (transistor-transistor logic) and CMOS (complementary metal-oxide semiconductor) families of digital devices. A LO output from a TTL device is < +0.4 V and a HI output is ≥ +2.5 V. A LO output from a CMOS device in the Model 1600A is approximately 0 V, and a HI output is approximately +5.0 V.

4-8. MNEMONICS. A mnemonic is a letter designator (term) that describes the active state and function of a signal line. A prefix letter (H, L, P or N) indicates the active state of the signal and the remaining letters indiate its function. An H prefix indicates the function is active in the HI state, and an L prefix indicates the function is active in the LO state. For edge-controlled devices, the prefix P indicates the function is active on the positive-going transition, and the prefix N indicates the function is active on the negative-going transition.

4-9. Mnemonic functional definitions and points of origin are listed alphabetically in table 4-1.

4-10. FUNCTIONAL DESCRIPTION.

4-11. Figure 4-1 presents the functional sequence of events within the Model 1600A. The Model 1600A alternates between a data acquisition cycle and a display cycle.

4-12. During the data acquisition cycle, each word of input data is temporarily stored before being loaded into the memory. In the table display modes the input data (after temporary storage) is compared with the front-panel TRIGGER WORD

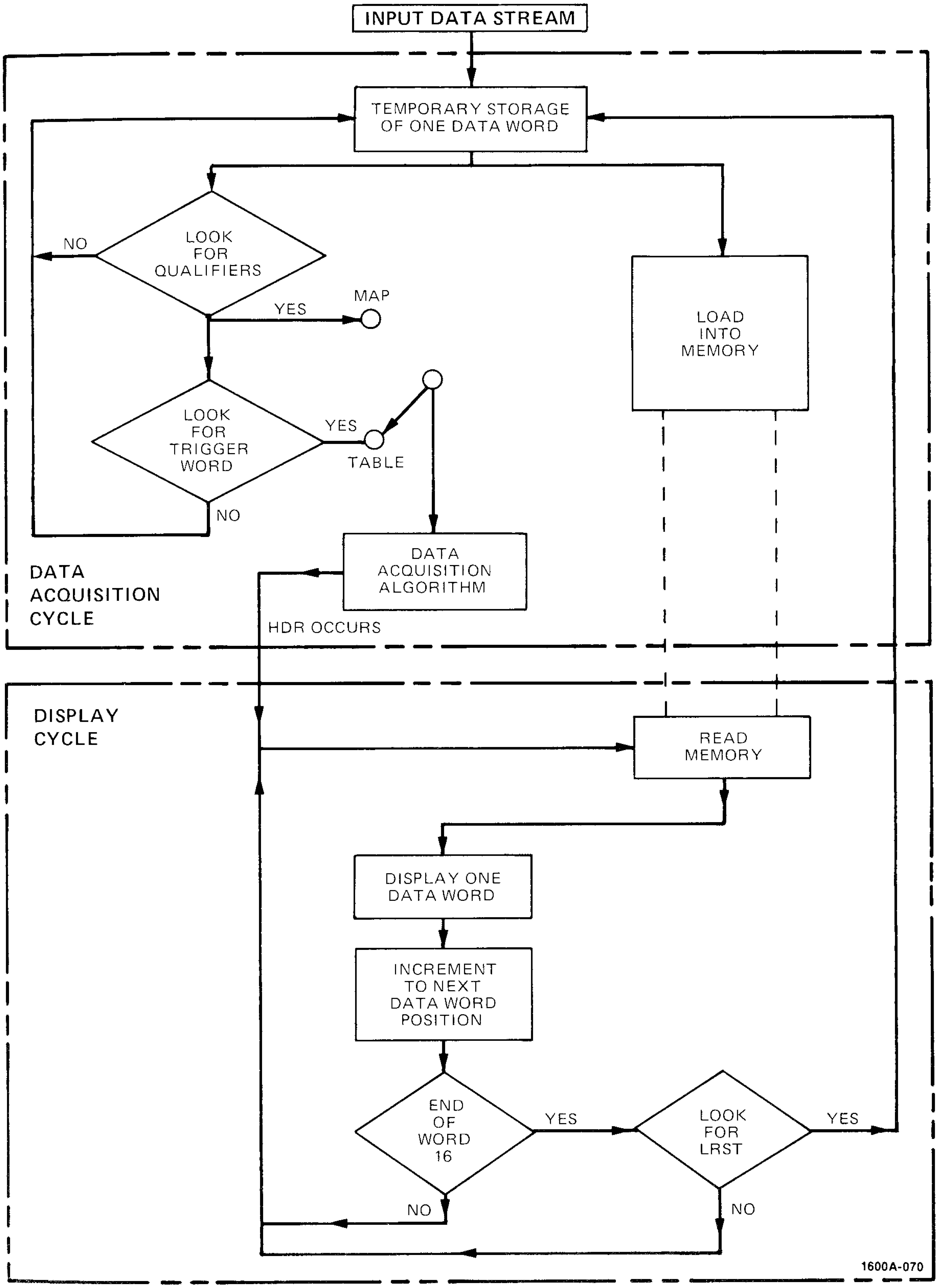


Figure 4-1. Functional Sequence of Events

switch position. When an input word matches the preset TRIGGER WORD, and trigger arming, bus, and qualifier conditions are met; the Model 1600A performs a data acquisition algorithm. In the map display modes, the Model 1600A performs the data acquisition algorithm whenever display qualifier conditions are met. Operation of the data acquisition algorithm is determined by the display and trigger modes selected. The algorithm controls memory loading and determines when gathered data is ready for display. When all algorithmic requirements have been satisfied, HDR occurs. The occurrence of HDR transfers the Model 1600A into a display cycle.

4-13. The display cycle begins with the occurrence of HDR. Information stored in the memory during the previous data acquisition cycle is read out and displayed one word at a time. At the end of each displayed word, the Model 1600A increments to the next data word position on the CRT. This process continues until the end of the sixteenth displayed word. At the end of the sixteenth word, the Model 1600A checks the SAMPLE MODE selected and the DISPLAY TIME control setting to determine if new data is required. When new data is not required, the display cycle repeats. When new data is required, LRST occurs. The occurrence of LRST transfers the Model 1600A into a data acquisition cycle. Pressing RESET will generate LRST regardless of where the machine is in the algorithm.

4-14. DIGITAL DELAY AND TRIGGER GENERATOR. The functional operation of the digital delay and trigger generator circuitry is shown in figure 4-2. The AND of trigger word recognition with qualifier recognition and LΔT produce HBTRG and HLTRG. HBTRG and HLTRG are applied to the bus and local flip-flops.

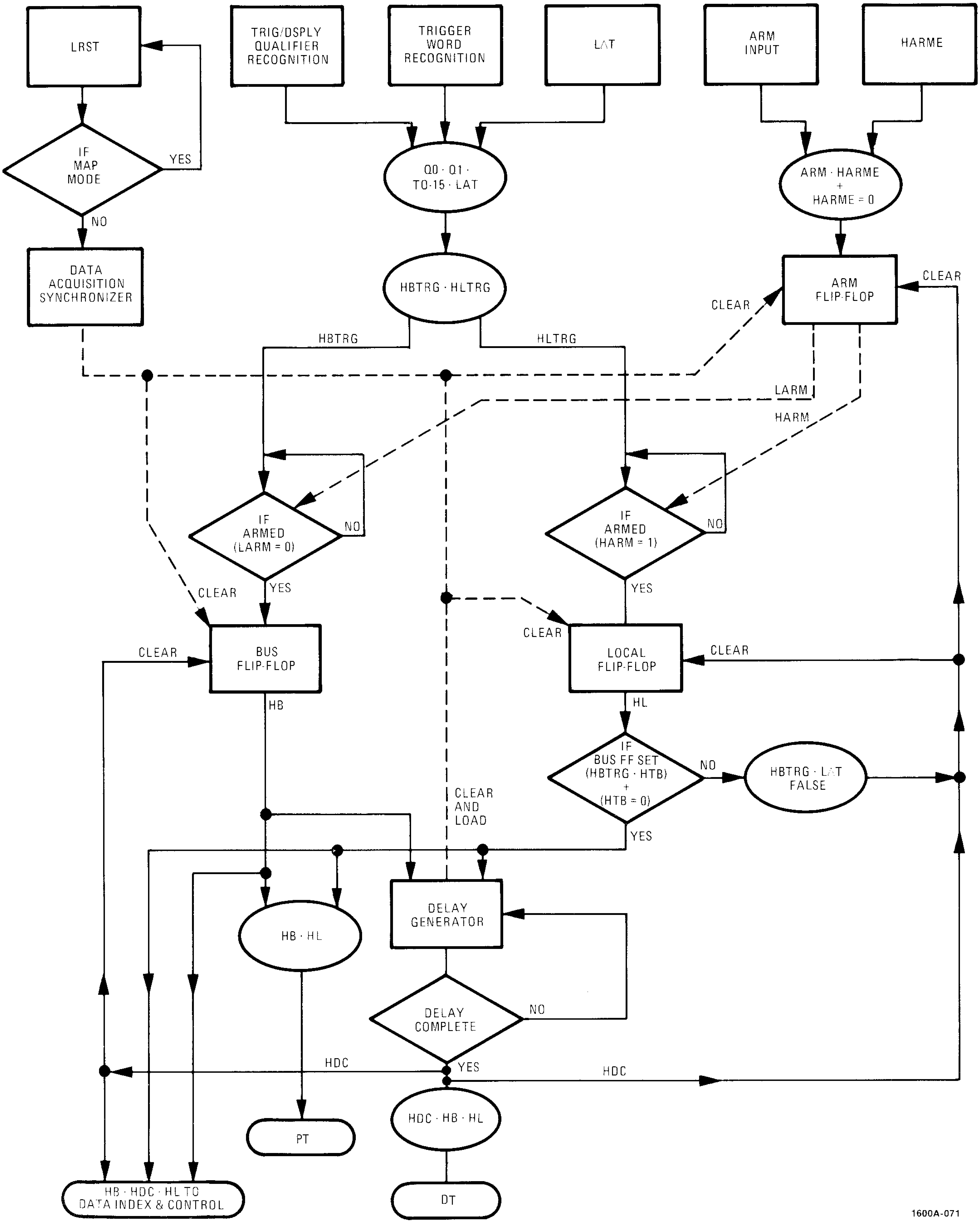


Figure 4-2. Digital Delay/Trigger Generator Algorithm

4-15. The bus and local flip-flops are enabled by LARM and HARM from the trigger arm flip-flop. When the ARM trigger mode is selected, an external arming signal is required to clock LARM and HARM are held in the true state. With LARM and HARM true, the occurrence of HBTRG and HLTRG force the $\overline{Q}$ outputs of the bus and local flip-flops HI, generating HB and HL. HB and HL enable the delay generator, and their AND generates the pattern trigger output (PT). If HB is false (the bus flip-flop has not been set) the local and arm flip-flops are cleared and the Model 1600A waits for the next trigger word.

4-16. Once enabled, the delay generator counts out the delay set on the DELAY thumbwheels. When the delay is complete, HDC occurs. The AND of HDC with HB and HL generate the delayed trigger output (DT). In addition HDC is used to clear the local, arm and bus flip-flops on the occurrence of LRST.

4-17. In map display modes, resets to the digital delay and trigger generator circuits are inhibited.

4-18. DATA INDEX AND CONTROL. Figure 4-3 shows the functional operation of the data index and control circuit. The data index and control circuit controls the read and write functions of the memory and determines when a data acquisition cycle is complete.

4-19. When the start display mode is selected, the occurrence of the trigger word and the subsequent completion of the dalay (HB · HL · HDC) set the start flip-flop. The outputs of the start flip-flop are LTRG and HTRG*. LRTG is inverted (HTRG) and used as a control signal for the blanking circuit. HTRG* enables the data index counter. Once enabled, the data index counter counts the number of words written into memory. When the count reaches terminal count

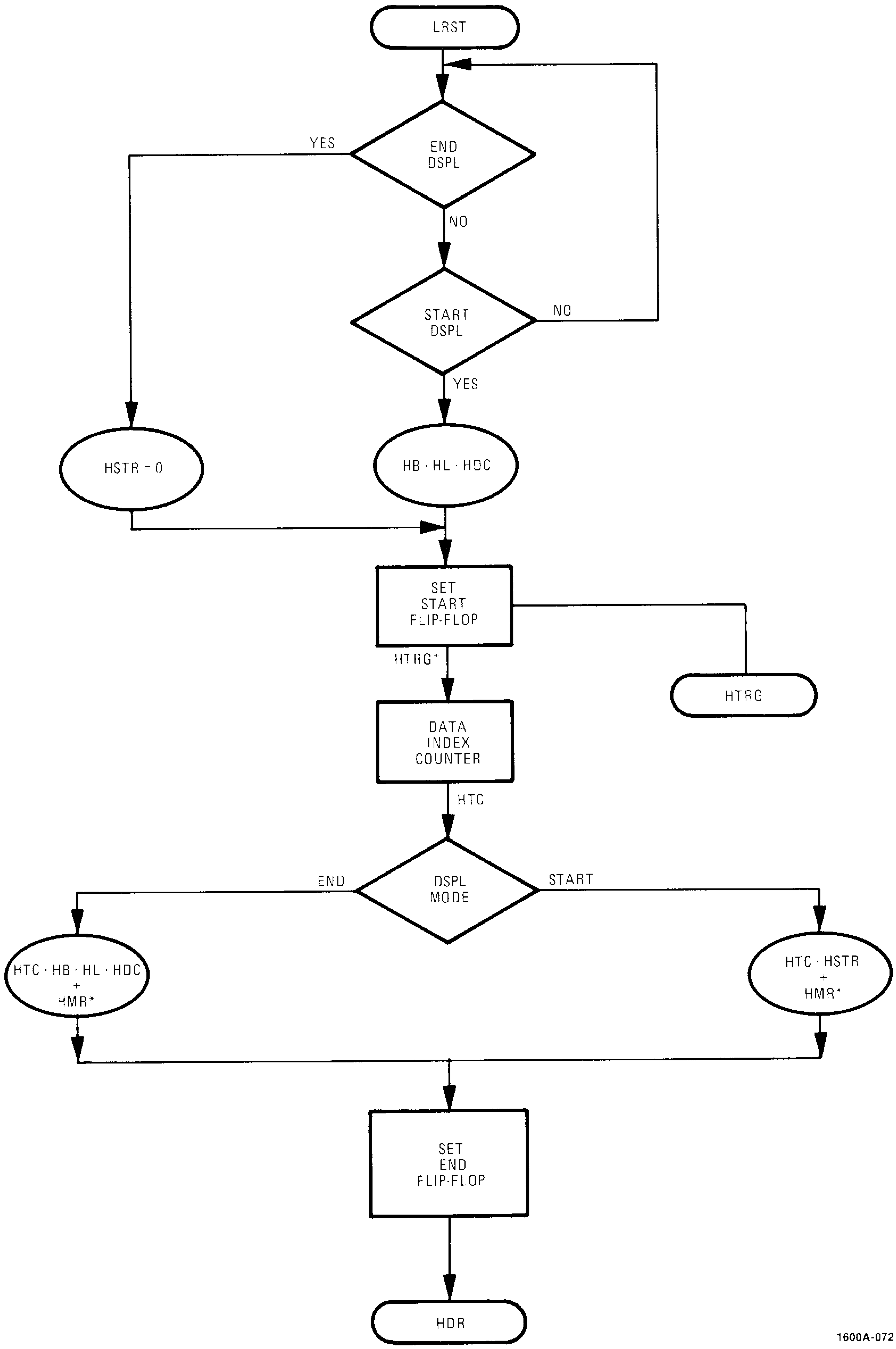


Figure 4-3. Data Index and Control Algorithm

(16 words have been written into memory), HTC goes HI setting the end flip-flop. Setting the end flip-flop generates HDR, initiating a display cycle.

4-20. When the end display mode is selected, HSTR is LO, which sets the start flip-flop. The data index counter is enabled. When terminal count is reached, HTC goes HI and remains in that state. Since the trigger word has not been detected, data words continue to refresh the memory with the current input data word being written into the bottom of memory and the oldest word being bumped out the top. When the trigger word is detected and the delay generator counts out, HB · HDC · HTC sets the end flip-flop initiating a display cycle.

4-21. DISPLAY CYCLE. The Model 1600A provides two types of functional displays. The table display modes provide a display of one's and zero's in tabular format. The map display modes display 16-bit data words each as a single dot whose location on the CRT uniquely identifies it. Figure 4-4 shows the functional operation of the display cycle in table display modes and figure 4-5 shows the functional operation of the display cycle in the map display modes.

4-22. Table Display Algorithm. The table display algorithm is initiated by HDSPR. When HDSPR goes LO, the horizontal and vertical state counters are enabled. The vertical state counter addresses a particular 16-bit word in memory, while the horizontal state counter selectes one of the 16 bits at a time to be written on the CRT. Once a complete word is displayed on the CRT, (horizontal state count = 16), the vertical state counter is incremented and the next word in memory is displayed.

4-23. At the end of word sixteen, the instrument checks HA. HA determines

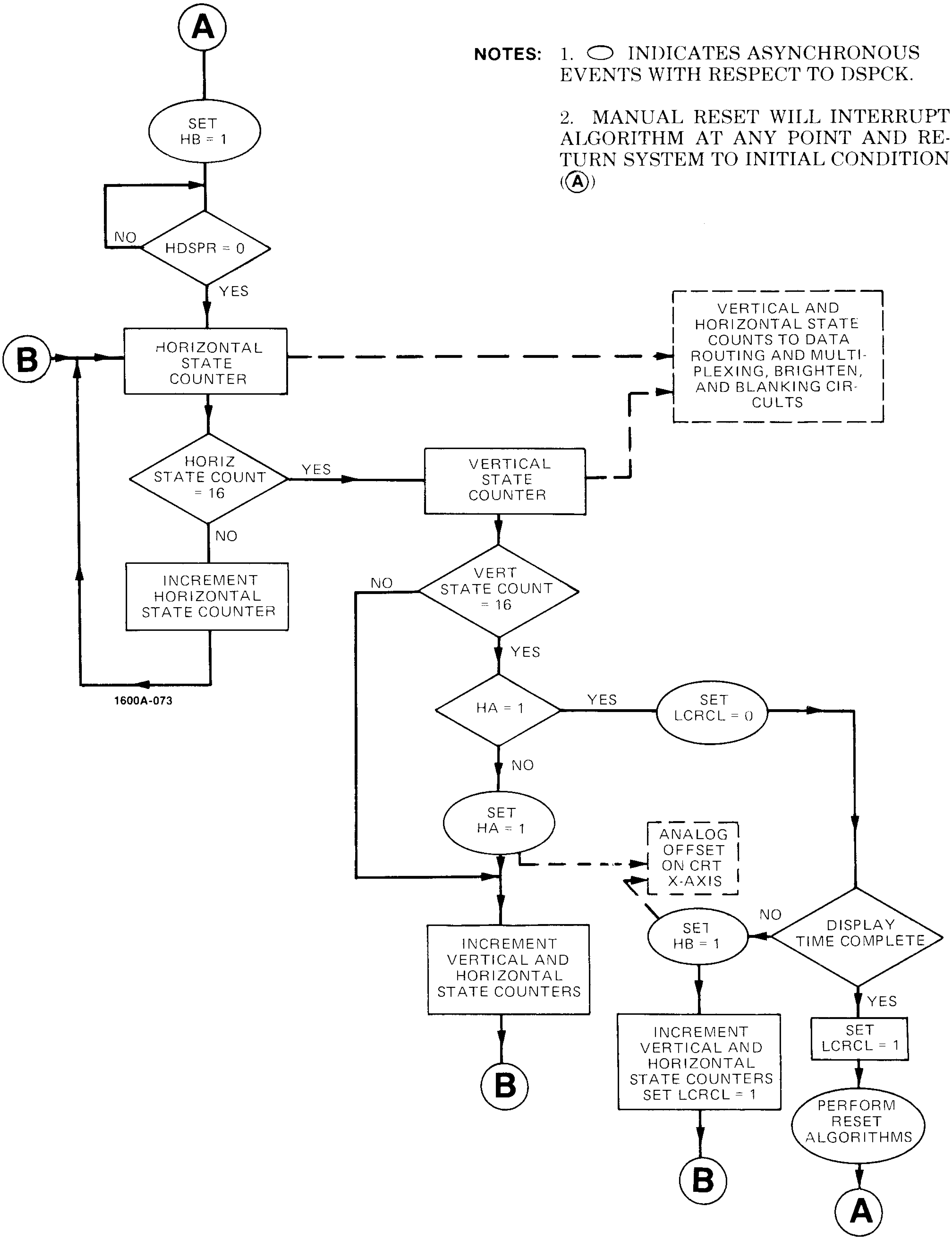


Figure 4-4. Table Display Algorithm

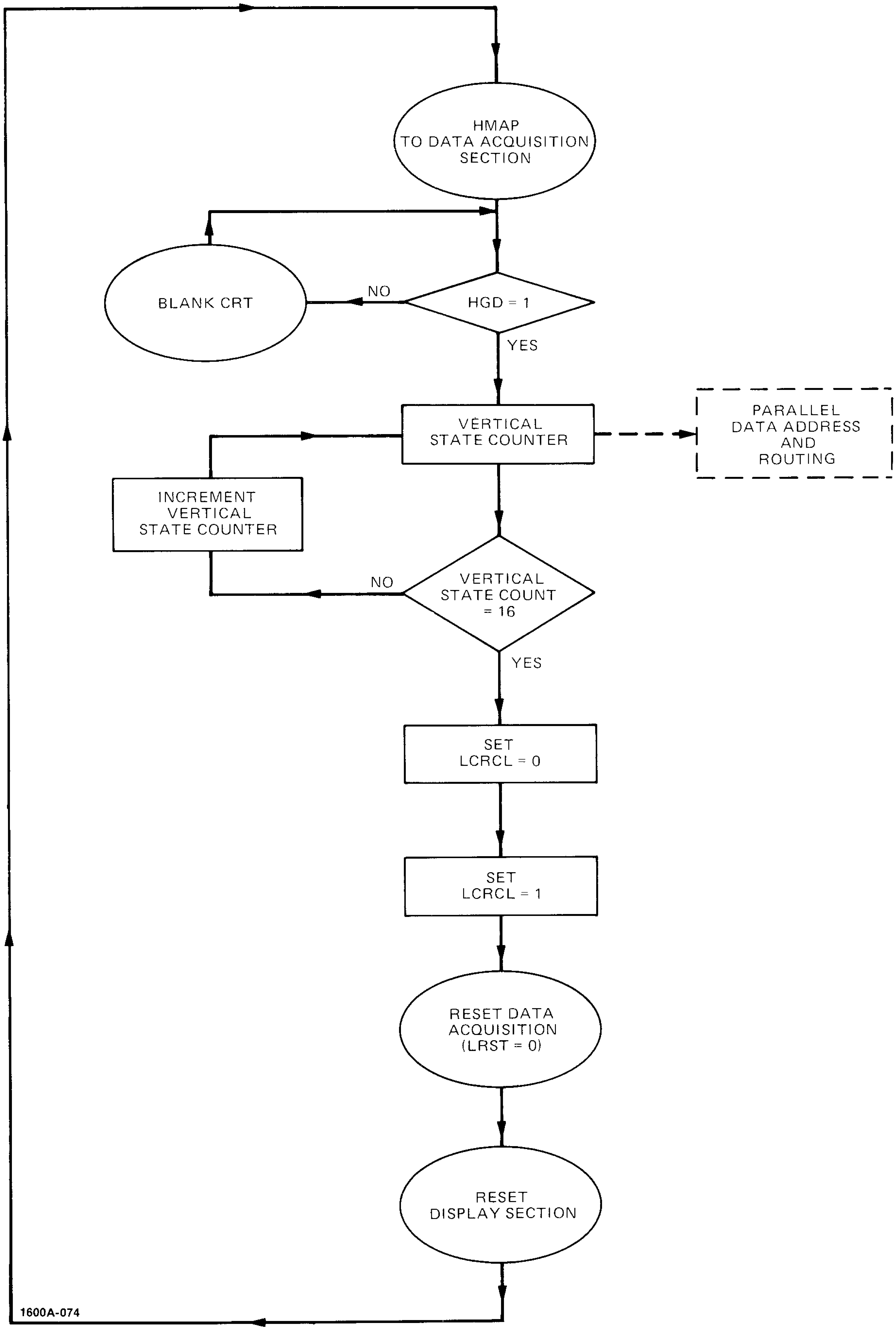


Figure 4-5. Map Display Algorithm

whether A-memory or B-memory data is displayed. B-memory data is written on the right half of CRT screen (HA = 0). The instrument then sets HA = 1 and writes A-memory data on the left half of the CRT screen.

4-24. After both 16-word tables have been displayed, LCRCL is set to zero. If the repetitive sample mode is selected, LCRCL interogates the repetitive reset circuit. If display time is complete; LRST is set to 0 and HDSPR is set to 1, initiating a data acquisition cycle. If display time is not complete; the instrument sets HB = 1, increments the vertical state counter, and repeats the display algorithm. If the instrument is in the single sample mode, the display algorithm is repeated until the instrument is manually reset.

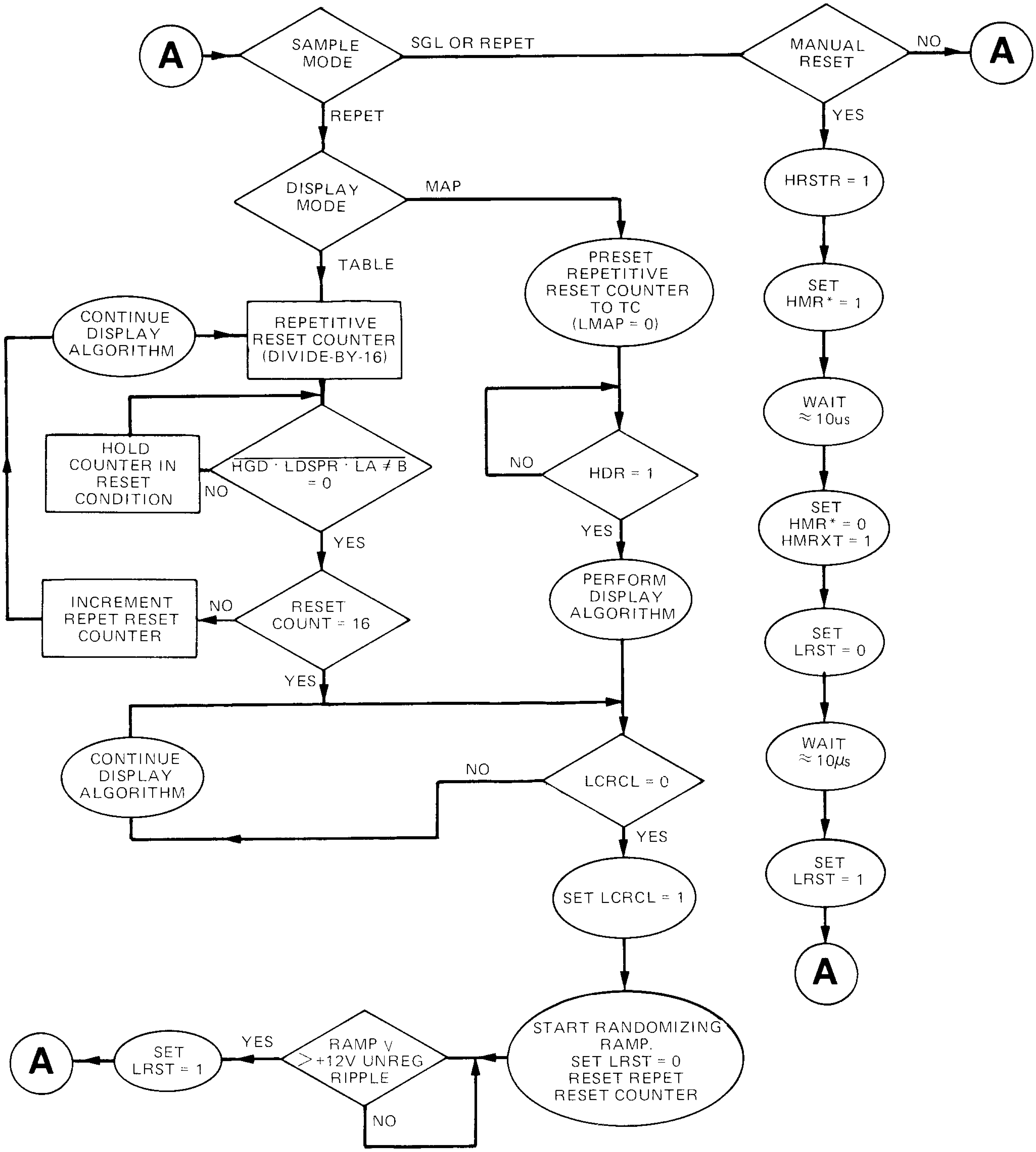
4-25. Map Display Algorithm. The map display algorithm is initiated by HGD. HGD = 1 indicates that sixteen words of valid data are stored in A-memory. When HGD is set to one, the vertical state counter is enabled. The vertical state counter addresses A-memory, reading out the sixteen bits of each data word in parallel. The 16 data bits are routed to D/A converters whose outputs drive the X and Y axes of the CRT. The eight most-significant data bits determine the vertical deflection and the eight least-significant bits determine the horizontal deflection of the CRT beam.

4-26. When all sixteen words in memory have been displayed (vertical state count = 16), LCRCL is set to zero. LCRCL · HMAP writes the cursor on the CRT screen. LCRCL then initiates a data acquisition cycle and resets the display section (HDSPR = 1).

4-27. RESET ALGORITHMS. At the end of a display cycle, the Model 1600A performs two reset algorithms. The data-acquisition reset algorithm resets the data acquisition section of the Model 1600A at the start of a data acquisition cycle. The display reset algorithm resets the display section at the end of a display cycle.

4-28. Data Acquisition Reset (see figure 4-6). The operation of the data acquisition reset algorithm is determined by the sample and display modes selected. When either REPET or HALT A ≠ B sample mode is selected, the Model 1600A performs a repetitive reset. In table display modes, the occurrence of LRST is controlled by DISPLAY TIME. DISPLAY TIME determines the frequency of the repetitive-reset clock generator. When not reset by $\overline{\mathrm{HGD \cdot LDSPR \cdot LA{\neq}B}}$, the repetitive-reset counter counts the outputs of the clock generator. When the counter reaches terminal count (reset count = 16), the circuit waits for LCRCL to occur. LCRCL sets LRST = 0 and starts a voltage ramp that is compared with a threshold set by the +12-volt unregulated ripple. When the voltage ramp exceeds the threshold, LRST is set to 1. The comparison of the voltage ramp with the +12-volt unregulated ripple provides a randomly varying start time for the data acquisition cycle to prevent the reset rate from locking to a subharmonic of the clock from the system under test. This ensures that a different block of 16 words will be captured in each data acquisition cycle for display in the map modes.

4-29. If a map display mode is selected, the reset counter is preset to the terminal count state disabling control of repetitive reset by DISPLAY TIME. At the occurrence of HDR, the 16 data words stored in A-memory are displayed and then LCRCL is generated. LCRCL starts the randomizing voltage ramp and sets LRST to 0. When the ramp crosses threshold, the Model 1600A sets LRST to one.



NOTES:

1. IN THE SINGLE SAMPLE MODE, REPETITIVE RESETS ARE IGNORED BY THE MODEL 1600A BUT ARE ROUTED TO THE I/O PORT TO RESET THE MODEL 1607A IN I/O BUS OPERATION.
2. MANUAL RESETS WILL INTERRUPT MODEL 1600A AT ANY POINT IN ITS OPERATION AND RETURN THE INSTRUMENT TO THE START OF A DATA ACQUISITION CYCLE.
3. ⬭ INDICATES ASYNCHRONOUS EVENTS WITH RESPECT TO REPETITIVE RESET CLOCK GENERATOR.

1600A-075

Figure 4-6. Data Acquisition Reset Algorithm

4-30. Reset is controlled by the reset pushbutton on the front panel in the single sample mode. Pressing RESET will also cause a reset to occur in a repetitive sample mode. When RESET is pressed, HRSTR goes HI. HRSTR generates HMR* which sets up the data acquisiton section for LRST. After approximately 10 μs, HMR* goes LO. The trailing edge of HMR* generates HMRXT and LRST. HMRXT is routed to the I/O PORT where it can be used to reset a Model 1607A in I/O bus operation. LRST initializes another data acquisition cycle.

4-31. Display Reset (see figure 4-7). The oepration of the display reset algorithm is determined by the display mode selected. HSA is HI when table A or a map is displayed. HSA enables the Model 1600A to reset the display section internally. With table A or map display selected, LRST from the data acquisition reset circuit generates the display reset (LDSPR = 0). In the map display modes, LGD can also cause a display reset. Whenever there is invalid data in A-memory; LGD goes HI, generating LDSPR. This condition can occur at low clock rates where the Model 1600A is in the partial display mode.

4-32. HSB is HI when table B display is selected. HSB enables an external reset signal (LXDPR) to generate LDSPR whenever a Model 1607A is connected to the Model 1600A I/O bus (LXPG1 = 0). When both table A and table B are displayed, both HSA and HSB are HI.

4-33. BLOCK DIAGRAM.

4-34. Figure 8-8 is the Model 1600A block diagram. Heavy lines enclose circuitry contained on a specific schematic. The Model 1600A contains two major sections, a data acquisition section and a display section. The data

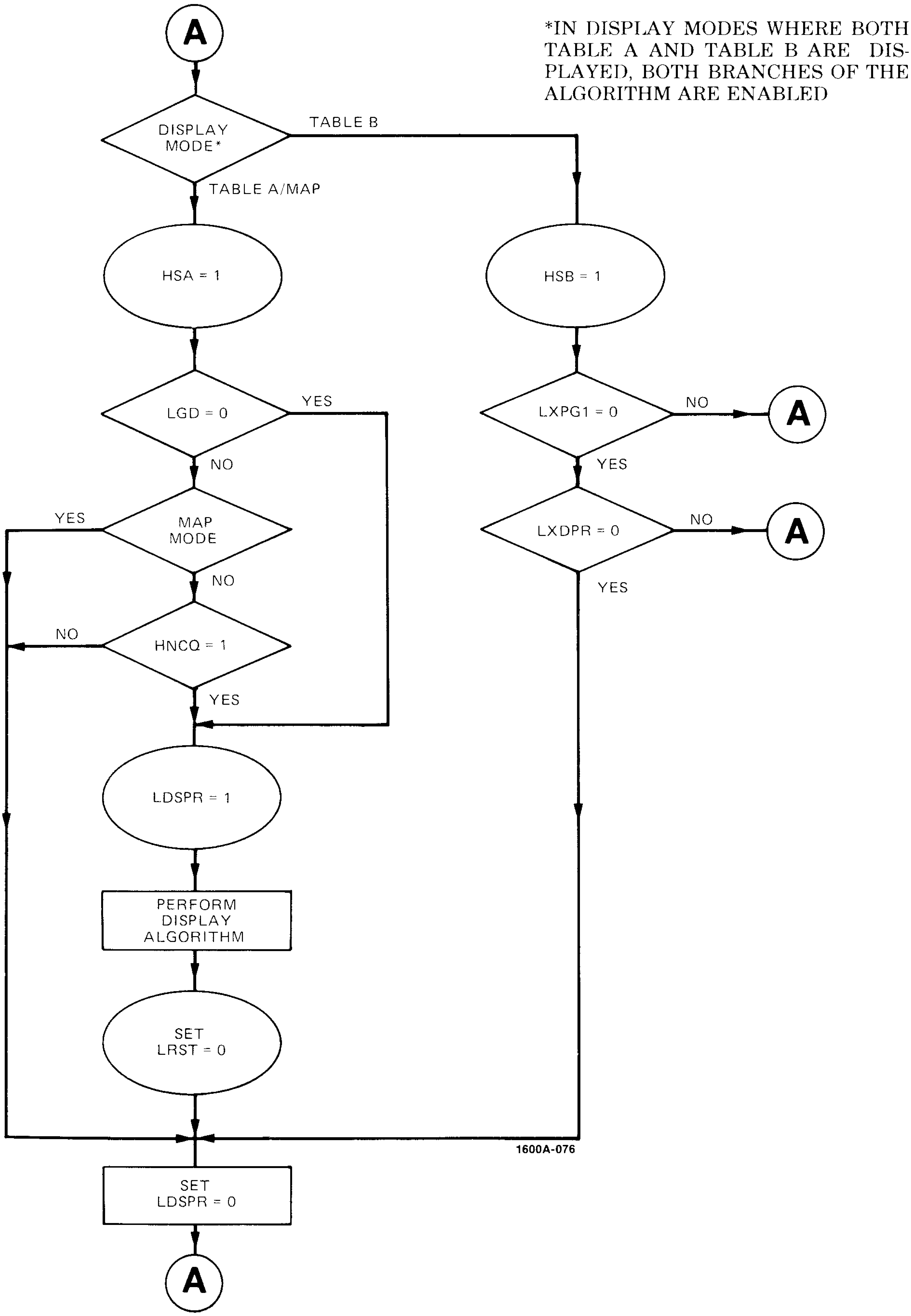


Figure 4-7. Display Reset Algorithm

acquisition section consists of the circuitry shown on schematics 3 through 10. The display section consists of the circuitry shown on schematics 11 through 15.

4-35. DATA ACQUISITION SECTION.

4-36. Data Input (see figure 4-8). Inputs to the Model 1600A are supplied by a clock probe and three data probes. The input threshold level for the clock and data probes is provided by the instrument threshold supply. With TTL selected, the threshold level is fixed at +1.5 V. With VAR selected, the threshold level is variable from -10 V to +10 V by VAR SET. Clock Select supplies two clock slope commands (SS and SI) to the clock probe. These commands, controlled by the clock pushbutton, determine which transition of the input clock signal transfers input data into the Model 1600A.

4-37. The clock probe supplies two buffered inputs, PCLK and NCLK. The leading-edge transitions of PCLK and NCLK are synchronous with data inputs from the data probes. When CLOCK is out (_|‾), the leading-edge transition of PCLK is a positive-going transistion, and the leading-edge transition of NCLK is a negative-going transition. With these conditions, data is clocked into the Model 1600A on the positive-going transition of the input clock signal. When CLOCK is in (‾|_), the leading-edge transition of PCLK is a negative-going transition, and the leading-edge transition of NCLK is a positive-going transition. With CLOCK in, data is clocked on the negative-going transition of the input clock signal.

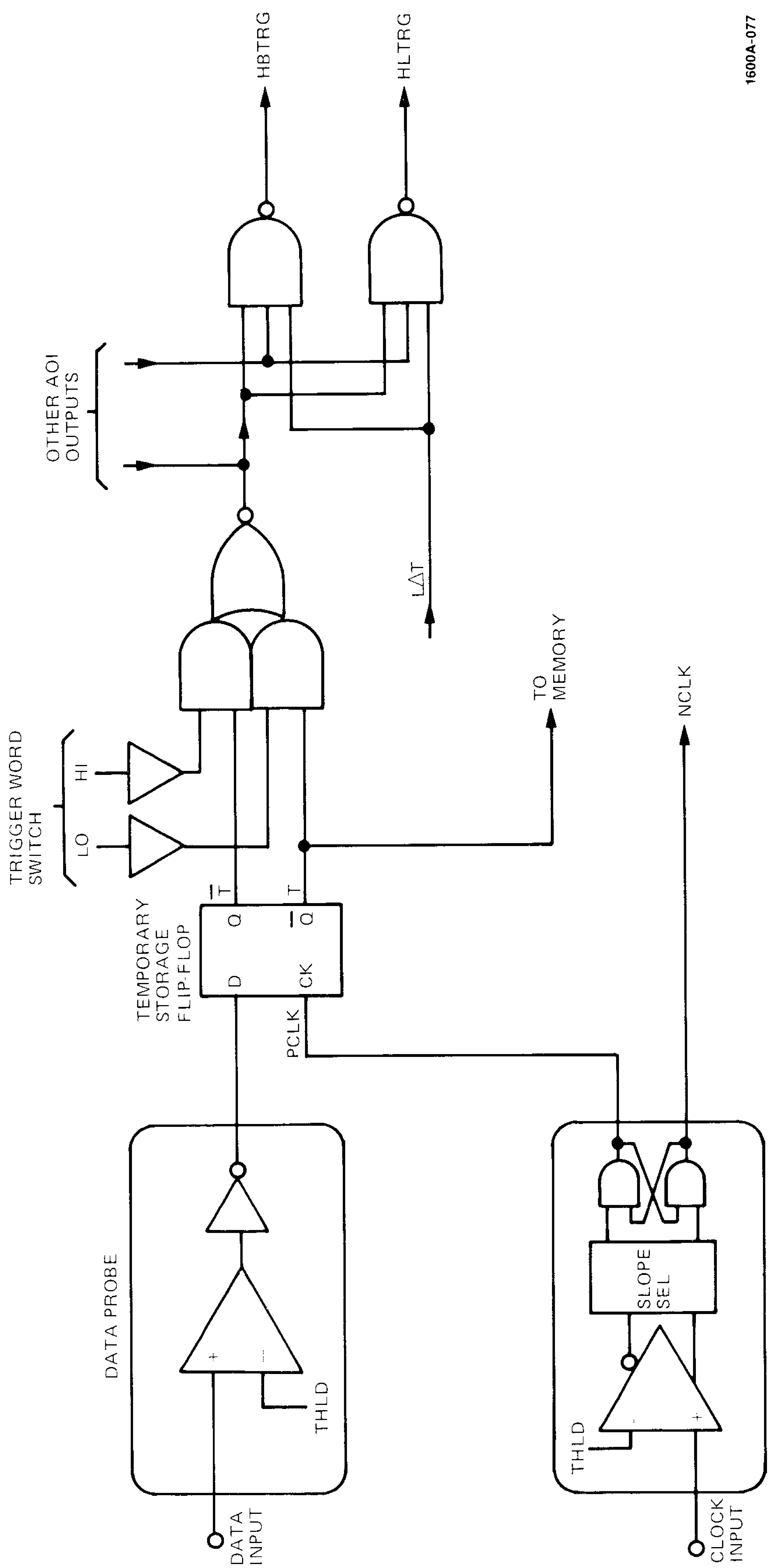


Figure 4-8. Data Input, Temporary Storage, and Pattern Recognition

4-38. PCLK transfers input data into temporary storage and is used by the Timing Generator to derive the internal data acquisition clocking signals. NCLK clock the NO CLOCK indicator control logic.

4-39. Temporary Data Storage. Input data from the data probes is applied to a series of D flip-flops for temporary storage. The temporary storage flip-flop outputs are the data word and its complement (T0 through T15 and $\overline{T0}$ through $\overline{T15}$) and the two qualifier bits and their complements (TQ0/TQ1 and $\overline{TQ0}/\overline{TQ1}$). The rising edge of PCLK loads new data into the temporary storage flip-flops. The outputs of the temporary storage flip-flops are connected to the pattern recognition gates and A-memory.

4-40. Pattern Recognition. The pattern recognition gates compare the TRIGGER WORD and QUALIFIER switch setting with the input data and qualifier lines. When a match occurs, HBTRG and HLTRG (enabled by LΔT) are produced. HBTRG is wire ANDED with the trigger bus. All inputs to the bus must be high before HBTRG will rise above threshold. When DSPLY qualifier mode is selected, the pattern recognition circuit generates HCLQ which is used to qualify timing signals in the Model 1600A.

4-41. Digital Delay and Trigger Generator (see figure 4-9). Once pattern recognition occurs, HLTRG is clocked into the local flip-flop. If the BUS trigger mode is selected, the rising edge of HBTRG sets the bus flip-flop. When both flip-flops are set, HB and HL generate the pattern trigger (PT) and enable the delay generator. If the delay generator is set to zero, PT and DT (delayed trigger) are generated when the local and bus flip-flops are set. For delays other than zero, PT goes HI when the bus and local flip-flops are set and remains HI while the delay generator is running. When the delay has timed out, HDC occurs. DT is generated by HDC and PT is terminated. The delay generator and local flip-flop clock is qualified so that a trigger is recognized only when qualifier conditions are met.

4-42. When trigger arming is selected, the arm flip-flop disables the local and bus flip-flops until an arming pulse is received. Once an arming pulse is received, the local and bus flip-flops are enabled. When trigger and qualifier conditions are met, PT is generated, and the arm flip-flop is reset.

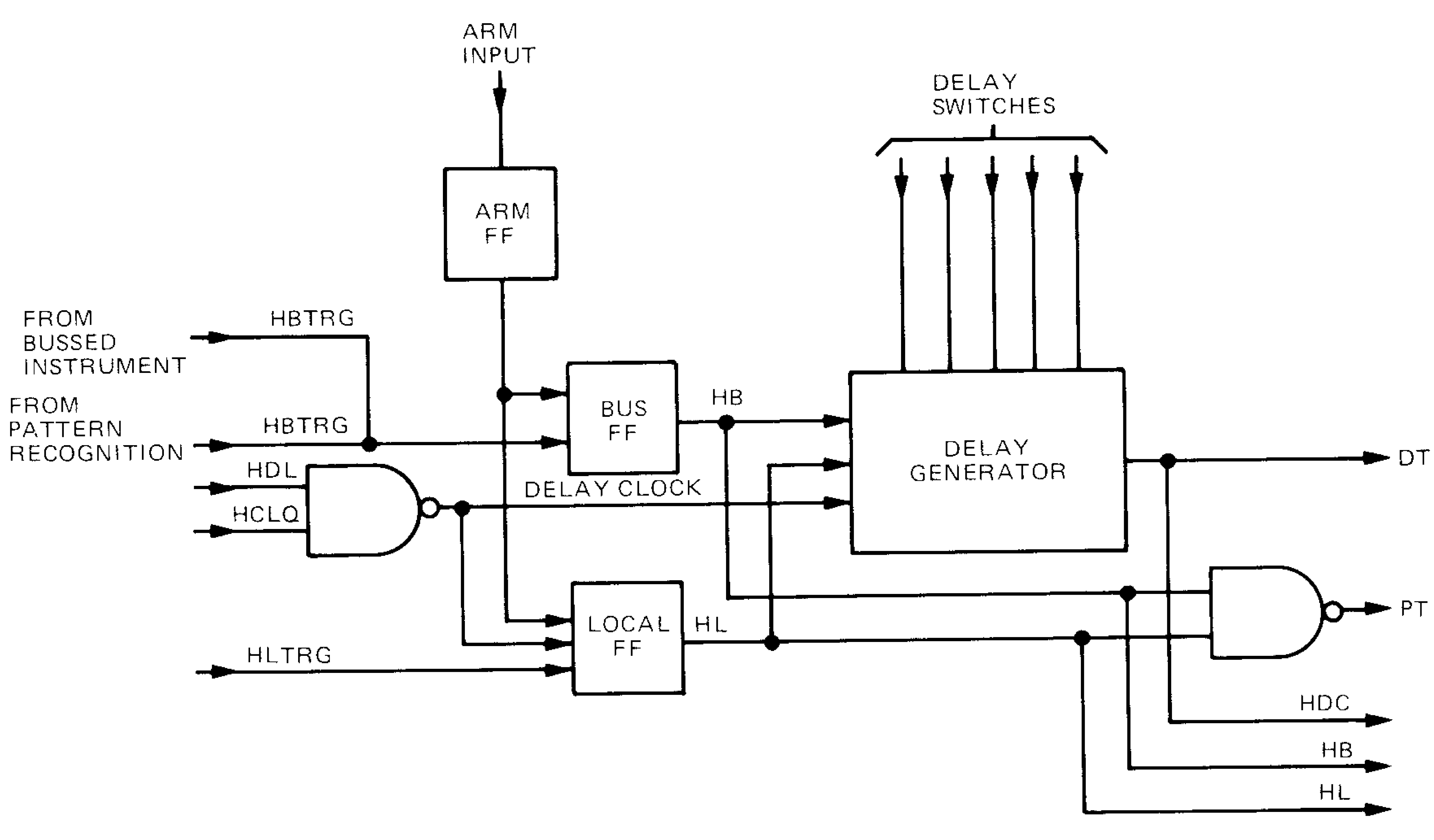


Figure 4-9. Digital Delay/Trigger Generator Block Diagram

4-43. A-memory and Data Index and Control (see figure 4-10). When the display section generates LRST, a data acquisition cycle is initiated.

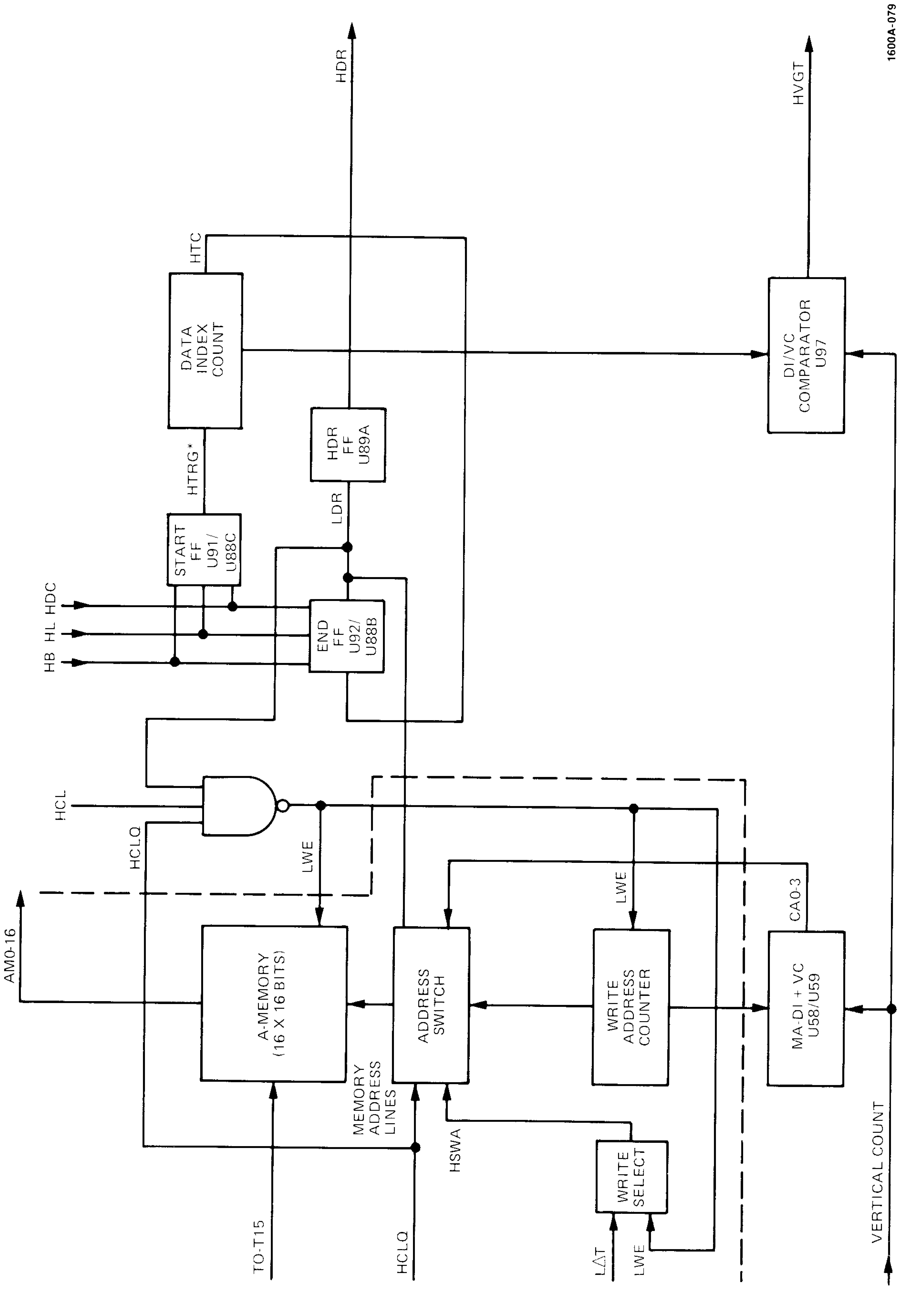


Figure 4.10. A-memory and Data Index/Control Block Diagram

The data index counters, and the start and end flip-flops are reset. When a qualified clock is detected, the memory address lines are switched to the write address counter and a memory write enable pulse (LWE) is generated. While LWE is true, one word is written in memory. At the trailing edge of LWE, the write address counter is incremented and the memory address lines are switched back to the display or computed address (CA0-3).

4-44. With the start display mode selected, the data index counter is incremented by LWE2 only after the start flip-flop is set. The start flip-flop is set when a trigger word is detected and the digital delay is complete. When the data index counter reaches terminal count, the end flip-flop generates HDR. HDR indicates that memory data is complete and initiates a display cycle.

4-45. With the end display mode selected, the start flip-flop is preset enabling the data index counter to run prior to trigger word recognition. When the data index counter reaches terminal count, the end flip-flop is enabled to receive a trigger. The occurrence of a trigger after terminal count is reached generates LDR, which initiates a display cycle.

4-46. The data index counter keeps track of the number of valid wrods written into memory. The write address counter points to the next address in memory to be written into. The difference of the output of the two counters is taken in U58 to determine where the first word in memory is located. This computed first word address is added to the vertical state count from the display section to determine the address of the words to be read from memory during a display cycle.

4-47. Whenever the qualified clock rate drops below approximately 30 Hz during a data acquistion cycle, the partial display mode is enabled. The vertical state counter reads partial memory data through U58/U59 and U97. When the vertical state count exceeds the data index count, i.e., addresses invalid data, comparator U97 provides HVGT to the display section. HVGT blanks the CRT so that only valid data is displayed.

4-48. Timing Generator. The timing generator develops four internal clocking signals used in the instrument based on the clock from the system under test. HCL is gated in the memory index control circuit to derive the write enable pulse (LWE). HDL is the clock for the delay generator. LΔT clocks the pattern recognition circuit and HΔT is used to clock the reset circuit for the local flip-flop in the trigger generator.

4-49. Indicator Light Control. The indicator light control logic provides a hierarchy that determines the sequence the indicator lights are enabled. When the NO CLOCK light is on, the NO QUAL and NO TRIG lights are disabled. When a clock is present and the NO QUAL light is on, NO TRIG is disabled. The NO ARM light also disables the NO TRIG light. Otherwise, the NO ARM light functions independently of the other lights.

4-50. The indicator light logic also provides HNCQ to the display section. When the qualified clock rate is less than approximately 30 Hz, HNCQ places the display section in the partial display mode.

4-51. DISPLAY SECTION.

THE DESCRIPTION OF THE DISPLAY SECTION IS NOT AVAILABLE AT THIS TIME. IT WILL BE FURNISHED IN THE FINAL OPERATING AND SERVICE MANUAL.

Table 4-1. Model 1600A Mnemonics

TERM	FUNCTION	ORIGIN
A	Switching signal for Table A CRT offset. When A is LO, data is displayed on left-half of CRT screen.	Schematic 16, A8U37F, PIN 12
ADATA	Complement of $\overline{\text{DATA}}$. A-memory data to be stored in B-memory when STORE A → B is pressed. ADATA is displayed on the left-half of the CRT screen.	Schematic 15, A8U46F, PIN 12
AMO-AM15	Memory output data. Data stored im memory for display.	Schematic 10, A1U28, A1U30, A1U32, A1U33, PINS 5, 7, 9 and 11
ARM	Arming input signal from TRIG ARM IN connector.	Schematic 8, TRIG ARM IN Connector J3
B	Switching signal for Table B CRT Offset. When B is LO, data is displayed on left-half of CRT screen.	Schematic 16, A8U37E, PIN 10
BDATA	Serialized data output from B-memory.	Schematic 16, A8U47, PIN 13
CAO-CA3	Computed Address. Memory address used to read memory during display cycle. Computed address = vertical state count + (Write Address Count - Data Index Count).	Schematic 11, A1U59, PINS 2, 6, 9 and 15
$\overline{\text{DATA}}$	Serialized data output from memory used to derive LZER and XDSPD.	Schematic 12, A1U39 PIN 10
DT	Delayed Trigger. Trigger generator output signal applied to DELAYED TRIG OUT connector.	Schematic 4, A1U62B, PIN 8
DO-D15	Input data bits 0 through 15 from Data Probes.	Schematic 5, A1J2, PINS 13 - 16; A1J3, PINS 11 - 16; A1J4, PINS 11 - 16

Table 4-1. Model 1600A Mnemonics (Cont'd)

TERM	FUNCTION	ORIGIN
DSPCK	Display Clock. Clocking signal for display section. DSPCK is 50-kHz clock in table display modes, 25-kHz clock in map display modes.	Schematic 19, A8U4C, PIN 8
$\overline{\text{DSPCK}}$	Complement of DSPCK.	Schematic 19, A8U4D, PIN 11
EDTBS	External Data To Be Stored. Serial data from an external device on the I/O bus to be stored in B-memory.	Schematic 22, J6, PIN 23
HA	HI, A. Display control signal indicating table A is currently being displayed.	Schematic 16, A8U30A, PIN 5
HARM	HI, Armed. Complement of LARM	Schematic 8, A1U71A, PIN 7
HARME	Hi, Arm Enable. Data acquisition control signal (dc level). HARME = HI when NORM/ARM is set to ARM position (in). When HI, the Model 1600A must be armed before it will recognize a trigger.	Schematic 20, NORM/ARM Switch A7S1D
HB	HI, B. Display control signal indicating table B is currently being displayed.	Schematic 16, A8U30A, PIN 6
HB	HI, Bus. Data acquisition control signal. HB = HI when bus flip-flop is set.	Schematic 8, A1U67A, PIN 7
HBCD	HI, BCD. Display control signal (dc level) for Horizontal Code Converter, U26. When HI, displayed word format is four four-bit bytes. When LO, displayed word format is five three-bit bytes with MSB left over.	Schematic 4, BYTE 4 BIT/3 switch A5S1F
HBCDX	HI, BCD External. Table B format control signal from Model 1607A in I/O Bus operation. When HI, table B word format is four 4-bit bytes. When LO, word format is five 3-bit bytes with MSB left over.	Schematic 22, J6, PIN 22

Table 4-1. Model 1600A Mnemonics (Cont'd)

TERM	FUNCTION	ORIGIN
HBR	HI, Brighten. Z-axis modulation control signal to Model 1600A HBR = HI indicates current displayed character should be intensified.	Schematic 15, A8U37B, PIN 4
HBRXT	HI, Brighten External. Z-axis modulation control signal from Model 1607A. HBRXT = HI indicates current displayed character in table B should be intensified.	Schematic 22, J6, PIN 19
HBTRG	HI, Bus Trigger. Trigger signal (HI state) indicating both Model 1607A and Model 1600A Trigger words have occurred simultaneously in the trigger bus mode.	Schematic 7, A1U25B, PIN 8
HCBLK	HI, Column Blank. Blanking control signal. When HI, Data column currently being addressed is blanked.	Schematic 17, A8U26A, PIN 1
HCL	HI, Clock. Clocking signal from timing generator used to clock data index and control. HCL is derived from PCLK.	Schematic 9, A1U43B, PIN 7
HCLQ	HI, Clock Qualifier. DSPLY qualification signal. HCLQ is HI when DSPLY qualifier requirements are met.	Schematic 7, A1U26, PIN 8
HCQD	HI, Correct Quadrant. Blanking control signal in EXP map mode. HCQD unblanks CRT when input data word lies in map sector selected in EXP. HCQD = HEMAP · LXPMP	Schematic 17, A8U22C, PIN 8
HCRCL	HI, Circle. Mode control signal HCRCL goes HI for one display clock each time display has been completed. In map, HCRCL causes the cursor to be displayed. In table, the cursor is blanked.	Schematic 16, A8U20B, PIN 8
HDC	HI, Delay Complete. Data acquisition control signal. HDC = HI when delay generator has counted out the delay set on DELAY thumbwheels.	Schematic 8, A1U84B, PIN 9

Table 4-1. Model 1600A Mnemonics (Cont'd)

TERM	FUNCTION	ORIGIN
HDL	HI, Delay Clock. Clocking signal from timing generator used to clock delay generator. HDL is derived from PCLK.	Schematic 9, A1U43A, PIN 6
HDR	HI, Data Ready. Hi state occurs at the end of a data acquisition cycle indicating 16 valid data words have been acquired.	Schematic 11, A1U89A, PIN 5
HDR*	HI, Data Ready*. Memory Address control signal indicating trigger word has been found and A-memory is loaded with valid data. When HI, HDR* enables reading of memory by display section.	Schematic 11, A1U88B, PIN 8
HDSPR	HI, Display Reset. Reset signal for display functions.	Schematic 19, A8U48B, PIN 4
HΔT	HI, Delta T. Clocking signal for local flip-flop reset gate. HΔT is derived from PCLK.	Schematic 9, A1U42A, PIN 6
HE	HI, Equal. Control signal for word intensify circuit. HI when trigger word is being addressed by display section.	Schematic 14, A1U86, PIN 14
HEMAP	HI, Equal Map. Blanking control signal in EXP map mode. HEMAP is HI when bits 15, 14, 7, and 6 of the input data word matches the setting on TRIGGER WORD switches.	Schematic 12, A1Q8
HGD	HI, Good Data. Complement of LGD. Control signal for blanking circuitry. HGD = HDR$\cdot\overline{\text{HR1}}$	Schematic 19, A8U9E, PIN 10
HGDX	HI, Good Data External. Control signal from Model 1607A, HGDX holds off Model 1600A repetitive reset until table B is displayed.	Schematic 22, J6, PIN 15
HLTRG	HI, Local Trigger. Trigger signal (HI state) indicating Model 1600A has met local triggering requirements.	Schematic 7, A1U25C, PIN 12

Table 4-1. Model 1600A Mnemonics (Cont'd)

TERM	FUNCTION	ORIGIN
HM1-5	Horizontal Multiplexer 1-5. Output from ROM that sets decading of horizontal state counter which locates bits on screen for 4-bit/3-bit spacing.	Schematic 20, A7U14, PINs 9 - 12 A7U17D, PIN 11
HMAP	HI, Map. Complement of LMAP control signal for Delay generator, data index and control, reset circuitry, and display multiplexors. HMAP = HI when map display mode is selected.	Schematic 15, A8U13D, PIN 13
HMR*	HI, Manual Reset*. Manual reset signal for data index and control circuit.	Schematic 18, A8U16B, PIN 10
HMRXT	HI, Manual Reset External. External manual reset pulse to Model 1607A.	Schematic 18, A8U16A, PIN 6
HNCQ	HI, No Clock or No Qualifier. Partial display mode control. HNCQ = HI when no display-qualified clock has occurred for more than approximately 20 ms.	Schematic 13, A1U47C, PIN 8
HNQL	HI, No Qualifier. NO QUAL indicator light control signal. HNQL = HI when no display qualifier has occurred for more than approximately 100 ms.	Schematic 13, A1U49C, PIN 10
HNTRG	HI, No Trigger. NO TRIG indicator light control signal. HNTRG = HI when no trigger has occurred for more than approximately 100 ms.	Schematic 13, A1U49A, PIN 1
HOCT	HI, Octal. Table display format control signal (dc level). When HOCT = HI, table is five 3-bit bytes with MSB left over. When HOCT = LO, table format is four 4-bit bytes.	Schematic 15, A8U35, PIN 6
HPOS	HI, Positive. Display control signal (dc level). When HPOS = HI, most-positive logic state is displayed as a "1". When HPOS = LO, most-positive logic state is displayed as a "0".	Schematic 4, LOGIC POS/NEG Switch A5S1E
HPTS	HI, Pattern Trigger Stored. Control signal for indicator light logic. When HPTS is HI, NO TRIG light is held off.	Schematic 8, A1U71B, PIN 10

Table 4-1. Model 1600A Mnemonics (Cont'd)

TERM	FUNCTION	ORIGIN
HRBL	HI, Reset Button Latched. Data index control signal. When HRBL goes HI, HVGT is forced HI.	Schematic 11, A1U94A, PIN 5
HRECL	HI, Reset Clock. Clocking signal for digital delay and trigger generator during reset function (LRST = LO).	Schematic 8, A1U68B, PIN 6
HRES	HI, Reset. Reset pulse used in digital delay and trigger generator circuit. HRES is derived from LRST.	Schematic 8, A1U68A, PIN 10
HR1	HI, Reset 1. When HI, HR1 indicates that a reset has been requested and will happen on next input clock.	Schematic 11, A1U93A, PIN 6
HRSTR	HI, Reset Start. Reset control signal. When RESET pushbutton is depressed, HRSTR initiates manual reset.	Schematic 4, RESET switch A5S1D
HSA	HI, Select A. Display control signal (dc level). HSA = HI when table A is selected for display.	Schematic 4, B pushbutton A4S1E
HSB	HI, Select B. Display control signal (dc level). HSB = HI when table B is selected for display.	Schematic 4, A pushbutton A4S1B
HSSS	HI, Single Sample Start. Complement of LSSS. In table displays, HSSS disables HVGT at instrument turn-on ensuring display on CRT in SINGLE mode. HSSS = HI at instrument turn-on. Once LRST occurs, HSSS remains LO.	Schematic 19, A8U6A, PIN 5
HSTAB	HI, Store A in B. B-memory control signal. When STORE A→B pushbutton is pressed, contents of A-memory are written into B-memory during display cycle.	Schematic 4, STORE A→B switch A4S1A
HSTR	HI, Start. Data acquisition/display control signal (dc level). HSTR = HI when START DSPL is selected or map mode is selected.	Schematic 10, A7U9B, PIN 5

Table 4-1. Model 1600A Mnemonics (Cont'd)

TERM	FUNCTION	ORIGIN
HSWA	HI, Select Write Address. Address control signal. When HSWA is HI, memory is addressed by write address counter.	Schematic 10, A1U46B, PIN 9
HL	HI, Local. Data acquisition control signal. HL = HI when local flip-flop is set.	Schematic 7, A1U67B, PIN 9
HTB	HI, Trigger Bus. Data acquisition control signal (dc level). HTB = HI when SRC LOCAL/BUS switch is set to BUS. When HI, Model 1600A will trigger only when its trigger word and the Model 1607A trigger word are true simultaneously in the trigger bus mode.	Schematic 20, LOCAL/BUS Switch A7S1E
HTC	HI, Terminal Count. Data index control signal. HTC = HI when data index counter is at terminal count.	Schematic 11, A1U94B, PIN 9
HTRG	HI, Trigger. HTRG goes HI when trigger word is found and remains HI until data acquisition section is reset.	Schematic 11, A1U88D, PIN 11
HTWO	HI, Trigger Word ON. Data acquisition control signal (dc level). HTWO enables TRIGGER WORD switches. HTWO = HI when OFF/WORD switch is set to WORD (in position).	Schematic 20, WORD OFF/ON Switch A8S1F
HVGT	HI, Vertical Greater Than. Display control signal to blank CRT when display section addresses invalid data in memory. HVGT = HI when vertical state count is greater than data index count.	Schematic 11, A1U97, PIN 15
HWE	HI, Write Enable. Data index control signal. HWE = HCLQ · HCL · LDR	Schematic 11, A1U88A
HXRPR	HI, External Repetitive Reset. External repetitive reset signal to Model 1607A.	Schematic 18, A8U6B, PIN 10
H0-H3	Horizontal State Count. Each four-bit word indicates address of a specific bit of current displayed word.	Schematic 16, A8U28, Pins 11, 12, 13 and 14

Table 4-1. Model 1600A Mnemonics (Cont'd)

TERM	FUNCTION	ORIGIN
LARM	LO, Armed. Control signal trigger generator circuit and indicator and control logic. LARM = LO when ARM and HARME are both HI, or when HARME = LO.	Schematic 8, A1U71A, PIN 6
LA≠B	LO, A not equal to B. Reset control signal in HALT A ≠ B sample mode. When A-memory contents differ from B-memory contents; LA ≠ B disables the repetitive reset circuit, locking the Model 1600A in the single sample mode.	Schematic 19, A8U23B, PIN 8
LCLQ	LO, Clock Qualified. Complement of HCLQ.	Schematic 7, A1U41C, PIN 8
LCRCL	LO, Circle. Complement of HCRCL.	Schematic 16, A8U20B, PIN 9
LDR	LO, Data Ready. Control signal used to initiate display cycle. LDR goes LO when data acquisition is complete.	Schematic 11, A1U92, PIN 8
LDSPR	LO, Display Reset. Display resets signal.	Schematic 19, A8U12B, PIN 8
L∆T	LO, Delta T. Clocking signal for pattern recognition, data index and control, and memory. L∆T is derived from PCLK.	Schematic 9, A1U42B, PIN 8
LECMP	LO, Enable Compare. Enable signal for trigger word intensify comparator U86.	Schematic 7, DSPLY/TRIG Switch A1S1C, Schematic 20, OFF WORD Switch A7S1F
LEXOR	LO, Exclusive OR. Control signal (dc level). When LEXOR = LO, A-memory data is compared with B-memory data and bit differences are displayed as intensified one's.	Schematic 4, A & (A + B) Switch A4S1D
LGD	LO, Good Data. Complement of HGD.	Schematic 19, A8U15D, PIN 11

Table 4-1. Model 1600A Mnemonics (Cont'd)

TERM	FUNCTION	ORIGIN
LHAB	LO, Halt A not equal B. Reset control signal (dc level). LHAB is used to derive LA ≠ B.	Schematic 4, HALT A ≠ B switch A5S1B
LHZ	LO, Horizontal Zero. One/Zero Switch A7U19A control signal. When LHZ = LO; horizontal one/zero switch is turned on, applying 100 kHz sinewave to CRT X-axis.	Schematic 15, A8U33, PIN 7
LMAP	LO, Map. Display Control signal (dc level). LMAP = LO when a map display mode is selected.	Schematic 4, MAP NORM/EXP switches A4S1F/G
LNARM	LO, No Arm. NO ARM indicator light control signal, LNARM = LO when no arming signal has occurred for more than approximately 100 ms.	Schematic 13, A1U72B, PIN 8
LNCK	LO, No Clock. NO CLOCK indicator light control signal. LNCK = LO when no display-qualified clock signal has occurred for more than approximately 100 ms.	Schematic 13, A1U47D, PIN 11
LNDLY	LO, No Delay. Data acquisition control signal (dc level). LNDLY = LO when DELAY OFF/ON switch is set to OFF.	Schematic 20, DELAY OFF/ON Switch A7S1A
LRHS	LO, Reset HI Start. Start flip-flop reset signal.	Schematic 11, A1U93A, PIN 5
LRST	LO, Reset. Reset signal for data acquisition section. LRST occurs at end of display cycle.	Schematic 18, A8U17, PIN 8
LR2	LO, Reset 2. Data index and control reset signal.	Schematic 11, A1U93B, PIN 7
LSS	LO, Single Sample. Reset control signal (dc level). LSS = LO when SGL sample mode is selected.	Schematic 4, SGL Switch, A5S1C

Table 4-1. Model 1600A Mnemonics (Cont'd)

TERM	FUNCTION	ORIGIN
LSSS	LO, Single Sample Start. LSSS disables blanking and display reset at instrument turn-on ensuring display on CRT in single sample mode. LSSS = LO at instrument turn-on. First LRST sets LSSS = HI.	Schematic 19, A8U6A, PIN 6
LSWA	LO, Select Write Address. Complment of HSWA.	Schematic 10, A1U46B, PIN 7
LTRG	LO, Trigger. LTRG is inverted and routed to display section to control blanking.	Schematic 11, A1U91, PIN 8
LTRQ	LO, Trigger Qualified. Qualifier control signal. When LTRQ = LO, HCLQ is held HI.	Schematic 7, DSPLY/TRIG Switch S1S1C
LVTC	LO, Vertical Terminal Count. Display control signal. LVTC indicates vertical state counter is at terminal count.	Schematic 16, A8U36A, PIN 2
LVZ	LO, Vertical Zero. One/Zero Switch U19B control signal. When LVZ = 0; vertical one/zero switch is turned on, applying 100 kHz sinewave to CRT Y-axis.	Schematic 15, A8U33, PIN 4
LWDX	LO, Write Disable External. B-memory control signal from external device on I/O bus. LWDX = LO disables B-memory write function.	Schematic 22, J6, PIN 5
LWE1	LO, Write Enable 1. Memory address control signal. LWE1 = LO enables HSWA and LSWA.	Schematic 11, A1U90A, PIN 6
LWE2	LO, Write Enable 2. Clock signal for write address counter.	Schematic 11, A1U90B, PIN 8
LXBNK	LO, External Blanking. Blanking control signal from Model 1607A. LXBNK blanks table B character currently addressed.	Schematic 22, J6, PIN 21

Table 4-1. Model 1600A Mnemonics (Cont'd)

TERM	FUNCTION	ORIGIN
LXMR	LO, External Manual Reset. External manual reset signal to Model 1607A for data index and control circuitry.	Schematic 15, I/O PORT Connector J6
LXPG1	LO, External Plugged 1. External Display control signal from Model 1607A. LXPG1 allows Model 1607A to control reset and table B blanking in I/O bus operation.	Scheamtic 22, J6, PIN 24
LXPG2	LO, External Plugged 2. External B-memory control signal. LXPG2 enables an external device to override B-memory.	Schematic 22, J6, PIN 25
LXPG3	LO, External Plugged 3. External B-memory control signal. LXPG3 enables data from an external device to be written into B-memory.	Schematic 22, J6, PIN 3
LXPMP	LO, Expand Map. Display control signal (dc level). LXPMP = LO when EXP map mode is selected.	Schematic 4, EXP switch A4S1G
L1600	LO, 1600. Control signal to Model 1607A enabling the Model 1600A to exercise control of the Model 1607A display section.	Schematic 22, I/O PORT Connector J6, PIN 35
LØ	LO, Zero. Blanking control signal indicating vertical state coutn = 0.	Schematic 17, A8U21C, PIN 8
MD0-15	Map Data Bits 0-15. 16-bit parallel data from A-memory applied to horizontal and vertical decoders MD0-15 drive the D/A converters in map display modes.	Schematic 12, A1U35-38, PINS 7, 4, 12, 9
NCLK	Negative (Transition) Clock. A buffered TTL reproduction of the clocking signal from the system under test, the complement of PCLK.	Schematic 5, CLOCK INPUT Connector A1J1, PIN 11
Q0, Q1	Qualifiers 0 and 1. Input qualifier bits 0 and 1 from data probes.	Scheamtic 5, Q1, Q0/ INPUTS 15 - 12 Connector A1J2, PINS 11 and 12

Table 4-1. Model 1600A Mnemonics (Cont'd)

TERM	FUNCTION	ORIGIN
SI	Slope Invert. Clock slope command signal to the Clock Probe. The complement of SS. SI = HI when CLOCK is ↑ (out) and LO when CLOCK is ↓ (in).	Schematic 5, CLOCK ↑ / ↓ Switch A1S1B
SQOH, SQ1H	Buffered QUALIFIER Q0/Q1 switch outputs for HI position. TERM = +5 V when applicable switch is set to HI and ≈ 0V when set to OFF or LO.	Schematic 6, A1U24A, PIN 2; A1U24B, PIN 4
SQOL, SQ1L	Buffered QUALIFIER Q0/Q1 switch outputs for LO position. TERM = +5 V when applicable switch is set to LO and ≈ 0V when set co OFF or HI.	Schematic 6, A1U24C, PIN 6; A1U24F, PIN 5
SS	Slope Switch. Clock slope command signal to Clock Probe. SS and SI control PCLK and NCLK leading edge transitions in reference to clocking signal from system under test. SS = LO when CLOCK is ↑ (out) and HI when CLOCK is ↓ (in).	Schematic 5, CLOCK ↑/↓ Switch A1S1B
SOH - S15H	Buffered TRIGGER WORD switch outputs for HI position. TERM = +5 V when applicable switch is set to HI and ≈ 0V when set to OFF or LO.	Schematic 6, A1U19 thru U24
SOL - S15L	Buffered TRIGGER WORD switch outputs for LO position. TERM = +5 V when applicable switch is set to LO and ≈ 0V when set to OFF or HI.	Schematic 6, A1U19 thru U24
THRESHOLD	A dc level applied to the Clock and Data Probes which matches probe comparator switching threshold to the switching threshold of the system under test.	Schematic 5, A1U48, PIN 6
TQ0, TQ1	Temporary Storage flip-flop qualifier output bits 0 and 1.	Schematic 7, A1U9, PINS 6 and 8
$\overline{TQ0}$, $\overline{TQ1}$	Complemented Temporary Storage flip-flop qualifier output bits 0 and 1.	Schematic 7, A1U9, PINS 5 and 9
TO - T15	Temporary Storage flip-flop output bits 0 through 5.	Schematic 7, A1U1 thru U8, PINS 6 and 8

Table 4-1. Model 1600A Mnemonics (Cont'd)

TERM	FUNCTION	ORIGIN
V0 - V3	Vertical State Count. Four-bit address of word currently being displayed.	Schematic 16, A8U29, PINS 11, 12, 13 and 14
VM0-5	Vertical Multiplexer 0-5. 6-bit coded data that selects location where words are written on the CRT. This code separates the words into groups of 2 and 4.	Schematic 16, A8U29, PINS 11 - 14 A7U7B, PIN 6 A7U8, PIN 4
WA0 - WA3	Write Address Count. WA0 - WA3 address memory during write function.	Schematic 10, A1U6, PINS 14, 13, 12 and 11
XDSPD	External Display Data. Data bit from Model 1607A currently being addressed by XV0 - XV3 and XH0 - XH3. Signal is routed to Model 1600A via I/O Bus for display on table B.	Schematic 22, I/O PORT J6, PIN 14
XH0 - XH3	External Horizontal State Count. Bit address from Model 1600A display section routed to Model 1607A.	Schematic 16, A8U41, PINS 11, 8, 3 and 6
XV0 - XV3	External Vertical State Count. Word address from Model 1600A display section routed to Model 1607A.	Schematic 16, A8U42, PINS 11, 8, 3 and 6
1D0-3, 2D0, 2D3, 3D0, 3D3, 4D0, 4D3, 5D0, 5D3	Outputs from DELAY switch used to derive HE. Term is XDY where X = decade and Y = bit of 4-bit code.	Schematic 8, A10S1

SECTION V

PERFORMANCE CHECKS AND ADJUSTMENTS

5-1. INTRODUCTION.

5-2. This section contains performance checks and adjustment procedures for your instrument. The performance tests, which begin with paragraph 5-7, verify that your instrument meets its published specifications (table 1-1). Adjustment procedures, beginning with paragraph 5-21, are provided to help you maintain your instrument within specification limits.

5-3. RECOMMENDED TEST EQUIPMENT.

5-4. Equipment required for the performance checks, adjustment procedures, and troubleshooting is listed in table 5-1, Recommended Test Equipment. Any equipment that satisfies the critical specification given in the table may be substituted for the recommended models.

5-5. CHECK RECORD.

5-6. A Performance Check Record form is provided at the end of this section for the purpose of recording the results of the performance checks. This form may be removed from your manual and retained as a permanent record of the incoming inspection or routine maintenance performed on the instrument. Be sure to include the instrument serial number on the record for identification.

5-7. PERFORMANCE CHECKS.

5-8. The following checks verify that your instrument is operating within the specifications outlined in table 1-1 of this manual. If it has been determined, after completing the performance checks, that the instrument does not meet one or more of its specifications; refer to paragraph 5-21, Adjustment Procedures, and Section VIII, Schematics and Troubleshooting.

5-9. INITIAL OPERATIONAL CHECK. Perform the operator's checks listed in Section III to verify proper operation of the display functions in the Model 1600A. To verify proper operation of the instrument acquisition functions, perform the following procedure.

NOTE

The test equipment setup for the initial operational check is used as a basis for several functional and specification checks.

a. Connect equipment as shown in figure 5-1.

b. Apply waveform shown in figure 5-2A to clock probe input. Apply waveform shown in figure 5-2B to data probe inputs 0-15.

c. Set Model 1600A controls as follows:

CLOCK	_|‾
THLD	TTL
QUALIFIER Q1, Q0	OFF
SAMPLE MODE	REPET
START DSPL	ON
TRIGGER MODE	
NORM/ARM	NORM
LOCAL/BUS	LOCAL
WORD	ON
TRIGGER WORD -	
MAP LOCATOR	ALL HI
DISPLAY MODE	TABLE A

d. Alternately switch each TRIGGER WORD switch to LO and back to HI. Observe that NO TRIG lamp turns on and loss of display occurs when switch is set to LO.

e. Ground each data probe separately. Observe that loss of display and no trigger indication occur when probe is grounded.

5-10. SPECIFICATION CHECK. The following paragraphs check the instrument performance to specifications listed in table 1-1.

5-11. Repetition Rate. Specification: 0 to 20 MHz.

a. Set Model 1600A controls per paragraph 5-9, step c and apply waveforms shown in figure 5-3.

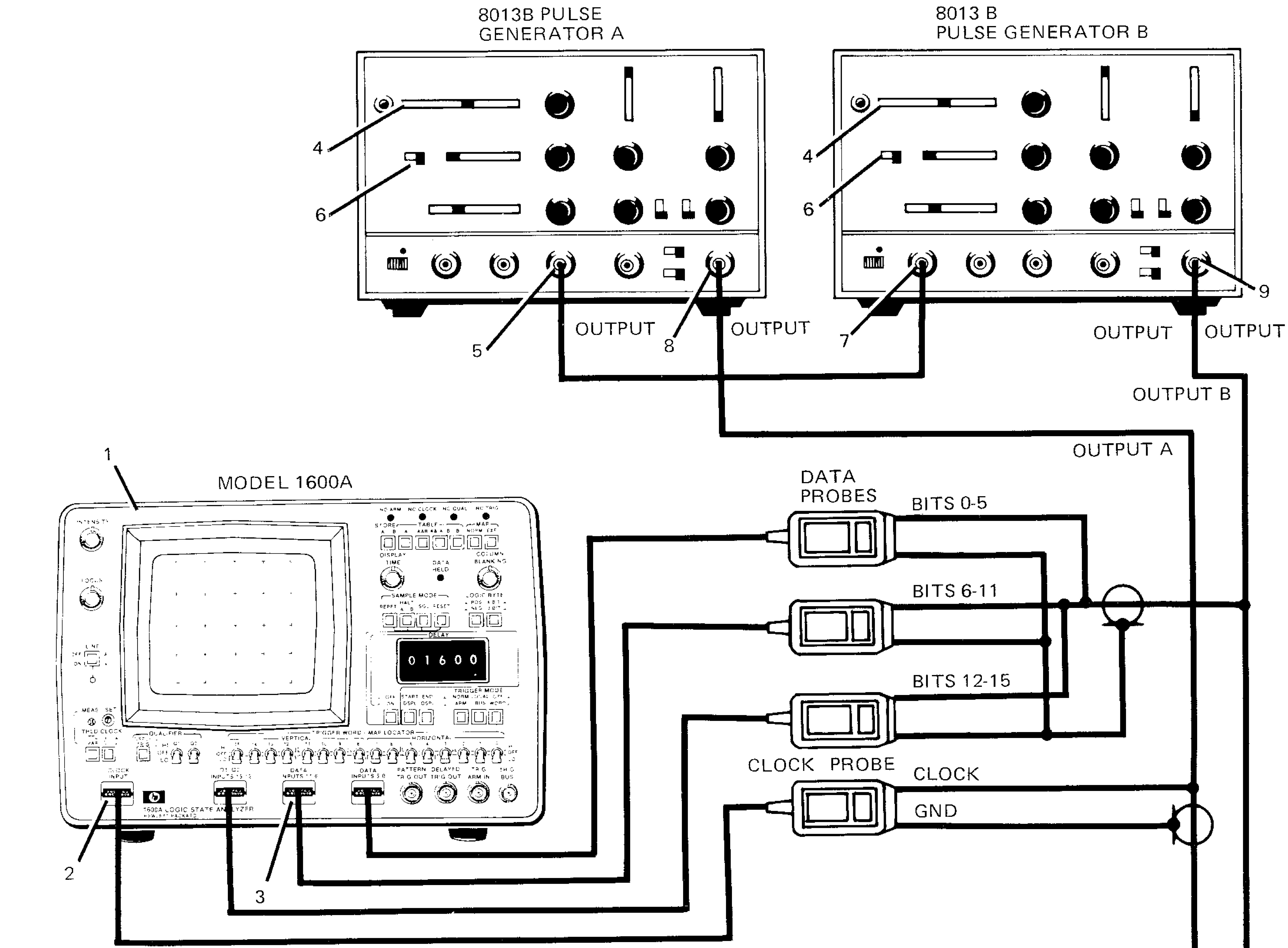
b. Observe that display is all 1's and NO CLOCK and NO TRIG indicators are off. This check verifies that the Model 1600A is properly accepting data at the maximum specified repetition rate.

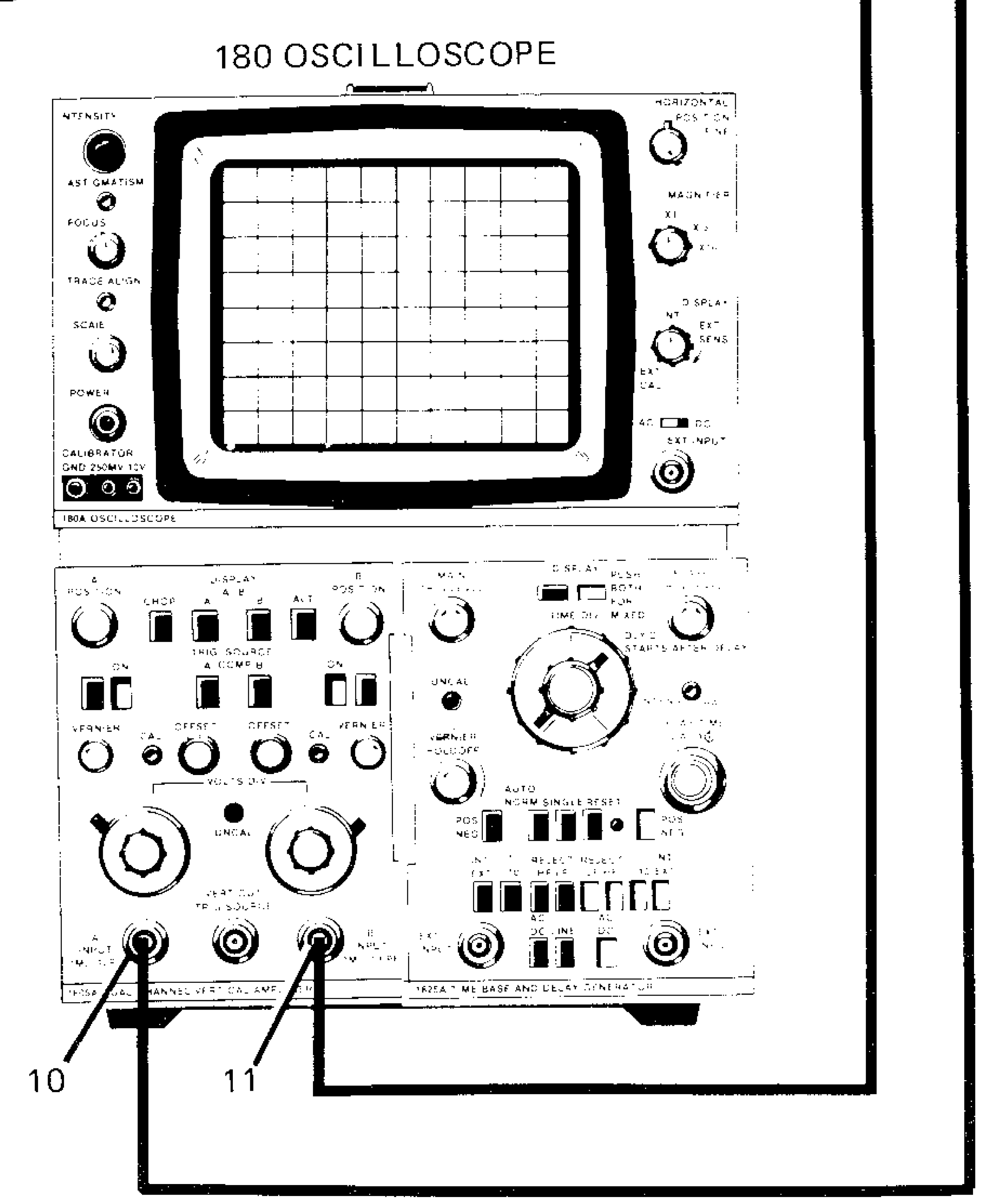
5-12. Input RC: Specification: Probe, 40 kΩ ±3 kΩ shunted by less than 14 pF.

a. Using a multimeter, measure the resistance between each data-probe input and ground. Also measure the resistance between clock-probe input and ground. Observe that input impedance of clock and data probes is 40 kΩ ±3 kΩ.

Table 5-1. Recommended Test Equipment

Instrument		Required Characteristics	Required For
Type	Model		
Clock Probe	HP 10230B	No substitute	Performance Check Troubleshooting
Six-bit Data Probe	HP 10231B	No substitute	Performance Check and Troubleshooting
Monitor Oscilloscope	HP 180 Mainframe with plug-ins	General purpose, >100 MHz; Sweep Speeds of 10 ns/DIV	Performance Check, Adjustments, and Troubleshooting
Vertical Plug-in	HP 1805A	50-ohm input, 100-MHz bandwidth	Performance Check and Troubleshooting
Time Base Plug-in	HP 1825A	10 ns/div, 100-MHz bandwidth	Performance Check and Troubleshooting
Pulse Generators (2)	HP 8013B	Adjustable 0 to 20 MHz; Adjustable 0 to 5 V pk amplitude; Positive and Negative Polarity; Adjustable 20 ns to 0.5-μs width; Adjustable 0 to 5-V offset	Performance Check and Troubleshooting
Multimeter	HP 3469B	Dc current 0 to 30 μA; dc voltage, 0 to 10 V; Resistance, 0 to 43 kilohms	Performance Check, Adjustments, and Troubleshooting
LCR Meter	HP 4332A	Capacitance, 0 to 25 pF	Performance Check and Troubleshooting
50-ohm BNC feedthrough	HP 11048B	50-ohm feedthrough termination	Performance Check
Function Generator	HP 3310A	±10 V offset	Performance Check
Counter	HP 5300A HP 5302A	Period Measurement	Performance Check
Logic Analyzer	HP 1601A	Pattern recognition and State Display	Troubleshooting
Logic Trouble-shooting Kit	HP 5015T	Logic Pulser, Logic Probe, Logic Clip	Troubleshooting
High Voltage Probe	K05-3440A	1000:1 divider ratio 10 GΩ input Z	Adjustments and Troubleshooting





TEST EQUIPMENT SETUPS

PULSE GENERATOR

RATE GENERATOR A, B, & EXT . . .	INTERNAL RATE OF APPROX 1 MHz
DELAY GENERATOR	DELAY OUTPUT OF .01 to .1 μs
OUTPUT GENERATOR A	WIDTH: 0.03 μs OFFSET: 0 Vdc AMPL: +3V pk
OUTPUT GENERATOR B	WIDTH: 0.03 μs OFFSET: 0 Vdc AMPL: +3V pk
MONITOR SCOPE	ADJUST TO VIEW STABLE DISPLAY (TRIGGER ON CHANNEL A SIGNAL)

LEGEND

1. MODEL 1600A
2. CLOCK INPUT
3. DATA INPUTS
4. RATE GENERATOR
5. TRIG OUTPUT
6. DELAY GENERATOR
7. TRIGGER INPUT
8. OUTPUT GENERATOR A OUTPUT +
9. OUTPUT GENERATOR B OUTPUT +
10. CHANNEL A
11. CHANNEL B

Figure 5-1. Operational Check Test Setup

1600A-046

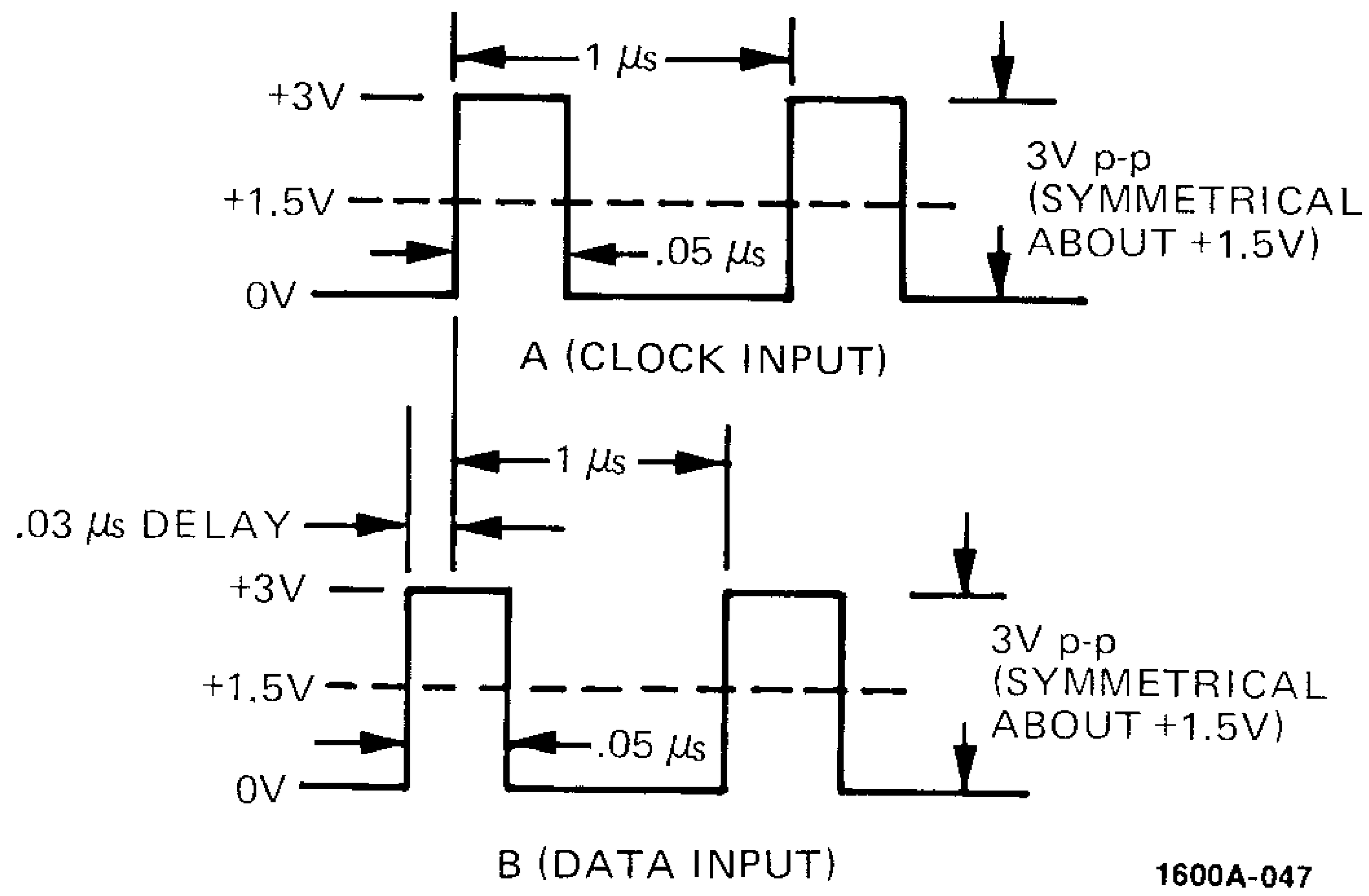


Figure 5-2. Operational Check Input Waveforms

b. Using LCR meter, measure shunt capacitance between each data-probe and clock-probe input and ground. Observe that each input capacitance is less than 14 pF.

5-13. Input Bias Current. Specification: Less than 30 μA.

a. Set THLD to VAR and using a multimeter, monitor VAR MEAS and adjust VAR SET for —10 Vdc.

b. Using multimeter, measure current between each input clock and data probe and ground. Observe that current is less than 30 μA.

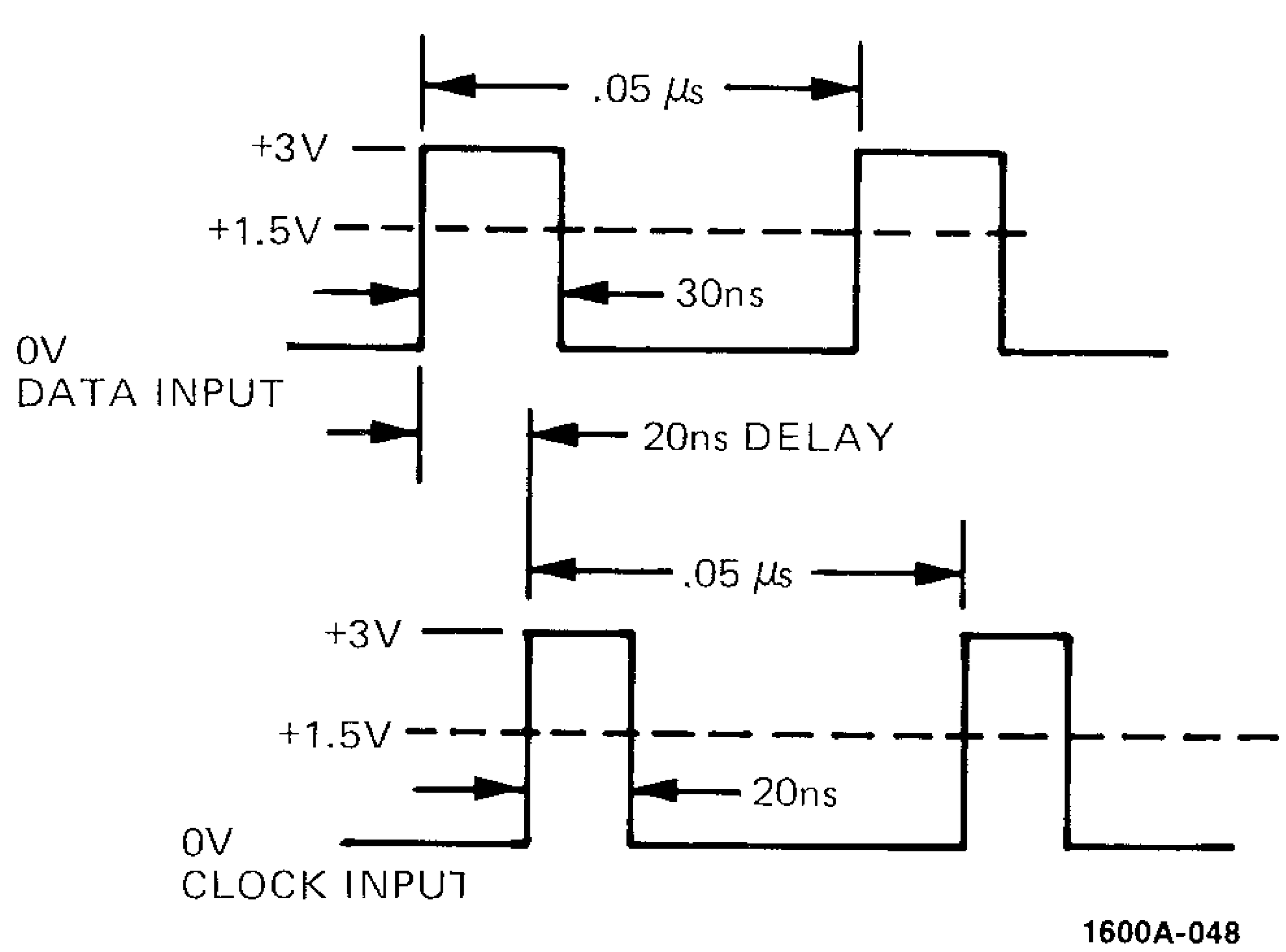


Figure 5-3. Repetition Rate Test Waveforms

5-14. Input Threshold/Swing. Input threshold specification: TTL, fixed at approximately 1.5 Vdc; variable, to ±10 Vdc. Input swing: 0.5 V +5% of threshold voltage p-p (min). Input level: —15 Vdc to +15 Vdc.

a. Remove data and clock probes from Model 1600A.

b. Apply power to Model 1600A and set THLD to VAR.

c. Using multimeter, monitor VAR MEAS while varying VAR SET from limit to limit. Verify that voltage swing is smooth and that limits are greater than or equal to ±10 Vdc.

d. Connect test equipment as shown in figure 5-4.

e. Apply test waveform shown in figure 5-5A to clock- and data-probe inputs of the Model 1600A.

f. Set Model 1600A controls as follows:

CLOCK .... _⌐
THLD .... TTL
START DSPL.......................... ON
WORD.................................. ON
QUALIFIER
  DSPLY/TRIG .... TRIG
  Q1, Q0.................................. HI
TRIGGER WORD -
  MAP LOCATOR............ Bits 0-15 HI

g. Observe that front-panel indicator lights are off.

h. Alternately switch each TRIGGER WORD switch to LO and back to HI. Observe that NO TRIG indicator lamp comes on when switch is set to LO.

i. Apply test waveform shown in figure 5-5B to clock- and data-probe inputs.

j. Set THLD to VAR and adjust VAR SET for valid clock and data inputs (indicator lights off).

k. Repeat step i.

l. Remove 50-ohm scope load and connect function-generator output directly to clock and data probes.

m. Apply test waveform shown in figure 5-5C to clock- and data-probe inputs.

n. Adjust VAR SET for valid data and clock inputs (indicator lights off).

o. Repeat step i.

p. Apply test waveform shown in figure 5-5D to clock- and data-probe inputs.

q. Adjust VAR SET for valid clock and data inputs (indicator lights off).

r. Repeat step i.

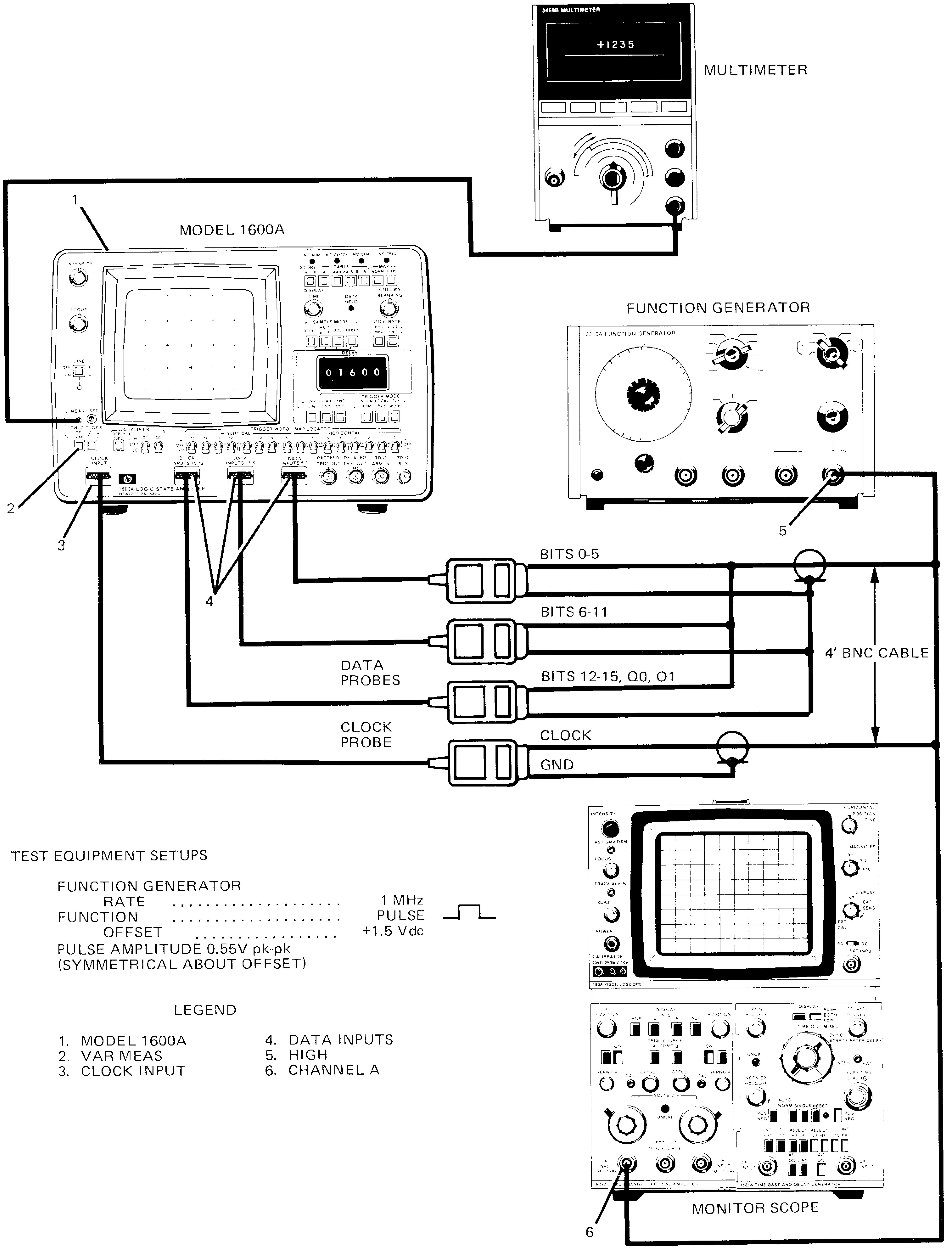


Figure 5-4. Threshold/Logic Swing Test Setup

1600A-049

s. Apply test waveform shown in figure 5-5E to clock- and data-probe inputs.

t. Adjust VAR SET for valid clock and data inputs (indicator lights off).

u. With multimeter connected to VAR MEAS, adjust VAR SET from —1 Vdc to —10 Vdc. Verify that Model 1600A remains triggered.

v. Apply test waveform shown in figure 5-5F to clock- and data-probe inputs.

w. Adjust VAR SET to obtain trigger (indicator lights off).

x. With multimeter connected to VAR MEAS, adjust VAR SET from +1 Vdc to +10 Vdc. Verify that Model 1600A remains triggered.

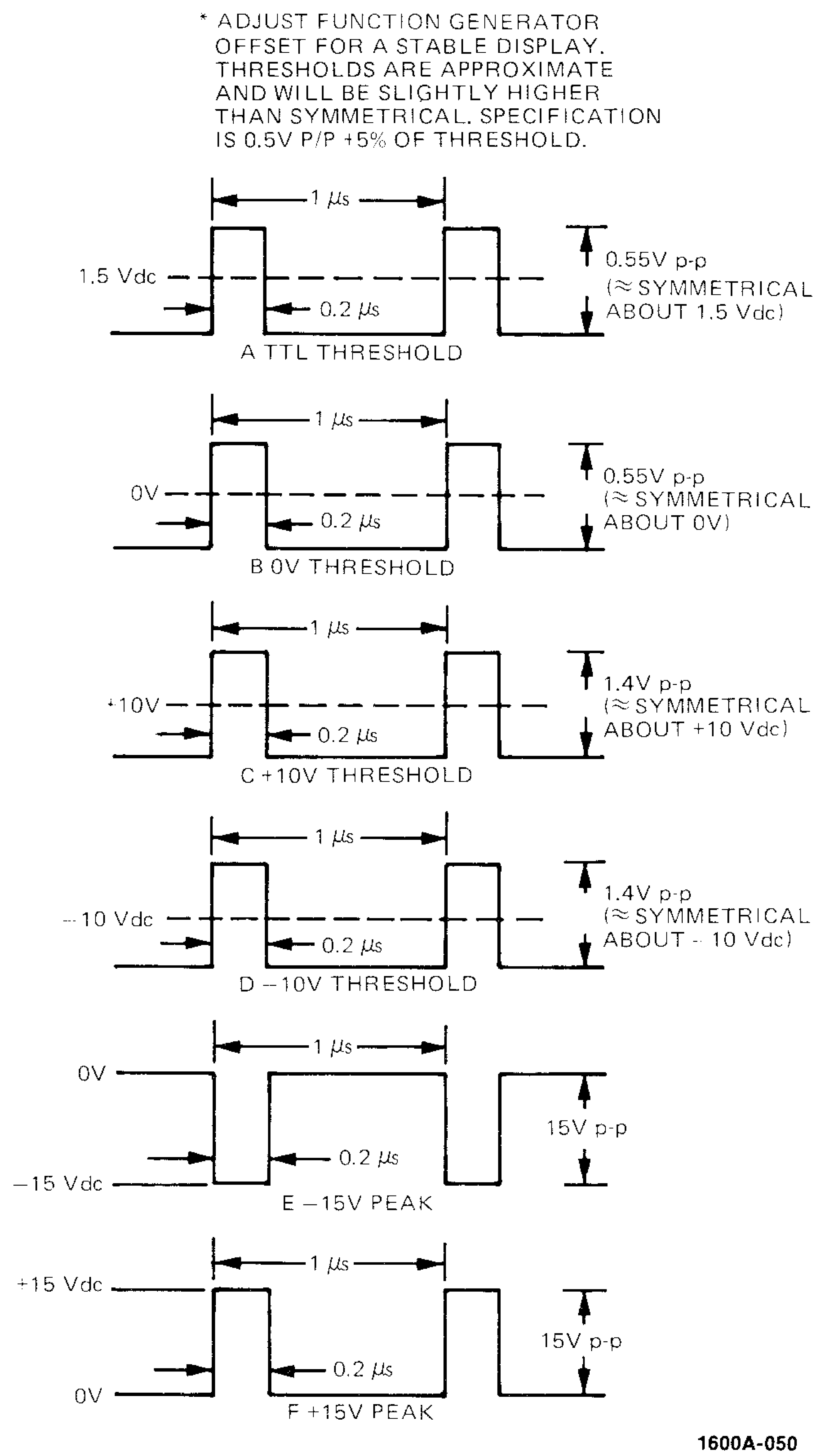


Figure 5-5. Threshold/Logic Swing Test Waveforms

5-15. Minimum Clock-pulse Width. Specification: 20 ns at threshold.

a. Connect test setup as shown in figure 5-1 and set Model 1600A controls as described in paragraph 5-9, step c. Apply test waveforms shown in figure 5-3.

b. Slowly decrease width of pulse applied to CLOCK INPUT of Model 1600A. Verify that NO CLOCK indicator light remains off and that trigger output is present for clock-pulse widths greater than or equal to 20 ns.

5-16. Minimum Data-pulse Width. Specification: 25 ns at threshold.

a. Connect test setup as shown in figure 5-1 and set Model 1600A controls as described in paragraph 5-9, step c. Apply test waveforms shown in figure 5-3.

b. Slowly decrease width of pulse applied to DATA INPUTS of Model 1600A. Observe that Model 1600A remains triggered for pulse widths greater than or equal to 25 ns.

5-17. Setup and Hold Time. Specification: Setup Time, 20 ns minimum; Hold Time, 0 ns minimum.

a. Connect test setup as shown in figure 5-1, and set Model 1600A controls as described in paragraph 5-9, step c.

b. Apply waveforms shown in figure 5-6A.

c. Slowly decrease delay time between leading edge (_|‾) of clock pulse and leading edge (_|‾) of data pulse. Observe that Model 1600A remains triggered and display is stable for delay times greater than or equal to 20 ns.

d. Adjust delay time between pulses so that trailing edge (‾|_) of data pulse is coincident with leading edge (_|‾) of clock pulse as shown in figure 5-6A (hold time). Observe that stable display occurs for 0 hold time.

e. Switch Model 1600A clock slope to (‾|_). Complement pulse generator output to clock probe.

f. Apply waveform shown in figure 5-6B.

g. Slowly decrease delay time between leading edge (‾|_) of clock pulse and leading edge (_|‾) of data pulse. Observe that Model 1600A remains triggered and display is stable for delay times greater than or equal to 20 ns.

h. Adjust delay time between pulses so that trailing edge (‾|_) of data pulse is coincident with leading edge (‾|_) of clock pulse as shown in figure 5-6B (hold time). Observe stable display for 0 hold time.

i. Complement output of pulse generator to data probes, and set all Model 1600A TRIGGER WORD switches to LO.

j. Apply waveforms shown in figure 5-6C.

k. Slowly decrease delay time between leading edge (‾|_) of clock pulse and leading edge (‾|_) of data pulse. Observe that Model 1600A remains triggered and stable display of all zero's occurs for delay times greater than or equal to 20 ns.

l. Adjust delay time between pulses so that trailing edge (_|‾) of data pulse is coincident with leading edge (‾|_) of clock pulse as shown in figure 5-6C (hold time). Observe that stable display occurs for 0 hold time.

m. Switch Model 1600A clock slope to (_|‾) and set pulse generator clock output to normal.

n. Apply waveforms shown in figure 5-6D.

o. Slowly decrease delay time between leading edge (_|‾) of clock pulse and leading edge (‾|_) of data pulse. Observe that Model 1600A remains triggered and display is stable for delays greater than or equal to 20 ns.

p. Adjust delay time between pulses so that trailing edge (_|‾) of data pulse is coincident with leading edge (_|‾) of clock pulse as shown in figure 5-6 (hold time). Observe that stable display occurs for 0 hold time.

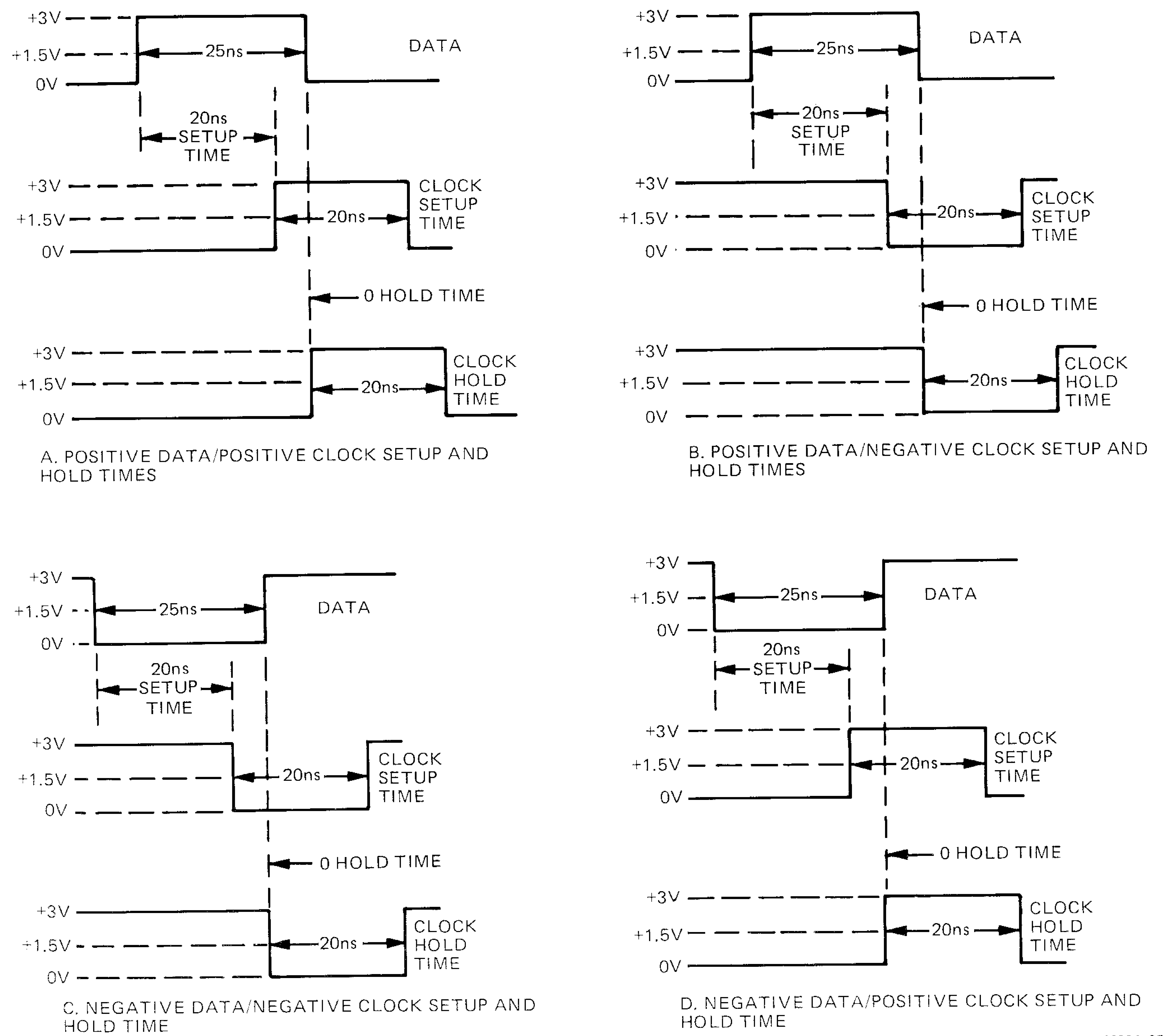
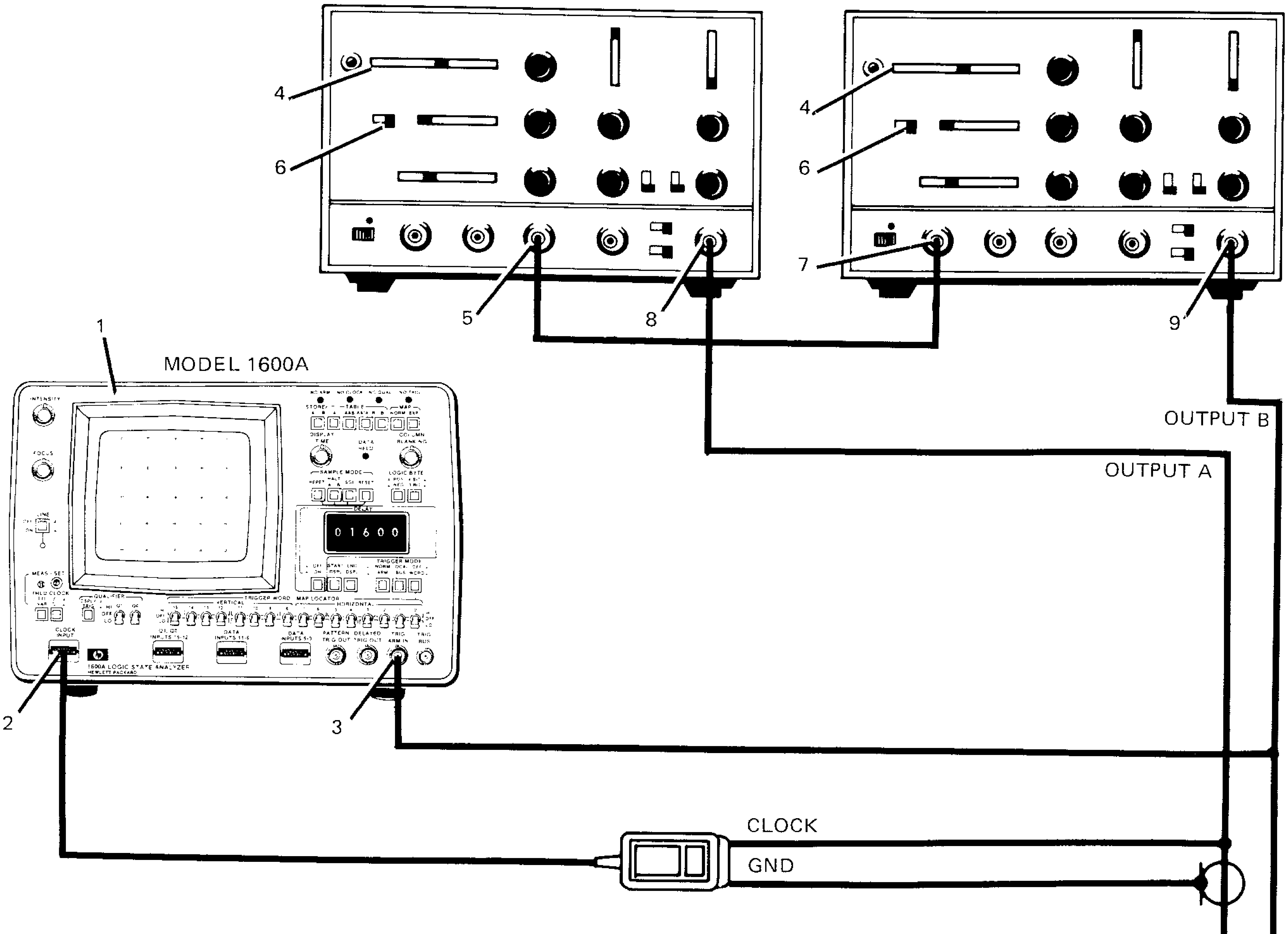


Figure 5-6. Setup and Hold Waveforms

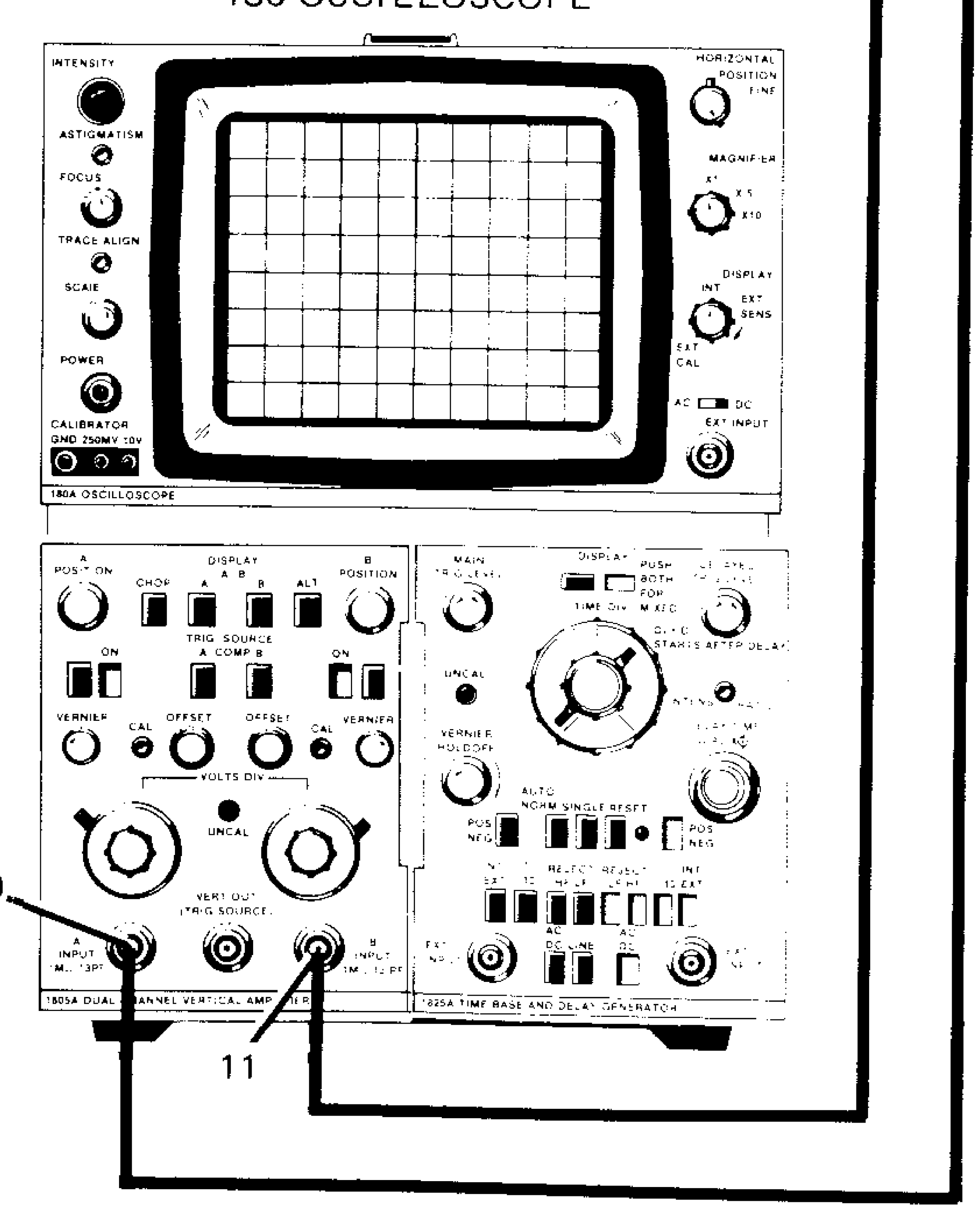


TEST EQUIPMENT SETUPS

PULSE GENERATOR

RATE GENERATOR A, B and EXT	INTERNAL RATE OF APPROX 1 MHz
DELAY GENERATOR	DELAY OUTPUT OF .01 to .1 μs
OUTPUT GENERATOR A	WIDTH: 0.03 μs OFFSET: 0 Vdc AMPL: +3V pk
OUTPUT GENERATOR B	WIDTH: 0.03 μs OFFSET: 0 Vdc AMPL: +3V pk
MONITOR SCOPE	ADJUST TO VIEW STABLE DISPLAY (TRIGGER ON CHANNEL A SIGNAL)

180 OSCILLOSCOPE



LEGEND

1. MODEL 1600A
2. CLOCK INPUT
3. TRIG ARM IN
4. RATE GENERATOR
5. TRIG OUTPUT
6. DELAY GENERATOR
7. TRIGGER INPUT
8. OUTPUT GENERATOR A
9. OUTPUT GENERATOR B
10. CHANNEL A
11. CHANNEL B

Figure 5-7. Trigger Arm Test Setup

1600A-052

5-18. Trigger Arm Input. Specification: Input Impedance, 50 ohms; Input Levels, 0 V ≤ LOW <0.4 V, 2 V < HIGH <5 V; Pulse Width, 15 ns minimum at 1.5 V.

a. Remove power from the Model 1600A.

b. Using multimeter, measure input impedance of the trigger arm input. Observe that measured value is 50 Ω ±2 Ω.

c. Reapply power to Model 1600A.

d. Set Model 1600A controls as follows:

CLOCK	⨼
THLD	TTL
QUALIFIERS Q0, Q1	OFF
SAMPLE MODE	REPET
START DSPL	ON
TRIGGER MODE	
NORM/ARM	ARM
LOCAL/BUS	LOCAL
WORD	ON
TRIGGER WORD	ALL LO

e. Connect test equipment as shown in figure 5-7, and apply waveforms shown in figure 5-8 to CLOCK INPUT and TRIG ARM input.

f. Connect PATTERN TRIG OUT from Model 1600A to channel A of oscilloscope. Trigger oscilloscope on channel A input.

g. Set oscilloscope control for sweep speed of 5 ms and pulse generator to single pulse.

h. Depress pulse generator manual (single pulse) pushbutton. Observe that a sweep occurs for every pulse input.

i. Reset test setup to settings shown in figure 5-7, and apply waveforms shown in figure 5-8.

j. Adjust pulse generator delays from 45 ns to greater than or equal to 75 ns.

k. Set oscilloscope control for sweep speed of 5 ms and pulse generator to single pulse.

l. Depress pulse generator manual (single pulse) pushbutton. Observe that triggered sweep occurs every other pulse input. This verifies the trigger arming conditions specified in table 1-1.

5-19. Display Time. Specification: Variable from <200 ms to >5 s.

a. Set up test equipment per paragraph 5-9, steps a, b, and c.

b. Remove power from Model 1600A and remove bottom cover.

c. Set up timer counter to measure period and connect timer counter input to A1U68, pin 10.

CAUTION

Exercise care to prevent shorting between adjacent pins.

d. Apply power and observe timer counter measurement while varying DISPLAY TIME control from full CCW to full CW positions. Measurements should vary from less than 200 ms for full CCW position of DISPLAY TIME to greater than five seconds for full CW position.

5-20. Pattern Trigger and Delayed Trigger Outputs. Specification: High, >2 V into 50 ohms; Low, <0.4 V into 50 ohms; Width, ≈25 ns (synchronous).

a. Setup test equipment per paragraph 5-9, steps a, b, and c.

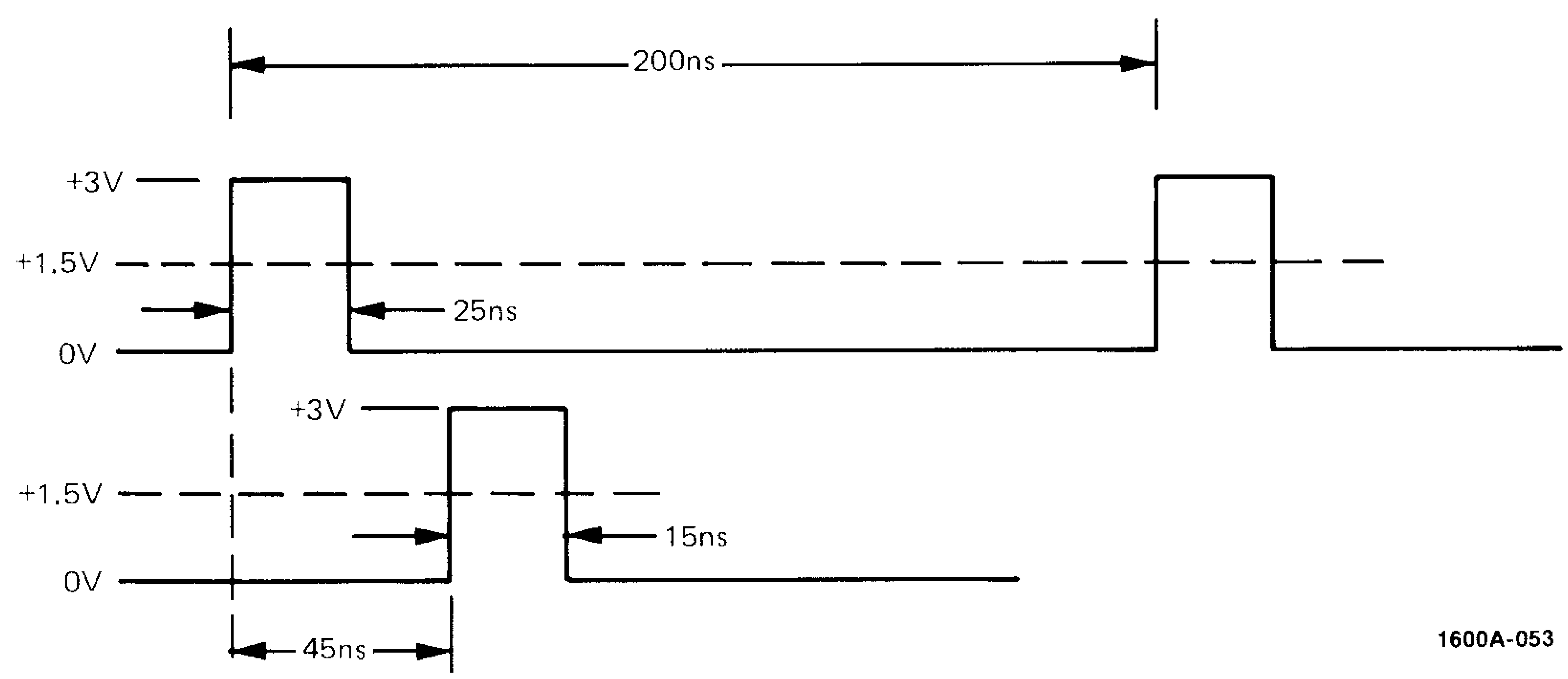


Figure 5-8. Trigger Arm Input Test Waveforms

b. Connect PATTERN TRIG OUT and DELAYED TRIG OUT to channels A and B inputs respectively of oscilloscope.

c. Set delay to all 0's. Observe that output pulses meet specifications listed above.

5-21. ADJUSTMENT PROCEDURES.

WARNING

Read the Safety Summary at the front of this manual before performing adjustment procedures.

5-22. The following is a complete adjustment procedure for the Model 1600A. These procedures should be performed only if it has previously been established by the performance checks that the instrument is out of adjustment. The adjustments can be made separately following repairs to the instrument or in sequence as part of a periodic calibration procedure. The location of adjustments and test points are shown in figures accompanying the adjustment procedures.

CAUTION

Adjustments are performed with top and bottom covers removed. Exercise care to avoid shorting or damaging the internal parts of the instrument.

5-23. +5 VOLT POWER SUPPLY ADJUSTMENT. (Refer to schematic 2 and figure 5-9.)

a. Remove power from Model 1600A.

b. Remove top and bottom covers.

c. Apply power to Model 1600A.

d. While monitoring +5-volt power supply at test point TP1 with respect to ground (TP2), adjust A3R18 for +5 V ±0.01 V.

5-24. TIMING ADJUSTMENTS. (Refer to schematic 9 and figures 5-10 and 5-11.)

a. Set up test equipment as shown in figure 5-1.

b. Perform steps b and c of paragraph 5-9.

c. Switch TRIGGER WORD bit 0 to LO and set Model 1600A to END DSPL mode. Verify that NO TRIG light is on.

d. Disconnect monitor oscilloscope inputs from pulse generator outputs.

e. Externally trigger monitor oscilloscope from clock pulse (OUTPUT A).

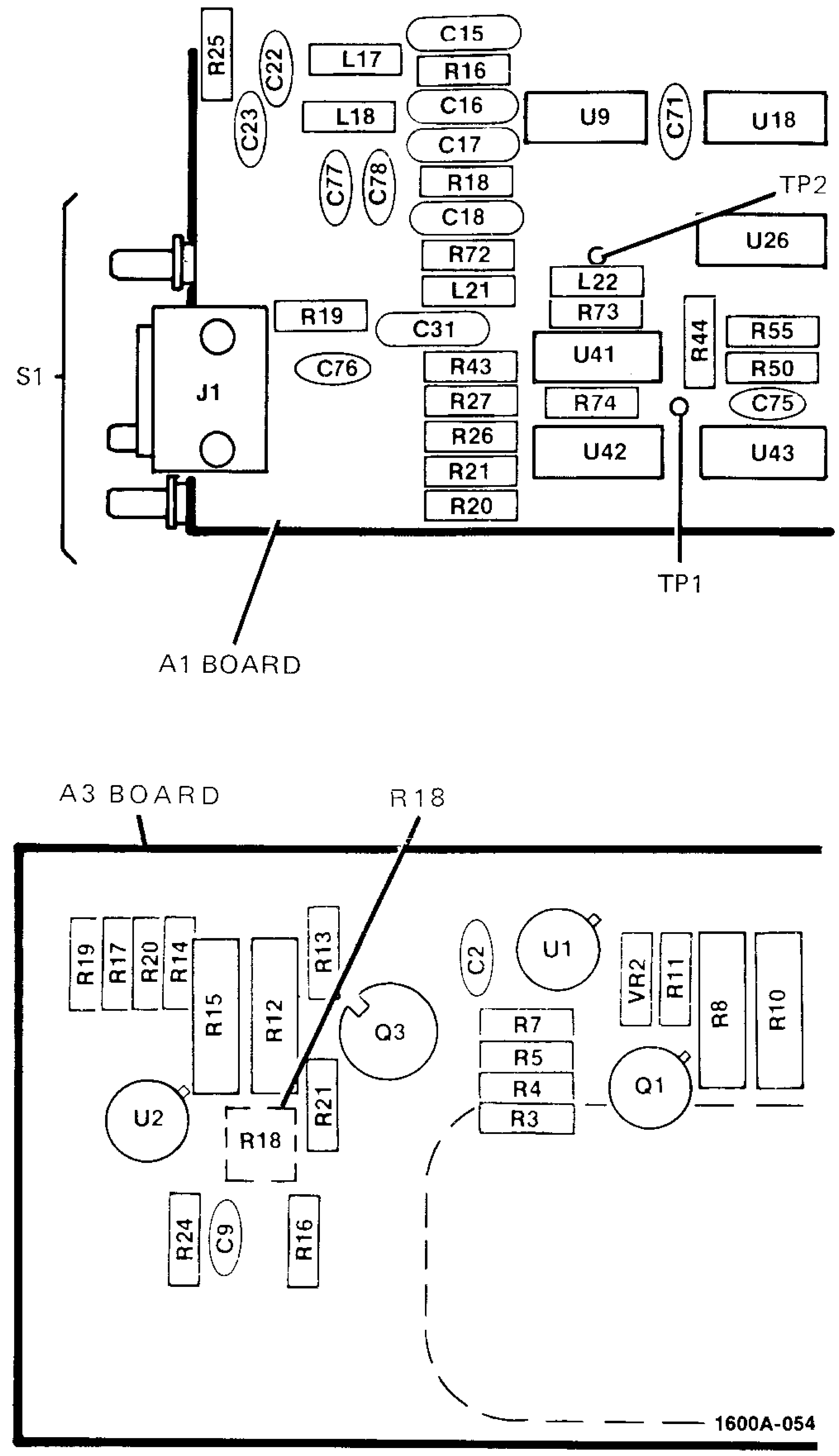


Figure 5-9. +5 Volt Power Supply Adjustment Location

f. Set oscilloscope sweep for 5 ns/cm and oscilloscope vertical sensitivity for 1 volt with X10 probe.

g. Adjust pulse generator rate for 10 MHz.

h. Monitor PCLK at A1U5, pin 3. Adjust monitor oscilloscope to position 1.5 V point on positive edge of PCLK at a reference point.

i. Monitor LWE at A1TP4. Adjust A1C33 for maximum delay between LWE and PCLK.

j. Adjust A1R49 to position LWE 28 ns from PCLK reference.

k. Adjust A1C37 to obtain 26 ns width for LWE.

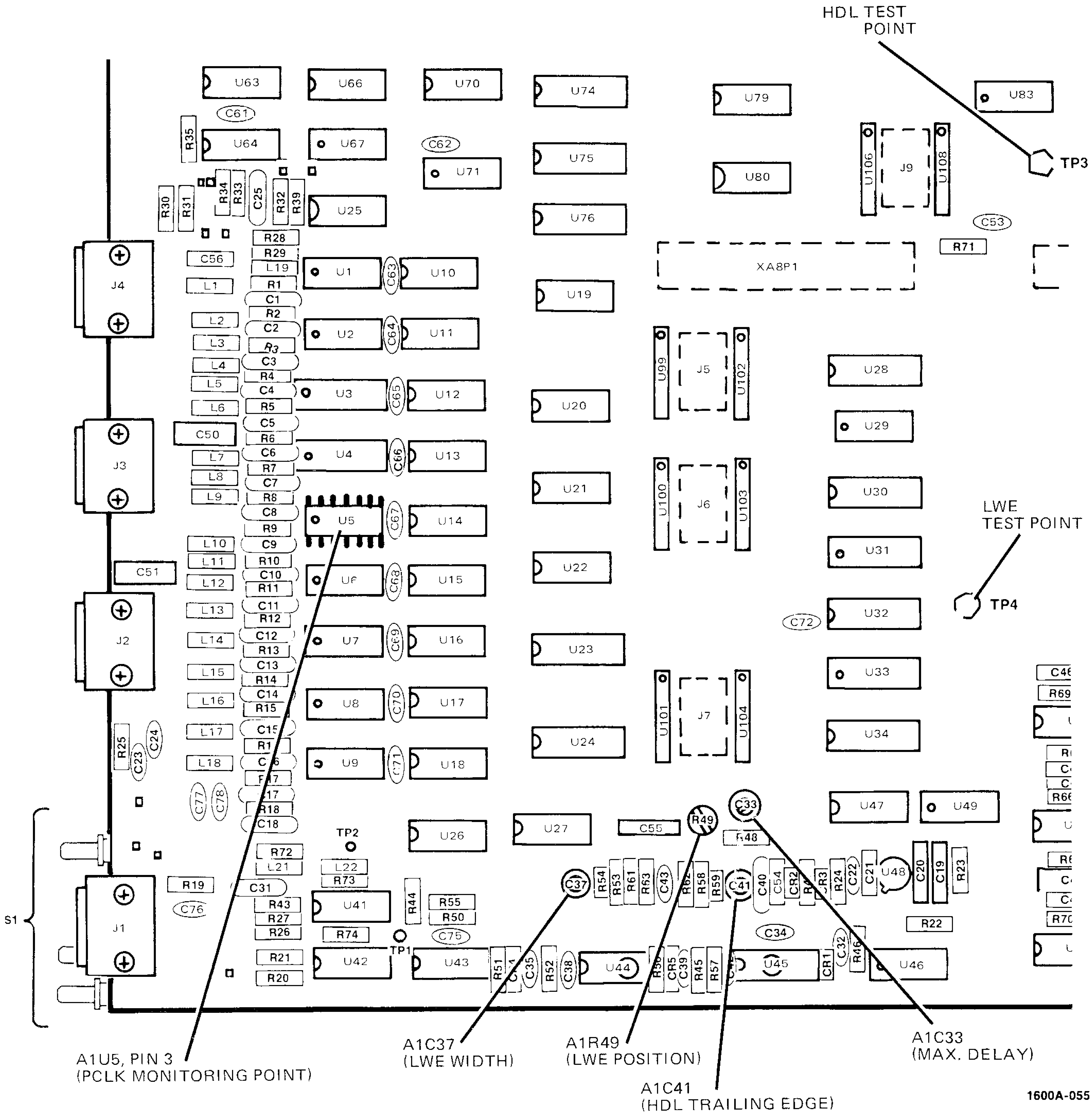


Figure 5-10. Timing Adjustment Locations

l. Monitor delay clock (HDL) at A1TP3. Set trailing edge of HDL 2 ns in advance of trailing edge of LWE by adjusting A1C41.

5-25. HIGH VOLTAGE SUPPLY ADJUSTMENT. (Refer to schematic 3 and figure 5-12.)

a. Monitor high voltage at solder connection of W6 (yellow wire).

b. Adjust A2R17 for +2450 V ±5 V.

5-26. DISPLAY ADJUSTMENTS. (Refer to schematics 3 and 21, and figures 5-12, 5-13, and 5-14.)

a. Adjust X-POSITION and Y-POSITION on rear panel to center display on CRT screen.

b. Adjust X-GAIN and Y-GAIN to obtain full screen display.

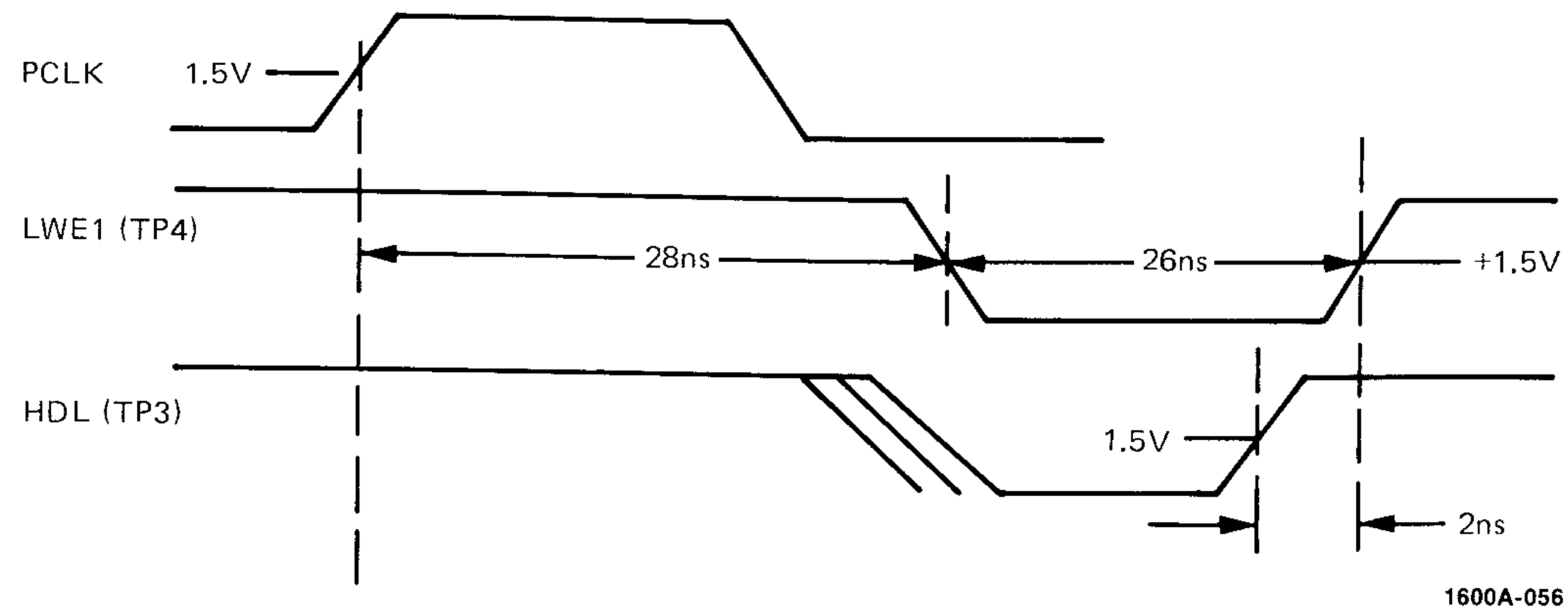


Figure 5-11. Timing Adjustment Waveforms

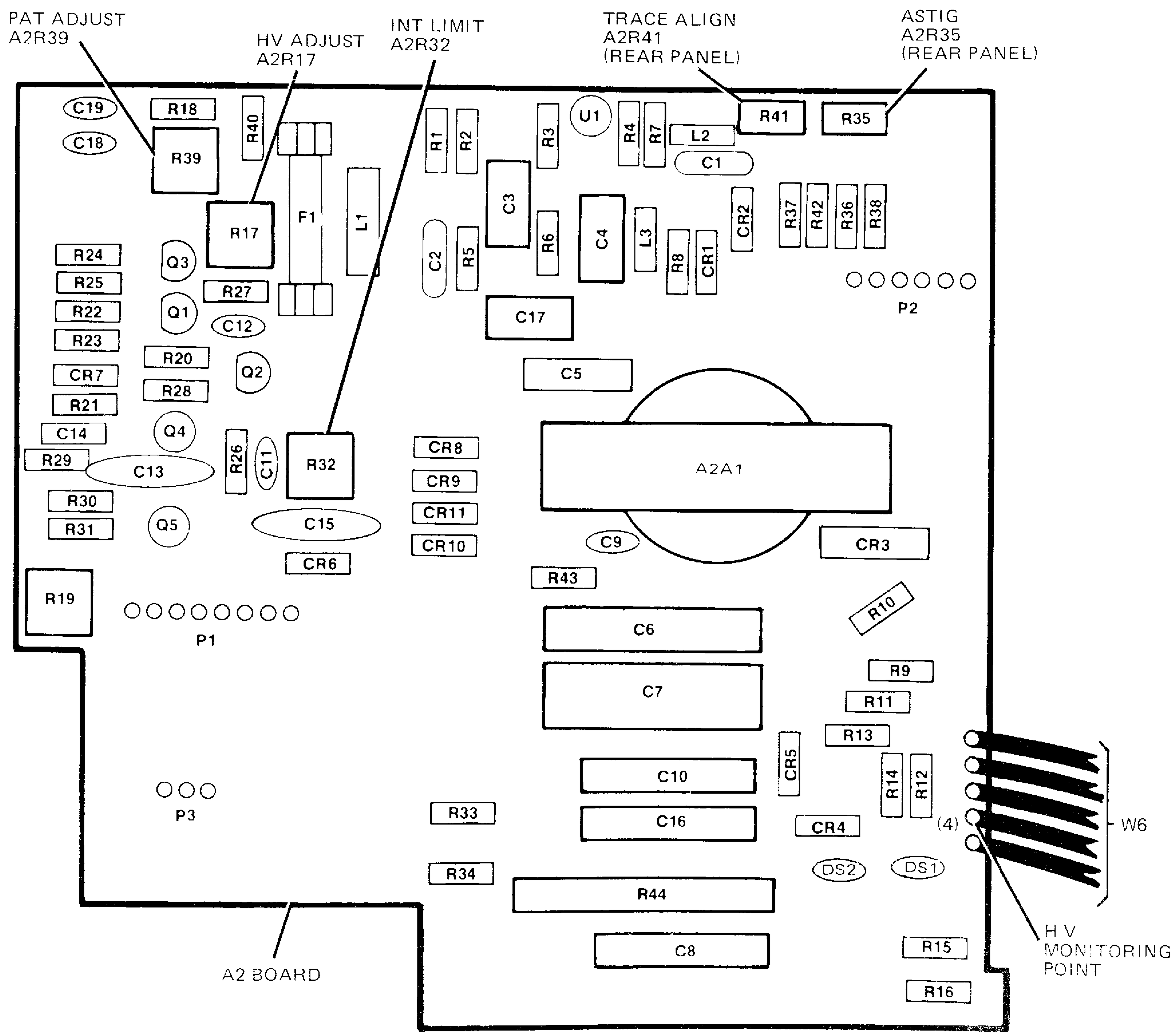


Figure 5-12. High Voltage and Display Adjustment Locations

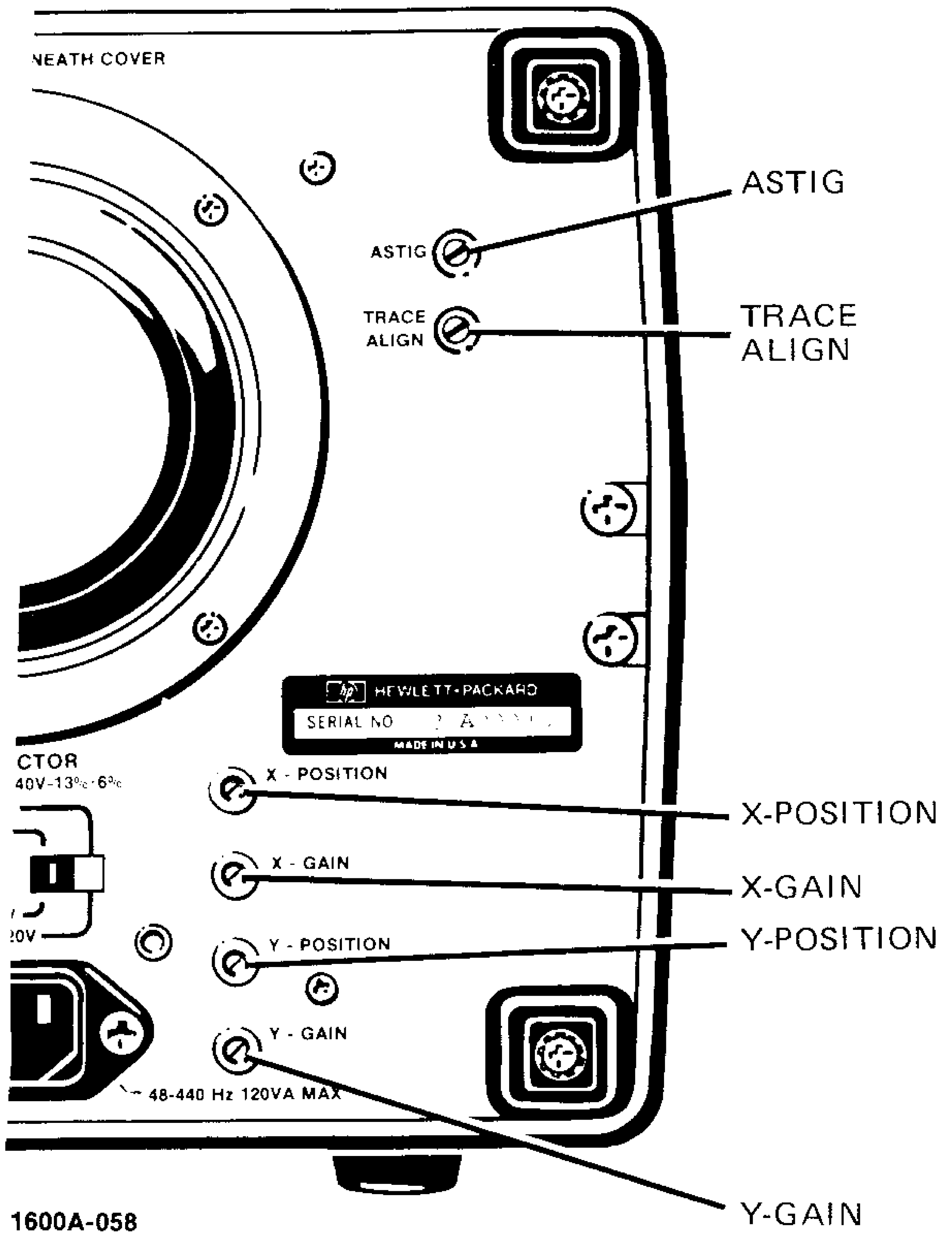


Figure 5-13. Rear Panel Adjustments

c. With INTENSITY (front panel) set to full CW position, adjust INT LIM A2R32 and FOCUS (front panel) to obtain brightest, focused display that can be completely blanked by COLUMN BLANKING control.

d. Adjust ASTIG (rear panel) and PAT (A2R39) to optimize appearance of display.

e. Adjust TRACE ALIGN (rear panel) to obtain display that is parallel to graticule marks.

f. Set up Model 1600A per paragraph 3-48, steps a and b of the operator's checks and adjustments.

g. Adjust character size A7R21 from full CW to full CCW. Verify that display remains on screen.

h. Adjust character size A7R21 for slight space between zeros. Displayed characters should be as large as possible without overlap.

i. Select NORM MAP display mode.

j. Adjust A7R71 (MAP ADJ) for shortest trace between dot locations.

5-27. CUSTOMER MODIFICATIONS.

5-28. 32-BIT WORD DISPLAY. (See figure 5-15.) The Model 1600A displays two 16-bit wide tables in the A & B and A & (A ⊕ B) modes as shipped from the factory. If it is desirable to display one 32-bit wide table on the CRT with proper octal format when BYTE is set to 3 BIT (10 3-bit bytes with 2 MSB's left over), modify the Model 1600A Analog Display Board A7 as follows:

a. Turn off instrument power and remove power cord from rear-panel connector.

b. Remove Analog Display Board A7 from Model 1600A (see disassembly procedure in Section VIII).

c. Remove 10-ohm resistor A7R85.

d. Install 10-ohm resistor A7R84 (not installed at factory).

e. Reinstall Analog Display Board A7 in Model 1600A. The Model 1600A will now display one 32-bit wide table in the A & B and A & (A ⊕ B) display modes.

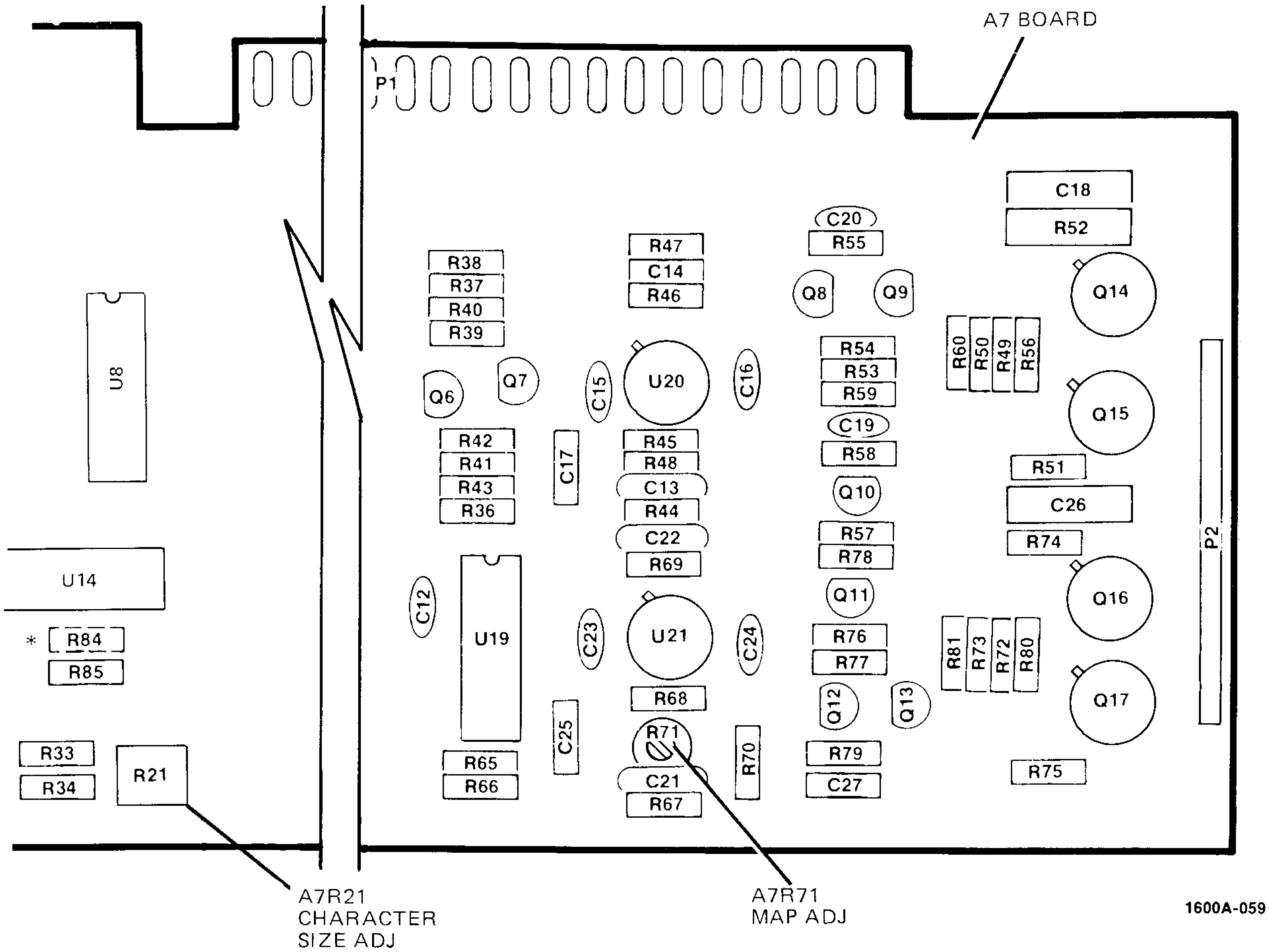


Figure 5-14. Map and Character Size Adjustment

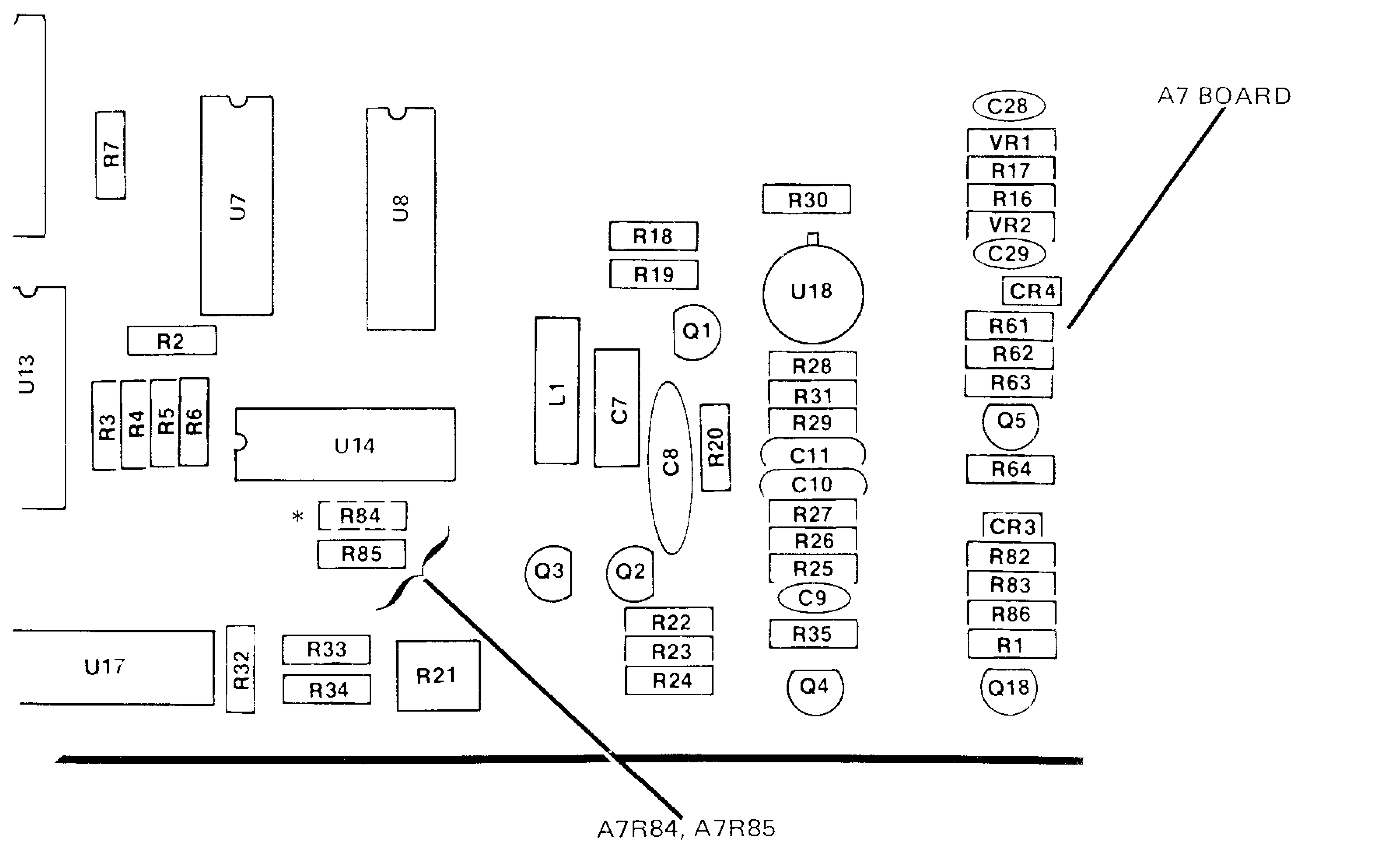


Figure 5-15. 32-Bit Word Modification Location

PERFORMANCE CHECK RECORD

MODEL 1600A

Instrument Serial Number ______________ Date ______________

Check	Specification	Measured
INITIAL OPERATIONAL CHECK DISPLAY	16 Bits 16 Words all ones	
REPETITION RATE	0 to 20 MHz	______
INPUT RC		
Input Resistance	40 kΩ ±3 kΩ	______
Shunt Capacitance	≤14 pF	______
INPUT BIAS CURRENT		
Clock-& Data-Probe Inputs	≤30 μA	______
INPUT THRESHOLD/SWING	.5 V +5% of THLD	
VAR MEAS/SET Swing	≥ +10 Vdc	______
	≤—10 Vdc	______
0 V Threshold	Valid Data	______
+10 V Threshold	Valid Data	______
—10 V Threshold	Valid Data	______
—15 V Peak	Valid Data	______
+15 V Peak	Valid Data	______
MINIMUM CLOCK PULSE WIDTH		
Applied pulses >20 ns	20 ns min	______
MINIMUM DATA PULSE WIDTH		
Applied pulse >25 ns	25 ns min	______
SETUP and HOLD TIME		
Setup Time	20 ns min	______
Hold Time	0 ns min	______

PERFORMANCE CHECK RECORD (Cont'd)

MODEL 1600A

Instrument Serial Number ____________ Date ____________

Check	Specification	Measured
TRIGGER ARM INPUT		
Input Impedance	50 Ω ±2 Ω	______
Levels		
HI	>2 V, <5 V	______
LO	>0 V, <0.4 V	______
Arming Condition	<45 ns	______
	>75 ns	______
DISPLAY TIME		
Display Time CCW	<200 ms	______
Display Time CW	>5 sec	______
PATTERN TRIGGER and DELAY TRIGGER OUTPUTS	into 50 Ω	______
Pattern Trigger Output	2 V < HI > 5 V pk	______
	0 V < LO >.4 V pk	______
Delay Trigger Output	2 V < HI > 5 V pk	______
	0 V < LO >.4 V pk	______
WIDTH	≈25 ns	______
	Synchronous	______

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering replacement parts. The abbreviations used in the parts list are described in table 6-1. Table 6-2 lists the parts in alphanumeric order by reference designation and includes the manufacturer and manufacturer's part number. Table 6-3 contains the list of manufacturers' codes.

6-3. ORDERING INFORMATION.

6-4. To obtain replacement parts from Hewlett-Packard, address order or inquiry to the nearest Hewlett-Packard Sales/Service Office and supply the following information:

a. Instrument model and serial number.

b. HP part number of item(s).

c. Quantity of part(s) desired.

d. Reference designation of part(s).

6-5. To order a part not listed in the table, provide the following information:

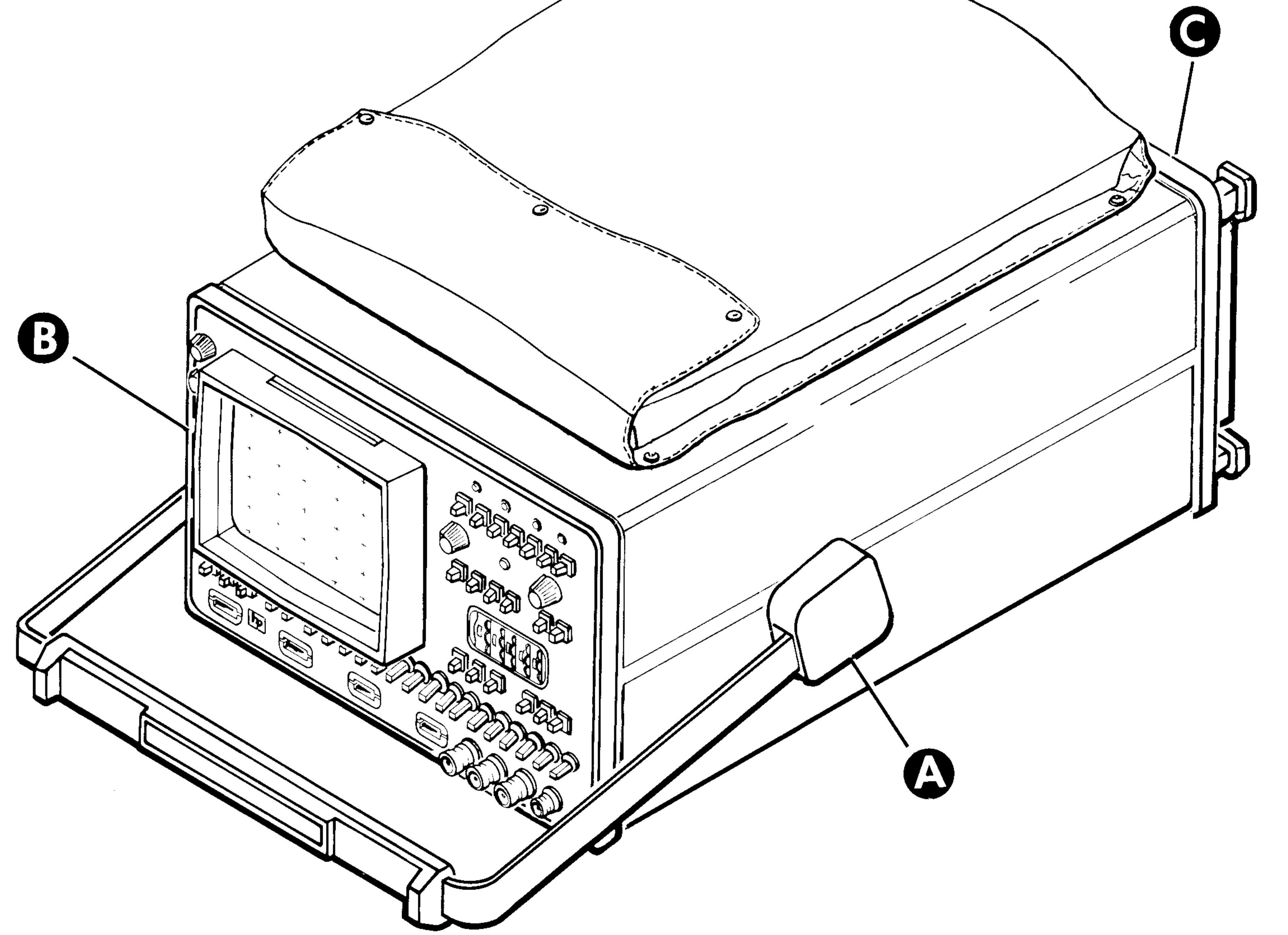
a. Instrument model and serial number.

b. Description of the part, including function and location in the instrument.

c. Quantity desired.

Table 6-1. Abbreviations for Replaceable Parts List

A	AMPERE(S)	H	HENRY(IES)	NPN	NEGATIVE-POSITIVE-	RWV	REVERSE WORKING
ASSY	ASSEMBLY	HG	MERCURY		NEGATIVE		VOLTAGE
		HP	HEWLETT-PACKARD	NSR	NOT SEPARATELY		
BD	BOARD(S)	HZ	HERTZ		REPLACEABLE	S-B	SLOW-BLOW
BH	BINDER HEAD					SCR	SILICON CONTROLLED
BP	BANDPASS	IF	INTERMEDIATE FREQ.				RECTIFIER
		IMPG	IMPREGNATED	OBD	ORDER BY	SE	SELENIUM
C	CENTI (10^{-2})	INCD	INCANDESCENT		DESCRIPTION	SEC	SECOND(S)
CAR	CARBON	INCL	INCLUDE(S)	OH	OVAL HEAD	SECT	SECTION(S)
CCW	COUNTERCLOCKWISE	INS	INSULATION(ED)	OX	OXIDE	SI	SILICON
CER	CERAMIC	INT	INTERNAL			SIL	SILVER
CMO	CABINET MOUNT ONLY			P	PEAK	SL	SLIDE
COAX	COAXIAL	K	KILO (10^3)	PC	PRINTED (ETCHED)	SP	SINGLE POLE
COEF	COEFFICIENT	KG	KILOGRAM		CIRCUIT(S)	SPL	SPECIAL
COMP	COMPOSITION			PF	PICOFARADS	ST	SINGLE THROW
CONN	CONNECTOR(S)	LB	POUND(S)	PHL	PHILLIPS	STD	STANDARD
CRT	CATHODE-RAY TUBE	LH	LEFT HAND	PIV	PEAK INVERSE		
CW	CLOCKWISE	LIN	LINEAR TAPER		VOLTAGE(S)	TA	TANTALUM
		LOG	LOGARITHMIC TAPER	PNP	POSITIVE-NEGATIVE-	TD	TIME DELAY
D	DECI (10^{-1})	LPF	LOW-PASS FILTER(S)		POSITIVE	TFL	TEFLON
DEPC	DEPOSITED CARBON	LVR	LEVER	P/O	PART OF	TGL	TOGGLE
DP	DOUBLE POLE			PORC	PORCELAIN	THYR	THYRISTOR
DT	DOUBLE THROW	M	MILLI (10^{-3})	POS	POSITION(S)	TI	TITANIUM
		MEG	MEGA (10^6)	POT	POTENTIOMETER(S)	TNLDIO	TUNNEL DIODE(S)
ELECT	ELECTROLYTIC	MET FILM	METAL FILM	P-P	PEAK-TO-PEAK	TOL	TOLERANCE
ENCAP	ENCAPSULATED	MET OX	METAL OXIDE	PRGM	PROGRAM	TRIM	TRIMMER
EXT	EXTERNAL	MFR	MANUFACTURER	PS	POLYSTYRENE		
		MINAT	MINIATURE	PWV	PEAK WORKING	U	MICRO (10^{-6})
F	FARAD(S)	MOM	MOMENTARY		VOLTAGE		
FET	FIELD-EFFECT	MTG	MOUNTING			V	VOLTS
	TRANSISTOR(S)	MY	MYLAR	RECT	RECTIFIER(S)	VAR	VARIABLE
FH	FLAT HEAD			RF	RADIO FREQUENCY	VDCW	DC WORKING VOLT(S)
FIL H	FILLISTER HEAD	N	NANO (10^{-9})	RFI	RADIO FREQUENCY		
FXD	FIXED	N/C	NORMALLY CLOSED		INTERFERENCE	W	WATT(S)
		NE	NEON	RH	ROUND HEAD	W/	WITH
G	GIGA (10^9)	N/O	NORMALLY OPEN		OR	WIV	WORKING INVERSE
GE	GERMANIUM	NOP	NEGATIVE POSITIVE		RIGHT HAND		VOLTAGE
GL	GLASS		ZERO (ZERO TEMPER-	RMO	RACK MOUNT ONLY	W/O	WITHOUT
GRD	GROUNDED		ATURE COEFFICIENT)	RMS	ROOT MEAN SQUARE	WW	WIREWOUND



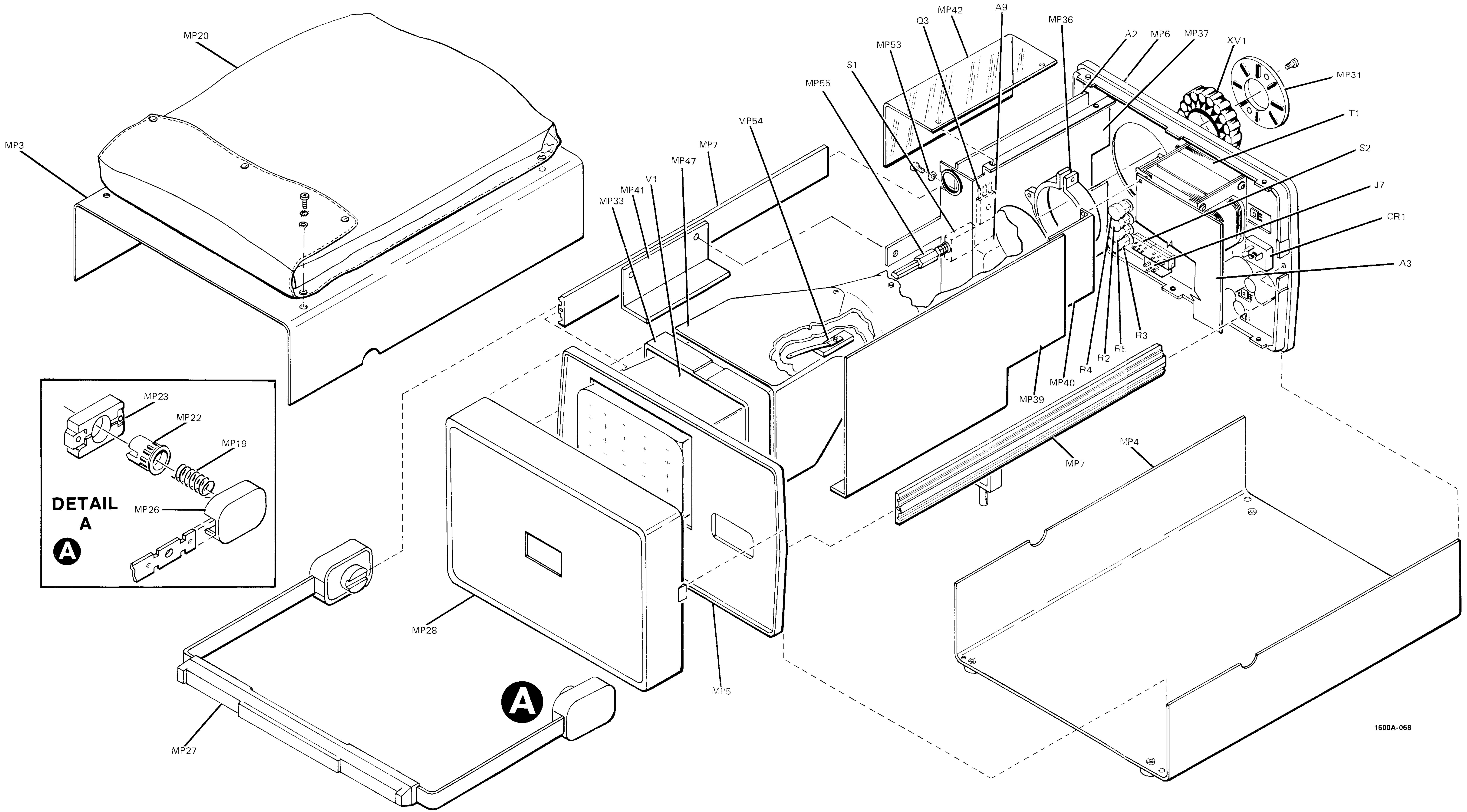


Figure 6-1.
Illustrated Parts Breakdown (Sheet 1 of 2)

Figure 6-1. Illustrated Parts Breakdown (Sheet 2 of 2)

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1	01600-66501		BOARD ASSY, DATA ACQUISITION	28480	01600-66501
A2	01600-66502		BOARD ASSY, HIGH VOLTAGE	28480	01600-66502
A3	01600-66503		BOARD ASSY, LOW VOLTAGE	28480	01600-66503
A4	01600-66504		BOARD ASSY, UPPER SWITCH	28480	01600-66504
A5	01600-66505		BOARD ASSY, LOWER SWITCH	28480	01600-66505
A6	01600-66506		BOARD ASSY, TRIGGER SWITCH	28480	01600-66506
A7	01600-66507		BOARD ASSY, ANALOG	28480	01600-66507
A8	01600-66508		BOARD ASSY, DIGITAL	28480	01600-66508
A9	0960-0430		ASSY, HIGH VOLTAGE MULTIPLIER	28480	0960-0430
A10	01600-66510		BOARD ASSY, DIGITAL SWITCH	28480	01600-66510
CR1	1901-0525	1	DIODE; MULT: FULL WAVE BRIDGE RECTIFIER	28480	1901-0525
DS1	1990-0486	5	LED-VISIBLE	28480	1990-0486
DS2	1990-0486		LED-VISIBLE	28480	1990-0486
DS3	1990-0486		LED-VISIBLE	28480	1990-0486
DS4	1990-0486		LED-VISIBLE	28480	1990-0486
DS5	1990-0486		LED-VISIBLE	28480	1990-0486
DS6	2140-0352	1	LAMP; INCAND; BULB T-1; 18V	71744	CM 6838
E1	0340-0511	5	INSULATOR, TRANSISTOR	13103	43-77-2
E2	6040-0239	1	GREASE; SILICONE COMPOUND	05820	120-5GM
F1	2110-0007		FUSE 1A 250V SLO-BLO 1.25X.25	71400	MDL-1
J1	1250-0118	4	CONNECTOR-RF BNC FEM SGL HOLE FR	95949	31-2221-1022
J2	1250-0118		CONNECTOR-RF BNC FEM SGL HOLE FR	95949	31-2221-1022
J3	1250-0118		CONNECTOR-RF BNC FEM SGL HOLE FR	95949	31-2221-1022
J4	1250-0659	1		28480	1250-0659
J5	1250-0118		CONNECTOR-RF BNC FEM SGL HOLE FR	95949	31-2221-1022
J6	1251-0085	1	CONNECTOR, 36-CONT, FEM, MICRO RIBBON	71785	57-40360-375
J7	1251-2357	1	CONNECTOR, AC POWER, HP-9 MALE FLANGE	28480	1251-2357
L1	5060-0435	1	COIL:ALIGNMENT Z AXIS	28480	5060-0435
MP1	01600-00202	1	PANEL, FRONT	28480	01600-00202
MP2	01600-00204	1	PANEL, REAR	28480	01600-00204
MP3	01600-04101	1	COVER, TOP	28480	01600-04101
MP4	01600-04102	1	COVER, BOTTOM	28480	01600-04102
MP5	01600-20501	1	FRAME, FRONT	28480	01600-20501
MP6	01600-20502	1	FRAME, REAR	28480	01600-20502
MP7	01600-23701	2	RAIL, SIDE	28480	01600-23701
MP8	0370-2626	23	BEZEL, PB GRAY	28480	0370-2626
MP9	0370-2790	1	PUSHBUTTON, YEL-ORN	28480	0370-2790
MP10	0370-0671	8	PUSHBUTTON, LEG BLU	28480	0370-0671
MP11	0370-0684	4	PUSHBUTTON, H GOLD	28480	0370-0684
MP12	0370-0603	3	PUSHBUTTON:SQUARE, MINT GRAY	28480	0370-0603
MP13	0370-2630	6	PUSHBUTTON, SQUARE, WIL GRN	28480	0370-2630
MP14	0370-1099	2	KNOB, BASE, PTR, .5 IN, JGK, SGI DECAL	28480	0370-1099
MP15	0370-1005	2	KNOB; BASE; PTR; .375 IN; JGK; SGI	28480	0370-1005
MP16	1400-0084	1	FUSEHOLDER-EXTR POST 15A 250V UL	28480	1400-0084
MP17			NOT ASSIGNED		
MP18	1450-0404	6	LIGHT-IND LENS CAP CLR TL LENS	28480	1450-0404
MP19	1460-0604	2	SPRING CPRSN-CYL .95-OD 1.185-LG MUW	28480	1460-0604
MP20	1540-0292	1	CASE-ACCESS PVC 10.5-LG 1.5-WD 13.5-DP	28480	1540-0292
MP21	5020-0476	1	BEZEL:CRT	28480	5020-0476
MP22	5020-8733	2	GEAR, HUB HANDLE	28480	5020-8733
MP23	5020-8734	2	RING, HANDLE	28480	5020-8734
MP24	5020-8758	1	CRT SHIELD, SAFETY	28480	5020-8758
MP25	5040-0508	1	SHIELD:LIGHT,OLIVE BLACK(STANDARD)	28480	5040-0508
MP26	5040-0511	2	CAP, TRIM	28480	5040-0511
MP27	5040-0515	1	ASSY, HANDLE	28480	5040-0515
MP28	5040-0516	1	COVER, PANEL	28480	5040-0516
MP29	5040-5861	4	FOOT:BASE	28480	5040-5861
MP30	5040-5862	4	FOOT:REAR,CAP	28480	5040-5862
MP31	1200-0408	1	COVER, SOCKET	28480	1200-0408
MP32	5080-9694	1	FUSE PACKAGE-230 VOLT	28480	5080-9694
MP33	00140-24712	1	SUPPORT, CRT SHIELD	28480	00140-24712
MP34	00180-01218	1	BRACKET, COIL	28480	00180-01218
MP35	00183-67701	1	BASE, PILOT LIGHT	28480	00183-67701
MP36	01200-44701	1	SUPPORT, CRT	28480	01200-44701
MP37	01600-01201	1	BRACKET, HIGH VOLTAGE	28480	01600-01201
MP38	01600-01202	1	BRACKET, TRANSFORMER	28480	01600-01202
MP39	01600-01203	1	BRACKET, DISPLAY	28480	01600-01203
MP40	01600-01204	1	BRACKET, LOW VOLTAGE	28480	01600-01204
MP41	01600-01205	1	BRACKET, LEFT	28480	01600-01205
MP42	01600-04103	1	COVER, HV	28480	01600-04103
MP43	01600-04104	1	COVER, SOCKET	28480	01600-04104
MP44*	01600-04701	1	SPACER, TRANS (FACTORY SELECTED PART. NOT INSTALLED IN ALL INSTRUMENTS).	28480	01600-04701
MP45	01600-20503	1	HEAT SINK, REAR	28480	01600-20503

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
MP46	01600-23201	1	EXTENSION, POWER SWITCH	28480	01600-23201
MP47	01600-60601	1	SHIELD ASSY, CRT	28480	01600-60601
MP48	0370-2862	1	PUSHBUTTON, CORP WHITE	28480	0370-2862
MP49	1490-0968	5	BUSHING; POT	28480	1490-0968
MP50	5040-0421	1	INSULATOR COVER, POT	28480	5040-0421
MP51	0590-0043	5	NUT, HEX, DBL CHAM	28480	0590-0043
MP52	3050-0791	5	WASHER, SHOULDER	28480	3050-0791
MP53	2190-0910	3	WASHER, SPRING	04713	04A52200F01
MP54	01758-0091	1	SPRING, CRT GND	28480	01758-0091
MP55	01830-23201	1	COUPLER, SWITCH	28480	01830-23201
Q1	1854-0433	2	TRANSISTOR NPN SI PD=90W FT=2MHZ	28480	1854-0433
Q2	1854-0433		TRANSISTOR NPN SI PD=90W FT=2MHZ	28480	1854-0433
R1	2100-2635	1	RESISTOR-VAR 50K 20% CC	01121	TYPE W
R2	2100-2066	2	RESISTOR-VAR 2K 20% CC	01121	TYPE W
R3	2100-2066		RESISTOR-VAR 2K 20% CC	01121	TYPE W
R4	2100-2590	2	RESISTOR-VAR 10K 10% CC	12697	SERIES 63M
R5	2100-2590		RESISTOR-VAR 10K 10% CC	12697	SERIES 63M
R6	2100-2492	1	RESISTOR-VAR 5K 20% CC	71450	SERIES 300
R7	2100-3135	1	RESISTOR-VAR 5K 20% CC	28480	2100-3135
R8	2100-0665	1	RESISTOR-VAR 5M 20% CC	28480	2100-0665
R9	2100-3460	1	RESISTOR-VAR 500K 10% CC	01121	WA1N040S504AZ
R10	0684-4711	1	RESISTOR, 470 OHM 10% .25W CC TUBULAR	01121	CB4711
S1	3101-0555	1	SWITCH-PB DPDT ALTNG 4A 250VAC	28480	3101-0555
S2	3101-0625	1	SWITCH-SL 2-DPDT-NS STD 3A 125VAC SLDR	82389	47206-LFF
T1	9100-3420	1	TRANSFORMER, POWER	28480	9100-3420
TP1	0360-1646	1	TERMINAL-STUD SPCL PRESS MTG	28480	0360-1646
U1	1826-0221	1	IC MC 7912CP	04713	MC7912CP
U2	1826-0147	1	IC REGULATOR	07263	7812UC
V1	5083-2381	1	CRT, ELECTRON TUBE	28480	5083-2381
W1	01600-61604	1	CABLE, UPPER SWITCH	28480	01600-61604
W2	01600-61606	1	CABLE, LOWER SWITCH	28480	01600-61606
W3	01600-61603	1	CABLE, SHORT FRONT PANEL	28480	01600-61603
W4	01600-61605	1	CABLE, FRONT PANEL	28480	01600-61605
W5	01600-61615	1	CABLE, INPUT/OUTPUT	28480	01600-61615
W6	01600-61614	1	CABLE, CRT SOCKET	28480	01600-61614
W7	01600-61601	1	CABLE, FOCUS AND INTENSITY	28480	01600-61601
W8	01600-61609	1	CABLE, DISPLAY POWER SUPPLY	28480	01600-61609
W9	01600-61608	1	CABLE, POWER SUPPLY	28480	01600-61608
W10	01600-61607	1	CABLE, HV REGULATOR	28480	01600-61607
W11	01600-61613	1	CABLE, LINE INPUT	28480	01600-61613
W12	01600-61610	1	CABLE, DEFLECTION	28480	01600-61610
W13	8120-1521	1	CABLE; UNSHLD 3-COND 18AWG	28480	8120-1521
W14	01600-61616	1	CABLE, VOLTAGE REGULATOR "A"	28480	01600-61616
W15	01600-61617	1	CABLE, VOLTAGE REGULATOR "B"	28480	01600-61617
W16	01600-61618	1	CABLE, VOLTAGE REGULATOR "C"	28480	01600-61618
XV1	1200-0037	1	SOCKET, CRT	28480	1200-0037

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1	01600-66501	1	BOARD ASSY, DATA ACQUISITION	28480	01600-66501
A1C1	0140-0202	19	CAPACITOR-FXD 15PF +-5% 500WVDC MICA	72136	DM15C150J0500WV1CR
A1C2	0140-0202		CAPACITOR-FXD 15PF +-5% 500WVDC MICA	72136	DM15C150J0500WV1CR
A1C3	0140-0202		CAPACITOR-FXD 15PF +-5% 500WVDC MICA	72136	DM15C150J0500WV1CR
A1C4	0140-0202		CAPACITOR-FXD 15PF +-5% 500WVDC MICA	72136	DM15C150J0500WV1CR
A1C5	0140-0202		CAPACITOR-FXD 15PF +-5% 500WVDC MICA	72136	DM15C150J0500WV1CR
A1C6	0140-0202		CAPACITOR-FXD 15PF +-5% 500WVDC MICA	72136	DM15C150J0500WV1CR
A1C7	0140-0202		CAPACITOR-FXD 15PF +-5% 500WVDC MICA	72136	DM15C150J0500WV1CR
A1C8	0140-0202		CAPACITOR-FXD 15PF +-5% 500WVDC MICA	72136	DM15C150J0500WV1CR
A1C9	0140-0202		CAPACITOR-FXD 15PF +-5% 500WVDC MICA	72136	DM15C150J0500WV1CR
A1C10	0140-0202		CAPACITOR-FXD 15PF +-5% 500WVDC MICA	72136	DM15C150J0500WV1CR
A1C11	0140-0202		CAPACITOR-FXD 15PF +-5% 500WVDC MICA	72136	DM15C150J0500WV1CR
A1C12	0140-0202		CAPACITOR-FXD 15PF +-5% 500WVDC MICA	72136	DM15C150J0500WV1CR
A1C13	0140-0202		CAPACITOR-FXD 15PF +-5% 500WVDC MICA	72136	DM15C150J0500WV1CR
A1C14	0140-0202		CAPACITOR-FXD 15PF +-5% 500WVDC MICA	72136	DM15C150J0500WV1CR
A1C15	0140-0202		CAPACITOR-FXD 15PF +-5% 500WVDC MICA	72136	DM15C150J0500WV1CR
A1C16	0140-0202		CAPACITOR-FXD 15PF +-5% 500WVDC MICA	72136	DM15C150J0500WV1CR
A1C17	0140-0202		CAPACITOR-FXD 15PF +-5% 500WVDC MICA	72136	DM15C150J0500WV1CR
A1C18	0140-0202		CAPACITOR-FXD 15PF +-5% 500WVDC MICA	72136	DM15C150J0500WV1CR
A1C19	0160-0174	9	CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A1C20	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A1C21	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A1C22	0160-3448	5	CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3448
A1C23	0160-3451	35	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C24	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C25	0140-0190	2	CAPACITOR-FXD 39PF +-5% 300WVDC MICA	72136	DM15E390J0300WV1CR
A1C26	0160-2207	3	CAPACITOR-FXD 300PF +-5% 300WVDC MICA	28480	0160-2207
A1C27	0140-0196	1	CAPACITOR-FXD 150PF +-5% 300WVDC MICA	72136	DM15F151J0300WV1CR
A1C28	0160-2204	3	CAPACITOR-FXD 100PF +-5% 300WVDC MICA	28480	0160-2204
A1C29	0140-0202		CAPACITOR-FXD 15PF +-5% 500WVDC MICA	72136	DM15C150J0500WV1CR
A1C30	0140-0190		CAPACITOR-FXD 39PF +-5% 300WVDC MICA	72136	DM15E390J0300WV1CR
A1C31	0160-2201	1	CAPACITOR-FXD 51PF +-5% 300WVDC MICA	28480	0160-2201
A1C32	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C33	0121-0046	3	CAPACITOR; VAR; TRMR; CER; 9/35PF	73899	DV11PS350
A1C34	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C35	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C36			NOT ASSIGNED		
A1C37	0121-0046		CAPACITOR; VAR; TRMR; CER; 9/35PF	73899	DV11PS350
A1C38	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C39	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C40	0160-2198	4	CAPACITOR-FXD 20PF +-5% 300WVDC MICA	28480	0160-2198
A1C41	0121-0046		CAPACITOR; VAR; TRMR; CER; 9/35PF	73899	DV11PS350
A1C42	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C43	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C44	0180-0197	4	CAPACITOR-FXD; 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A1C45	0180-0116	9	CAPACITOR-FXD; 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A1C46	0180-0116		CAPACITOR-FXD; 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A1C47	0180-0197		CAPACITOR-FXD; 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A1C48	0180-0116		CAPACITOR-FXD; 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A1C49	0180-0116		CAPACITOR-FXD; 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A1C50	0180-0116		CAPACITOR-FXD; 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A1C51	0180-0116		CAPACITOR-FXD; 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A1C52	0160-2198		CAPACITOR-FXD 20PF +-5% 300WVDC MICA	28480	0160-2198
A1C53	0160-2198		CAPACITOR-FXD 20PF +-5% 300WVDC MICA	28480	0160-2198
A1C54	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A1C55	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A1C56	0180-0106	2	CAPACITOR-FXD; 60UF+-20% 6VDC TA-SOLID	56289	150D606X0006B2
A1C57	0180-0106		CAPACITOR-FXD; 60UF+-20% 6VDC TA-SOLID	56289	150D606X0006B2
A1C58	0180-0228	5	CAPACITOR-FXD; 22UF+-10% 15VDC TA-SOLID	56289	150D226X9015B2
A1C59	0180-0228		CAPACITOR-FXD; 22UF+-10% 15VDC TA-SOLID	56289	150D226X9015B2
A1C60	0160-2198		CAPACITOR-FXD 20PF +-5% 300WVDC MICA	28480	0160-2198
A1C61	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C62	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C63	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C64	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C65	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C66	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C67	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C68	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C69	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C70	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1C71	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C72	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C73	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C74	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C75	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C76	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C77	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C78	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1CR1	1901-0040	14	DIODE-SWITCHING 2NS 30V 50MA	28480	1901-0040
A1CR2	1901-0535	2	DIODE-SCHOTTKY	28480	1901-0535
A1CR3	1901-0535		DIODE-SCHOTTKY	28480	1901-0535
A1CR4	1901-0040		DIODE-SWITCHING 2NS 30V 50MA	28480	1901-0040
A1CR5	1901-0040		DIODE-SWITCHING 2NS 30V 50MA	28480	1901-0040
A1J1	1251-0699	4	CONNECTOR	28480	1251-0699
A1J2	1251-0699		CONNECTOR	28480	1251-0699
A1J3	1251-0699		CONNECTOR	28480	1251-0699
A1J4	1251-0699		CONNECTOR	28480	1251-0699
A1J5	1200-0441	5	SOCKET, ELEC, IC 14-CONT DIP SLDR TERM	24995	583527-1
A1J6	1200-0441		SOCKET, ELEC, IC 14-CONT DIP SLDR TERM	24995	583527-1
A1J7	1200-0441		SOCKET, ELEC, IC 14-CONT DIP SLDR TERM	24995	583527-1
A1J8	1200-0441		SOCKET, ELEC, IC 14-CONT DIP SLDR TERM	24995	583527-1
A1J9	1200-0441		SOCKET, ELEC, IC 14-CONT DIP SLDR TERM	24995	583527-1
A1L1	9100-2259	20	COIL-FXD MOLDED RF CHOKE 1.5UH 10%	24226	10/151
A1L2	9100-2259		COIL-FXD MOLDED RF CHOKE 1.5UH 10%	24226	10/151
A1L3	9100-2259		COIL-FXD MOLDED RF CHOKE 1.5UH 10%	24226	10/151
A1L4	9100-2259		COIL-FXD MOLDED RF CHOKE 1.5UH 10%	24226	10/151
A1L5	9100-2259		COIL-FXD MOLDED RF CHOKE 1.5UH 10%	24226	10/151
A1L6	9100-2259		COIL-FXD MOLDED RF CHOKE 1.5UH 10%	24226	10/151
A1L7	9100-2259		COIL-FXD MOLDED RF CHOKE 1.5UH 10%	24226	10/151
A1L8	9100-2259		COIL-FXD MOLDED RF CHOKE 1.5UH 10%	24226	10/151
A1L9	9100-2259		COIL-FXD MOLDED RF CHOKE 1.5UH 10%	24226	10/151
A1L10	9100-2259		COIL-FXD MOLDED RF CHOKE 1.5UH 10%	24226	10/151
A1L11	9100-2259		COIL-FXD MOLDED RF CHOKE 1.5UH 10%	24226	10/151
A1L12	9100-2259		COIL-FXD MOLDED RF CHOKE 1.5UH 10%	24226	10/151
A1L13	9100-2259		COIL-FXD MOLDED RF CHOKE 1.5UH 10%	24226	10/151
A1L14	9100-2259		COIL-FXD MOLDED RF CHOKE 1.5UH 10%	24226	10/151
A1L15	9100-2259		COIL-FXD MOLDED RF CHOKE 1.5UH 10%	24226	10/151
A1L16	9100-2259		COIL-FXD MOLDED RF CHOKE 1.5UH 10%	24226	10/151
A1L17	9100-2259		COIL-FXD MOLDED RF CHOKE 1.5UH 10%	24226	10/151
A1L18	9100-2259		COIL-FXD MOLDED RF CHOKE 1.5UH 10%	24226	10/151
A1L19	9100-2259		COIL-FXD MOLDED RF CHOKE 1.5UH 10%	24226	10/151
A1L20	9100-2255	2	COIL-FXD MOLDED RF CHOKE 470MH 10%	24226	10/470
A1L21	9100-2255		COIL-FXD MOLDED RF CHOKE 470MH 10%	24226	10/470
A1L22	9100-2259		COIL-FXD MOLDED RF CHOKE 1.5UH 10%	24226	10/151
A1MP1	5040-7478	4	HOUSING, TOP	28480	5040-7478
A1MP2	5040-7479	4	HOUSING, BOTTOM	28480	5040-7479
A1Q1	1854-0071	12	TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A1R1	0757-0420	19	RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A1R2	0757-0420		RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A1R3	0757-0420		RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A1R4	0757-0420		RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A1R5	0757-0420		RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A1R6	0757-0420		RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A1R7	0757-0420		RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A1R8	0757-0420		RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A1R9	0757-0420		RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A1R10	0757-0420		RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A1R11	0757-0420		RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A1R12	0757-0420		RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A1R13	0757-0420		RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A1R14	0757-0420		RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A1R15	0757-0420		RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A1R16	0757-0420		RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A1R17	0757-0420		RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A1R18	0757-0420		RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A1R19	0684-6821	4	RESISTOR 6.8K 10% .25W FC TC=-400/+700	01121	CB6821
A1R20	0698-0084	3	RESISTOR 2.15K 1% .125W F TC=0+-100	16299	C4-1/8-T0-2151-F
A1R21	0757-0438	5	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1R22	0757-0472	2	RESISTOR 200K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2003-F
A1R23	0757-0465	6	RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A1R24	0757-0463	1	RESISTOR 82.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8252-F
A1R25	0683-0275	1	RESISTOR 2.7 5% .25W FC TC=-400/+500	01121	CB27G5

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1R26	0684-6821		RESISTOR 6.8K 10% .25W FC TC=-400/+700	01121	CB6821
A1R27	0684-6821		RESISTOR 6.8K 10% .25W FC TC=-400/+700	01121	CB6821
A1R28	0757-0407	4	RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A1R29	0757-0401	2	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A1R30	0684-3911	4	RESISTOR 390 10% .25W FC TC=-400/+600	01121	CB3911
A1R31	0684-3911		RESISTOR 390 10% .25W FC TC=-400/+600	01121	CB3911
A1R32	0684-3911		RESISTOR 390 10% .25W FC TC=-400/+600	01121	CB3911
A1R33	0757-0280	13	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R34	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R35	0684-3911		RESISTOR 390 10% .25W FC TC=-400/+600	01121	CB3911
A1R36	0757-0288	5	RESISTOR 9.09K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-9091-F
A1R37	0757-0288		RESISTOR 9.09K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-9091-F
A1R38	0757-0288		RESISTOR 9.09K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-9091-F
A1R39	0683-5105	2	RESISTOR 51 5% .25W FC TC=-400/+500	01121	CB5105
A1R40	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R41	0698-3447	2	RESISTOR 422 1% .125W F TC=0+-100	16299	C4-1/8-T0-422R-F
A1R42	0757-0418	1	RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-T0-619R-F
A1R43	0757-0416	6	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A1R44	0698-3150	1	RESISTOR 2.37K 1% .125W F TC=0+-100	16299	C4-1/8-T0-2371-F
A1R45	0698-3122	1	RESISTOR 412 1% .125W F TC=0+-100	03888	PME55-1/8-T0-4120-F
A1R46	0757-0416		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A1R47	0757-0442	4	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R48	0757-0416		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A1R49	2100-1783	1	RESISTOR-VAR TRMR 500 OHM 10% C TOP ADJ	84048	170-501
A1R50	0698-3444	2	RESISTOR 316 1% .125W F TC=0+-100	16299	C4-1/8-T0-316R-F
A1R51	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R52	0757-0442		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R53	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R54	0698-4130	1	RESISTOR 39 5% .125W CC TC=0+588	01121	BB3905
A1R55	0698-3444		RESISTOR 316 1% .125W F TC=0+-100	16299	C4-1/8-T0-316R-F
A1R56	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R57	0757-0442		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R58	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R59	0698-3379	1	RESISTOR 68 5% .125W CC TC=0+588	01121	BB6805
A1R60	0684-2201	2	RESISTOR 22 10% .25W FC TC=-400/+500	01121	CB2201
A1R61	0684-4721	4	RESISTOR 4.7K 10% .25W FC TC=-400/+700	01121	CB4721
A1R62	0757-0434	2	RESISTOR 3.65K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3651-F
A1R63	0757-0426	1	RESISTOR 1.3K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1301-F
A1R64	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R65	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R66	0757-0457	7	RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A1R67	0757-0457		RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A1R68	0757-0457		RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A1R69	0757-0457		RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A1R70	0757-0457		RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A1R71	0684-2201		RESISTOR 22 10% .25W FC TC=-400/+500	01121	CB2201
A1R72	0684-6821		RESISTOR 6.8K 10% .25W FC TC=-400/+700	01121	CB6821
A1R73	0757-0407		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A1R74	0757-0401		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A1R75	0698-0084		RESISTOR 2.15K 1% .125W F TC=0+-100	16299	C4-1/8-T0-2151-F
A1R76	0698-3151	1	RESISTOR 2.87K 1% .125W F TC=0+-100	16299	C4-1/8-T0-2871-F
A1R77	0757-0457		RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A1S1	3101-1946	1	SWITCH	28480	3101-1946
A1TP1	0360-0535	2	TERMINAL, TEST POINT	4G819	OBD
A1TP2	0360-0535		TERMINAL, TEST POINT	4G819	OBD
A1TP3	1251-2229	2	CONNECTOR; 1-CONT SKT .033 DIA	00779	1-331677-3
A1TP4	1251-2229		CONNECTOR; 1-CONT SKT .033 DIA	00779	1-331677-3
A1U1	1820-0693	9	IC SN74S 74 N	01295	SN74S74N
A1U2	1820-0693		IC SN74S 74 N	01295	SN74S74N
A1U3	1820-0693		IC SN74S 74 N	01295	SN74S74N
A1U4	1820-0693		IC SN74S 74 N	01295	SN74S74N
A1U5	1820-0693		IC SN74S 74 N	01295	SN74S74N
A1U6	1820-0693		IC SN74S 74 N	01295	SN74S74N
A1U7	1820-0693		IC SN74S 74 N	01295	SN74S74N
A1U8	1820-0693		IC SN74S 74 N	01295	SN74S74N
A1U9	1820-0693		IC SN74S 74 N	01295	SN74S74N
A1U10	1820-0692	9	IC SN74S 65 N	01295	SN74S65N
A1U11	1820-0692		IC SN74S 65 N	01295	SN74S65N
A1U12	1820-0692		IC SN74S 65 N	01295	SN74S65N
A1U13	1820-0692		IC SN74S 65 N	01295	SN74S65N
A1U14	1820-0692		IC SN74S 65 N	01295	SN74S65N
A1U15	1820-0692		IC SN74S 65 N	01295	SN74S65N
A1U16	1820-0692		IC SN74S 65 N	01295	SN74S65N
A1U17	1820-0692		IC SN74S 65 N	01295	SN74S65N
A1U18	1820-0692		IC SN74S 65 N	01295	SN74S65N
A1U19	1820-1146	6	IC CD4050AE	02735	CD4050AE
A1U20	1820-1146		IC CD4050AE	02735	CD4050AE

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1U21	1820-1146		IC CD4050AE	02735	CD4050AE
A1U22	1820-1146		IC CD4050AE	02735	CD4050AE
A1U23	1820-1146		IC CD4050AE	02735	CD4050AE
A1U24	1820-1146		IC CD4050AE	02735	CD4050AE
A1U25	1820-0687	1	IC SN74S 15 N	01295	SN74S15N
A1U26	1820-0691	11	IC SN74S 64 N	01295	SN74S64N
A1U27	1820-1201	1	IC SN74LS 08 N	01295	SN74LS08N
A1U28	1820-1106	4	IC MEMORY	34649	3101A
A1U29	1820-1139	3	IC:TTL, HEX INVERTER	28480	1820-1139
A1U30	1820-1106		IC MEMORY	34649	3101A
A1U31	1820-1139		IC:TTL, HEX INVERTER	28480	1820-1139
A1U32	1820-1106		IC MEMORY	34649	3101A
A1U33	1820-1139		IC:TTL, HEX INVERTER	28480	1820-1139
A1U34	1820-1106		IC MEMORY	34649	3101A
A1U35	1820-1365	4	IC MM74C157N	27014	MM74C157N
A1U36	1820-1365		IC MM74C157N	27014	MM74C157N
A1U37	1820-1365		IC MM74C157N	27014	MM74C157N
A1U38	1820-1365		IC MM74C157N	27014	MM74C157N
A1U39	1820-0640	1	IC SN74 150 N	01295	SN74150N
A1U40	1820-1340	1	IC MC14585CP	04713	MC14585CP
A1U41	1820-0681	3	IC SN74S 00 N	01295	SN74S00N
A1U42	1820-1158	1	IC SN74S 51 N	01295	SN74S51N
A1U43	1820-0629	5	IC SN74S 112 N	01295	SN74S112N
A1U44	1821-0002	2	IC CA3045	02735	CA3045
A1U45	1821-0002		IC CA3045	02735	CA3045
A1U46	1820-0629		IC SN74S 112 N	01295	SN74S112N
A1U47	1820-0661	1	IC SN74 32 N	01295	SN7432N
A1U48	1820-0203	1	IC AMPLIFIER	28480	1820-0203
A1U49	1820-0584	6	IC DM74L 02N	27014	DM74L02N
A1U50	1810-0183	18	NETWORK-RES 9-PIN SIP .1-PIN-SPCG	28480	1810-0183
A1U51	1820-0515	6	IC MULTIVIBRATOR	07263	9602DC
A1U52	1820-0515		IC MULTIVIBRATOR	07263	9602DC
A1U53	1820-0515		IC MULTIVIBRATOR	07263	9602DC
A1U54	1820-0691		IC SN74S 64 N	01295	SN74S64N
A1U55	1820-0691		IC SN74S 64 N	01295	SN74S64N
A1U56	1820-0691		IC SN74S 64 N	01295	SN74S64N
A1U57	1820-0691		IC SN74S 64 N	01295	SN74S64N
A1U58	1820-0910	3	IC SN74LS 83 N	01295	SN74LS83N
A1U59	1820-0910		IC SN74LS 83 N	01295	SN74LS83N
A1U60	1820-1475	2	IC COUNTER	07263	93S16DC
A1U61	1820-0515		IC MULTIVIBRATOR	07263	9602DC
A1U62	1820-0697	2	IC SN74S 140 N	01295	SN74S140N
A1U63	1820-0681		IC SN74S 00 N	01295	SN74S00N
A1U64	1820-0691		IC SN74S 64 N	01295	SN74S64N
A1U65	1820-0691		IC SN74S 64 N	01295	SN74S64N
A1U66	1820-0069	1	IC SN74 20 N	01295	SN7420N
A1U67	1820-1372	3	IC FLIP-FLOP	07263	9S109DC
A1U68	1820-0515		IC MULTIVIBRATOR	07263	9602DC
A1U69	1820-0685	1	IC SN74S 10 N	01295	SN74S10N
A1U70	1820-1373	1	IC COUNTER	07263	93S10DC
A1U71	1820-1372		IC FLIP-FLOP	07263	9S109DC
A1U72	1820-0063	2	IC SN74 51 N	01295	SN7451N
A1U73	1820-0669	4	IC COUNTER	07263	93L10DC
A1U74	1820-0669		IC COUNTER	07263	93L10DC
A1U75	1820-0669		IC COUNTER	07263	93L10DC
A1U76	1820-0669		IC COUNTER	07263	93L10DC
A1U77	1820-0691		IC SN74S 64 N	01295	SN74S64N
A1U78	1820-0070	1	IC SN74 30 N	01295	SN7430N
A1U79	1820-0910		IC SN74LS 83 N	01295	SN74LS83N
A1U80	1820-0589	1	IC DM74L 30N	27014	DM74L30N
A1U81	1820-0382	2	IC SN74H 55 N	01295	SN74H55N
A1U82	1820-0588	1	IC DM74L 20N	27014	DM74L20N
A1U83	1820-0710	3	IC MULTIPLEXER	07263	93L22DC
A1U84	1820-1372		IC FLIP-FLOP	07263	9S109DC
A1U85	1820-0583	5	IC DM74L 00N	27014	DM74L00N
A1U86	1820-0904	3	IC COMPARATOR	07263	93L24DC
A1U87	1820-0382		IC SN74H 55 N	01295	SN74H55N
A1U88	1820-0681		IC SN74S 00 N	01295	SN74S00N
A1U89	1820-0629		IC SN74S 112 N	01295	SN74S112N
A1U90	1820-0697		IC SN74S 140 N	01295	SN74S140N
A1U91	1820-0691		IC SN74S 64 N	01295	SN74S64N
A1U92	1820-0691		IC SN74S 64 N	01295	SN74S64N
A1U93	1820-0629		IC SN74S 112 N	01295	SN74S112N
A1U94	1820-0629		IC SN74S 112 N	01295	SN74S112N
A1U95	1820-1475		IC COUNTER	07263	93S16DC

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1U96	1820-0683	1	IC SN74S 11 N	01295	SN74S11N
A1U97	1820-0904		IC COMPARATOR	07263	93L24DC
A1U98	1820-0683	1	IC SN74S 04 N	01295	SN74S04N
A1U99	1810-0183		NETWORK-RES 9-PIN SIP .1-PIN-SPCG	28480	1810-0183
A1U100	1810-0183		NETWORK-RES 9-PIN SIP .1-PIN-SPCG	28480	1810-0183
A1U101	1810-0183		NETWORK-RES 9-PIN SIP .1-PIN-SPCG	28480	1810-0183
A1U102	1810-0183		NETWORK-RES 9-PIN SIP .1-PIN-SPCG	28480	1810-0183
A1U103	1810-0183		NETWORK-RES 9-PIN SIP .1-PIN-SPCG	28480	1810-0183
A1U104	1810-0183		NETWORK-RES 9-PIN SIP .1-PIN-SPCG	28480	1810-0183
A1U105	1810-0183		NETWORK-RES 9-PIN SIP .1-PIN-SPCG	28480	1810-0183
A1U106	1810-0183		NETWORK-RES 9-PIN SIP .1-PIN-SPCG	28480	1810-0183
A1U107	1810-0183		NETWORK-RES 9-PIN SIP .1-PIN-SPCG	28480	1810-0183
A1U108	1810-0183		NETWORK-RES 9-PIN SIP .1-PIN-SPCG	28480	1810-0183
A1U109	1810-0183		NETWORK-RES 9-PIN SIP .1-PIN-SPCG	28480	1810-0183
A1U110	1810-0183		NETWORK-RES 9-PIN SIP .1-PIN-SPCG	28480	1810-0183
A1XA8P1	1251-2035	2	CONNECTOR; PC EDGE; 15-CONT; DIP SOLDER	71785	252-15-30-300
A1XA8P2	1251-2035		CONNECTOR; PC EDGE; 15-CONT; DIP SOLDER	71785	252-15-30-300
A2	01600-66502	1	BOARD ASSY, HIGH VOLTAGE	28480	01600-66502
A2C1	0180-0197		CAPACITOR-FXD; 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A2C2	0180-0197		CAPACITOR-FXD; 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A2C3	0160-0168	2	CAPACITOR-FXD .1UF +-10% 200WVDC POLYE	56289	292P10492
A2C4	0170-0040	2	CAPACITOR-FXD .047UF +-10% 200WVDC POLYE	56289	292P47392
A2C5	0180-1794	1	CAPACITOR-FXD; 22UF+-10% 35VDC TA-SOLID	56289	150D226X9035R2
A2C6	0160-0544	1	CAPACITOR-FXD .022UF +-20% 4000WVDC MET	84411	HEW-337
A2C7	0160-4024	1	CAPACITOR-FXD .1UF +-20% 4000WVDC MET	56289	430P104040
A2C8	0160-0684	2	CAPACITOR-FXD 1000PF +-20% 4000WVDC MET	84411	HEW337
A2C9	0150-0115	1	CAPACITOR-FXD 27 PF +-10% 500 WVDC CER	28480	0150-0115
A2C10	0160-0684		CAPACITOR-FXD 1000PF +-20% 4000WVDC MET	84411	HEW337
A2C11	0160-2234	1	CAPACITOR-FXD .51PF +-.25PF 500WVDC CER	28480	0160-2234
A2C12	0160-3443	7	CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0160-3443
A2C13	0160-0163	1	CAPACITOR-FXD .033UF +-10% 200WVDC POLYE	56289	292P33392
A2C14	0160-3453	1	CAPACITOR-FXD .05UF +80-20% 100WVDC CER	28480	0160-3453
A2C15	0160-3665	1	CAPACITOR-FXD .01UF +80-20% 500WVDC CER	28480	0160-3665
A2C16	0160-4051	1	CAPACITOR-FXD .01UF +-20% 4000WVDC MET	84411	HEW-337
A2C17	0170-0040		CAPACITOR-FXD .047UF +-10% 200WVDC POLYE	56289	292P47392
A2C18	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A2C19	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A2CR1	1901-0028	3	DIODE-PWR RECT 400V 750MA	04713	SR1358-9
A2CR2	1901-0028		DIODE-PWR RECT 400V 750MA	04713	SR1358-9
A2CR3	1901-0683	1	DIODE-HV RECT 250NS 10KV 5MA	28480	1901-0683
A2CR4	1901-0036	4	DIODE-HV RECT 1KV 600MA	28480	1901-0036
A2CR5	1901-0036		DIODE-HV RECT 1KV 600MA	28480	1901-0036
A2CR6	1901-0040		DIODE-SWITCHING 2NS 30V 50MA	28480	1901-0040
A2CR7	1901-0040		DIODE-SWITCHING 2NS 30V 50MA	28480	1901-0040
A2CR8	1901-0036		DIODE-HV RECT 1KV 600MA	28480	1901-0036
A2CR9	1901-0036		DIODE-HV RECT 1KV 600MA	28480	1901-0036
A2CR10	1901-0646	2	DIODE-PWR RECT 150NS 200V 1A	14099	S2F
A2CR11	1901-0646		DIODE-PWR RECT 150NS 200V 1A	14099	S2F
A2DS1	2140-0013	2	LAMP, GLOW, BULB T-2, 57V	74276	NE23A
A2DS2	2140-0013		LAMP, GLOW, BULB T-2, 57V	74276	NE23A
A2F1	2110-0020	1	FUSE .8A 250V SLO-BLO 1.25X.25	71400	MDL 8/10
A2L1	9140-0171	1	COIL-FXD MOLDED RF CHOKE 40UH 10%	06560	10608-1
A2L2	9140-0210	1	COIL-FXD MOLDED RF CHOKE 100UH 5%	24226	15/103
A2L3	9140-0129	1	COIL-FXD MOLDED RF CHOKE 220UH 5%	24226	15/223
A2MP1	5040-0430	2	MOUNT:TRANSFORMER	28480	5040-0430
A2MP2	5040-0430		MOUNT:TRANSFORMER	28480	5040-0430
A2MP3	2110-0269	12	FUSEHOLDER-CLIP TYPE .25FUSE	28480	2110-0269
A2MP4	2110-0269		FUSEHOLDER-CLIP TYPE .25FUSE	28480	2110-0269
A2P1	1251-3196	2	CONNECTOR 8-PIN M POST TYPE	27264	09-60-1081(2403-08A)
A2P2	1251-3276	1	CONNECTOR 6-PIN M POST TYPE	27264	09-60-1061(A2403-6A)
A2P3	1251-3192	1	CONNECTOR 3-PIN M POST TYPE	27264	09-60-1031(2403-03A)
A2Q1	1853-0020	1	TRANSISTOR PNP SI PD=300MW FT=150MHZ	28480	1853-0020
A2Q2	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A2Q3	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A2Q4	1853-0037	1	TRANSISTOR PNP SI TO-39 PD=1W FT=100MHZ	28480	1853-0037
A2Q5	1854-0022	1	TRANSISTOR NPN SI TO-39 PD=700MW	07263	S17843
A2R1	0757-0465		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A2R2	0757-0465		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A2R3	0684-1051	1	RESISTOR 1M 10% .25W FC TC=-800/+900	01121	CB1051
A2R4	0683-2265	1	RESISTOR 22M 5% .25W FC TC=-900/+1200	01121	CB2265
A2R5	0684-1011	5	RESISTOR 100 10% .25W FC TC=-400/+500	01121	CB1011

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A2R6	0684-1031	24	RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A2R7	0687-5611	2	RESISTOR 560 10% .5W CC TC=0+529	01121	EB5611
A2R8	0684-1021	19	RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A2R9	0684-1041	2	RESISTOR 100K 10% .25W FC TC=-400/+800	01121	CB1041
A2R10	0687-1531	1	RESISTOR 15K 10% .5W CC TC=0+765	01121	EB1531
A2R11	0687-5611		RESISTOR 560 10% .5W CC TC=0+529	01121	EB5611
A2R12	0684-4721		RESISTOR 4.7K 10% .25W FC TC=-400/+700	01121	CB4721
A2R13	0684-4721		RESISTOR 4.7K 10% .25W FC TC=-400/+700	01121	CB4721
A2R14	0684-1061	1	RESISTOR 10M 10% .25W FC TC=-900/+1100	01121	CB1061
A2R15	0687-1551	2	RESISTOR 1.5M 10% .5W CC TC=0+1000	01121	EB1551
A2R16	0687-1551		RESISTOR 1.5M 10% .5W CC TC=0+1000	01121	EB1551
A2R17	2100-3214	2	RESISTOR-VAR TRMR 100KOHM 10% C TOP ADJ	73138	72PR100K
A2R18	0698-3451	1	RESISTOR 133K 1% .125W F TC=0+-100	16299	C4-1/8-T0-1333-F
A2R19			NOT ASSIGNED		
A2R20	0687-4711	1	RESISTOR 470 10% .5W CC TC=0+529	01121	EB4711
A2R21	0757-0444	2	RESISTOR 12.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1212-F
A2R22	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R23	0698-0084		RESISTOR 2.15K 1% .125W F TC=0+-100	16299	C4-1/8-T0-2151-F
A2R24	0757-0434		RESISTOR 3.65K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3651-F
A2R25	0757-0278	2	RESISTOR 1.78K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1781-F
A2R26	0757-0456	1	RESISTOR 43.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4322-F
A2R27	0757-0274	9	RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1213-F
A2R28	0684-1521	1	RESISTOR 1.5K 10% .25W FC TC=-400/+700	01121	CB1521
A2R29	0684-4721		RESISTOR 4.7K 10% .25W FC TC=-400/+700	01121	CB4721
A2R30	0684-3931	1	RESISTOR 39K 10% .25W CC TUBULAR	01121	CB3931
A2R31	0757-0288		RESISTOR 9.09K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-9091-F
A2R32	2100-3253		RESISTOR-VAR TRMR 50KOHM 10% C TOP ADJ	73138	72PR50K
A2R33	0687-2221	2	RESISTOR 2.2K 10% .5W CC TC=0+647	01121	EB2221
A2R34	0687-2221		RESISTOR 2.2K 10% .5W CC TC=0+647	01121	EB2221
A2R35	2100-3355	1	RESISTOR-VAR TRMR 100KOHM 10% C SIDE ADJ	73138	72XR100K
A2R36	0757-0451	2	RESISTOR 24.3K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2432-F
A2R37	0757-0424	1	RESISTOR 1.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1101-F
A2R38	0757-0438		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A2R39	2100-3214		RESISTOR-VAR TRMR 100KOHM 10% C TOP ADJ	73138	72PR100K
A2R40	0757-0451		RESISTOR 24.3K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2432-F
A2R41	2100-3207	1	RESISTOR-VAR TRMR 5KOHM 10% C SIDE ADJ	32997	3386X-502
A2R42	0757-0422	1	RESISTOR 909 1% .125W F TC=0+-100	24546	C4-1/8-T0-909R-F
A2R43	0684-4741	1	RESISTOR 470K 10% .25W FC TC=-800/+900	01121	CB4741
A2R44	0698-8018	1	RESISTOR 30M 1% 3W CP TC=0+-100	03888	PVC175-3-T0-3004-F
A2U1	1826-0167	1	IC CA3094AT	02735	CA3094AT
A2XU1	1200-0763	1	SOCKET, ELEC, IC 8-CONT DIP SLDR TERM	71785	133-98-92-061
A2A1	01600-61101	1	TRANSFORMER ASSY, HIGH VOLTAGE	28480	01600-61101
A3	01600-66503	1	BOARD ASSY, LOW VOLTAGE	28480	01600-66503
A3C1	0180-0484	2	CAPACITOR-FXD; 4500UF+75-10% 25VDC AL (NOT SUPPLIED WITH A3, ORDER SEPARATELY)	56289	36D452G025AA-2B-DQB
A3C2	0160-3448		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3448
A3C3	0180-0484		CAPACITOR-FXD; 4500UF+75-10% 25VDC AL (NOT SUPPLIED WITH A3, ORDER SEPARATELY)	56289	36D452G025AA-2B-DQB
A3C4	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A3C5	0180-0482	1	CAPACITOR-FXD 250UF +50-10% 200VDC AL (NOT SUPPLIED WITH A3, ORDER SEPARATELY)	56289	36D251F200AA2A-DQB
A3C6	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A3C7	0180-0230	4	CAPACITOR-FXD; 1UF+-20% 50VDC TA-SOLID	56289	150D105X0050A2
A3C8	0180-0483	1	CAPACITOR-FXD; 22000UF+75-10% 15VDC AL (NOT SUPPLIED WITH A3, ORDER SEPARATELY)	56289	36D223G015AC2A-DQB
A3C9	0160-3448		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3448
A3C10	0180-0230		CAPACITOR-FXD; 1UF+-20% 50VDC TA-SOLID	56289	150D105X0050A2
A3C11	0180-1701	3	CAPACITOR-FXD; 6.8UF+-20% 6VDC TA-SOLID	56289	150D685X0006A2
A3C12	0180-0230		CAPACITOR-FXD; 1UF+-20% 50VDC TA-SOLID	56289	150D105X0050A2
A3C13	0160-3508	2	CAPACITOR-FXD 1UF +80-20% 50WVDC CER	28480	0160-3508
A3C14	0160-3448		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3448
A3C15	0160-3448		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3448
A3C16	0160-3448		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3448
A3CR1	1906-0027	3	DIODE-MULT FULL WAVE BRIDGE RECTIFIER	04713	MDA922-6
A3CR2	1906-0027		DIODE-MULT FULL WAVE BRIDGE RECTIFIER	04713	MDA922-6
A3CR3	1906-0027		DIODE-MULT FULL WAVE BRIDGE RECTIFIER	04713	MDA922-6
A3CR4	1901-0028		DIODE-PWR RECT 400V 750MA	04713	SR1358-9
A3DS1	2140-0008	1	LAMP, GLOW, BULB T-2, 59V	71744	A1A (NE-2)
A3F1	2110-0011	1	FUSE .062A 250V 1.25X.25 IEC	71400	AGC 1/16
A3F2	2110-0007	3	FUSE 1A 250V SLO-BLO 1.25X.25	71400	MDL-1
A3F3	2110-0007		FUSE 1A 250V SLO-BLO 1.25X.25	71400	MDL-1
A3F4	2110-0367	1	FUSE 5A 250V SLO-BLO 1.281X.259 UL IEC	71400	MDA-250-5
A3F5	2110-0012	1	FUSE .5A 250V 1.25X.25 IEC	71400	AGC 1/2

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A3MP1	1205-0258	1	THERMAL-LINK PLSTCPWR PKG	28480	1205-0258
A3MP2	1205-0226	1	HEAT SINK	28480	1205-0226
A3MP3	0340-0511	2	INSULATOR, TRANSISTOR	13103	43-77-2
A3MP4	1400-0439	2	CLAMP, SNAP-IN, 1.375 DIA .312W .594L	80033	E-50011-044
A3MP5	2110-0269		FUSEHOLDER-CLIP TYPE .25FUSE	28480	2110-0269
A3Q1	1854-0234	5	TRANSISTOR NPN 2N3440 SI TO-5 PD=1W	02735	2N3440
A3Q2	1854-0230	1	TRANSISTOR NPN SI PD=21W FT=10MHZ	28480	1854-0230
A3Q3	1854-0039	1	TRANSISTOR NPN 2N3053 SI TO-5 PD=1W	04713	2N3053
A3Q4	1884-0082	1	THYRISTOR-SCR JEDEC 2N4441	04713	2N4441
A3R1	0684-2741	1	RESISTOR 270K 10% .25W FC TC=-800/+900	01121	CB2741
A3R2	0684-2241		RESISTOR, 220K 10% .25W CC TUBULAR	01121	CB2241
A3R3	0757-0465		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A3R4	0757-0279	1	RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A3R5	0757-1093	2	RESISTOR 3K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3001-F
A3R6	0684-1041	4	RESISTOR, 100K 10% .25W CC TUBULAR	01121	CB1041
A3R7	0757-1093		RESISTOR 3K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3001-F
A3R8	0811-1531	1	RESISTOR 10K 1% 3W PW TC=0+-20	07088	KH-300
A3R9	0698-3447		RESISTOR 422 1% .125W F TC=0+-100	16299	C4-1/8-T0-422R-F
A3R10	0698-3394	1	RESISTOR 31.6 1% .5W F TC=0+-100	GK005	[illegible]
A3R11	0757-0342		RESISTOR, 100K 1% .25W F TUBULAR	24546	C5-1/4-T0-1003-F
A3R12	0811-1662	2	RESISTOR .47 5% 2W PW TC=0+-800	75042	BWH2-47/100-J
A3R13	0757-0427	3	RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
A3R14	0757-0427		RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
A3R15	0811-1662		RESISTOR .47 5% 2W PW TC=0+-800	75042	BWH2-47/100-J
A3R16	0684-1031		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A3R17	0757-0420		RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A3R18	2100-2574	1	RESISTOR-VAR TRMR 500 OHM 10% C SIDE ADJ	19701	ET50X501
A3R19	0757-0932	1	RESISTOR 2.2K 2% .125W F TC=0+-100	24546	C4-1/8-T0-2201-G
A3R20	0757-0289	1	RESISTOR 13.3K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-1332-F
A3R21	0757-0427		RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
A3R22	0683-5105		RESISTOR 51 5% .25W FC TC=-400/+500	01121	CB5105
A3R23	0684-1001	1	RESISTOR 10 10% .25W FC TC=-400/+500	01121	CB1001
A3R24	0757-0416		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A3U1	1820-0196	2	IC REGULATOR	07263	723HC
A3U2	1820-0196		IC REGULATOR	07263	723HC
A3VR1	1902-0049	4	DIODE-ZNR 6.19V 5% DO-7 PD=.4W TC=+.022%	04713	SZ 10939-122
A3VR2	1902-3193	1	DIODE-ZNR 13.3V 5% DO-7 PD=.4W TC=+.059%	04713	SZ 10939-218
A3VR3	1902-3104	1	DIODE-ZNR 5.62V 5% DO-7 PD=.4W TC=+.016%	04713	SZ 10939-110
A4	01600-66504	1	BOARD ASSY, UPPER SWITCH	28480	01600-66504
A4P1	1251-3971	7	CONNECTOR, POST TYPE 16-MALE FXD CONTACT	27264	22-03-1161
A4P2	1251-3975	1	CONNECTOR,POST TYPE 6-MALE FXD CONTACTS	27264	22-03-1061
A4R1	0684-2211	5	RESISTOR 220 10% .25W FC TC=-400/+600	01121	CB2211
A4R2	0684-2211		RESISTOR 220 10% .25W FC TC=-400/+600	01121	CB2211
A4R3	0684-2211		RESISTOR 220 10% .25W FC TC=-400/+600	01121	CB2211
A4R4	0684-2211		RESISTOR 220 10% .25W FC TC=-400/+600	01121	CB2211
A4S1	3101-1943	1	SWITCH	28480	3101-1943
A4U1	1820-0071	1	IC SN74 40 N	01295	SN7440N
A4U2	1820-0583		IC DM74L 00N	27014	DM74L00N
A4U3	1810-0183		NETWORK-RES 9-PIN SIP .1-PIN-SPCG	28480	1810-0183
A5	01600-66505	1	BOARD ASSY, LOWER SWITCH	28480	01600-66505
A5C1	0180-0229	1	CAPACITOR-FXD; 33UF+-10% 10VDC TA-SOLID	56289	150D336X9010B2
A5P1	1251-3971		CONNECTOR, POST TYPE 16-MALE FXD CONTACT	27264	22-03-1161
A5P2	1251-3975	1	CONNECTOR,POST TYPE 8-MALE FXD CONTACTS	27264	22-03-1081
A5R1	0684-4731		RESISTOR 47K 10% .25W FC TC=-400/+800	01121	CB4731
A5R2	0684-2211		RESISTOR 220 10% .25W FC TC=-400/+600	01121	CB2211
A5R3	0684-1021		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A5S1	3101-1944	1	SWITCH	28480	3101-1944
A5U1	1820-0068	1	IC SN74 10 N	01295	SN7410N
A5U2	1820-0730	2	IC MULTIVIBRATOR	34335	96L02DC
A5U3	1810-0183		NETWORK-RES 9-PIN SIP .1-PIN-SPCG	28480	1810-0183

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A6	01600-66506	1	BOARD ASSY, TRIGGER SWITCH	28480	01600-66506
A6S1	3101-0576	17	SWITCH-TGL SUBMIN SPDT NS 2A 250VAC	28480	3101-0576
A6S2	3101-0576		SWITCH-TGL SUBMIN SPDT NS 2A 250VAC	28480	3101-0576
A6S3	3101-0576		SWITCH-TGL SUBMIN SPDT NS 2A 250VAC	28480	3101-0576
A6S4	3101-0576		SWITCH-TGL SUBMIN SPDT NS 2A 250VAC	28480	3101-0576
A6S5	3101-0576		SWITCH-TGL SUBMIN SPDT NS 2A 250VAC	28480	3101-0576
A6S6	3101-0576		SWITCH-TGL SUBMIN SPDT NS 2A 250VAC	28480	3101-0576
A6S7	3101-0576		SWITCH-TGL SUBMIN SPDT NS 2A 250VAC	28480	3101-0576
A6S8	3101-0576		SWITCH-TGL SUBMIN SPDT NS 2A 250VAC	28480	3101-0576
A6S9	3101-0576		SWITCH-TGL SUBMIN SPDT NS 2A 250VAC	28480	3101-0576
A6S10	3101-0576		SWITCH-TGL SUBMIN SPDT NS 2A 250VAC	28480	3101-0576
A6S11	3101-0576		SWITCH-TGL SUBMIN SPDT NS 2A 250VAC	28480	3101-0576
A6S12	3101-0576		SWITCH-TGL SUBMIN SPDT NS 2A 250VAC	28480	3101-0576
A6S13	3101-0576		SWITCH-TGL SUBMIN SPDT NS 2A 250VAC	28480	3101-0576
A6S14	3101-0576		SWITCH-TGL SUBMIN SPDT NS 2A 250VAC	28480	3101-0576
A6S15	3101-0576		SWITCH-TGL SUBMIN SPDT NS 2A 250VAC	28480	3101-0576
A6S16	3101-0576		SWITCH-TGL SUBMIN SPDT NS 2A 250VAC	28480	3101-0576
A6S17	3101-0576		SWITCH-TGL SUBMIN SPDT NS 2A 250VAC	28480	3101-0576
A6W1	8120-0621	3	CABLE CA ASSY 14-COND 26AWG	28480	8120-0621
A6W2	8120-0621		CABLE CA ASSY 14-COND 26AWG	28480	8120-0621
A6W3	8120-0621		CABLE CA ASSY 14-COND 26AWG	28480	8120-0621
A7	01600-66507	1	BOARD ASSY, ANALOG	28480	01600-66507
A7C1	0180-1701		CAPACITOR-FXD; 6.8UF+-20% 6VDC TA-SOLID	56289	150D685X0006A2
A7C2	0160-2204		CAPACITOR-FXD 100PF +-5% 300WVDC MICA	28480	0160-2204
A7C3	0160-3443		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0160-3443
A7C4	0180-1701		CAPACITOR-FXD; 6.8UF+-20% 6VDC TA-SOLID	56289	150D685X0006A2
A7C5	0160-2204		CAPACITOR-FXD 100PF +-5% 300WVDC MICA	28480	0160-2204
A7C6	0160-3443		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0160-3443
A7C7	0160-0161	1	CAPACITOR-FXD .01UF +-10% 200WVDC POLYE	56289	292P10392
A7C8	0140-0136	1	CAPACITOR-FXD 1500PF +-2% 300WVDC MICA	72136	DM15F152G0300WV1CR
A7C9	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A7C10	0160-2207		CAPACITOR-FXD 300PF +-5% 300WVDC MICA	28480	0160-2207
A7C11	0160-2207		CAPACITOR-FXD 300PF +-5% 300WVDC MICA	28480	0160-2207
A7C12	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A7C13	0160-2303	2	CAPACITOR-FXD 36PF +-5% 300WVDC MICA	28480	0160-2303
A7C14	0160-0154	2	CAPACITOR-FXD 2200PF +-10% 200WVDC POLYE	56289	292P22292
A7C15	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A7C16	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A7C17	0160-0299	2	CAPACITOR-FXD 1800PF +-10% 200WVDC POLYE	56289	292P18292
A7C18	0180-0374	2	CAPACITOR-FXD; 10UF+-10% 20VDC TA-SOLID	56289	150D106X9020B2
A7C19	0160-3443		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0160-3443
A7C20	0160-3443		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0160-3443
A7C21	0160-2303		CAPACITOR-FXD 36PF +-5% 300WVDC MICA	28480	0160-2303
A7C22	0160-0154		CAPACITOR-FXD 2200PF +-10% 200WVDC POLYE	56289	292P22292
A7C23	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A7C24	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A7C25	0160-0299		CAPACITOR-FXD 1800PF +-10% 200WVDC POLYE	56289	292P18292
A7C26	0180-0374		CAPACITOR-FXD; 10UF+-10% 20VDC TA-SOLID	56289	150D106X9020B2
A7C27	0160-3443		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0160-3443
A7C28	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A7C29	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A7CR1	1901-0040		DIODE-SWITCHING 2NS 30V 50MA	28480	1901-0040
A7CR2	1901-0040		DIODE-SWITCHING 2NS 30V 50MA	28480	1901-0040
A7CR3	1901-0040		DIODE-SWITCHING 2NS 30V 50MA	28480	1901-0040
A7CR4	1901-0040		DIODE-SWITCHING 2NS 30V 50MA	28480	1901-0040
A7L1	9100-1663	1	COIL-FXD MOLDED RF CHOKE 2.7MH 5%	06560	22-1312-29J
A7P2	1251-3971		CONNECTOR, POST TYPE 16-MALE FXD CONTACT	27264	22-03-1161
A7Q1	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A7Q2	1853-0036	9	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A7Q3	1853-0036		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A7Q4	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A7Q5	1853-0036		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A7Q6	1853-0036		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A7Q7	1853-0036		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A7Q8	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A7Q9	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A7Q10	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A7Q11	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A7Q12	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A7Q13	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A7Q14	1854-0234		TRANSISTOR NPN 2N3440 SI TO-5 PD=1W	02735	2N3440
A7Q15	1854-0234		TRANSISTOR NPN 2N3440 SI TO-5 PD=1W	02735	2N3440

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A7Q16	1854-0234		TRANSISTOR NPN 2N3440 SI TO-5 PD=1W	02735	2N3440
A7Q17	1854-0234		TRANSISTOR NPN 2N3440 SI TO-5 PD=1W	02735	2N3440
A7Q18	1853-0036		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A7R1	0684-1031		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A7R2	0684-1021		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A7R3	0684-1031		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A7R4	0684-1031		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A7R5	0684-1031		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A7R6	0684-1031		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A7R7	0684-1031		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A7R8	0698-0085	2	RESISTOR 2.61K 1% .125W F TC=0+-100	16299	C4-1/8-T0-2611-F
A7R9	0698-3155	2	RESISTOR 4.64K 1% .125W F TC=0+-100	16299	C4-1/8-T0-4641-F
A7R10	0757-0273	4	RESISTOR 3.01K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3011-F
A7R11	0757-0273		RESISTOR 3.01K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3011-F
A7R12	0698-0085		RESISTOR 2.61K 1% .125W F TC=0+-100	16299	C4-1/8-T0-2611-F
A7R13	0698-3155		RESISTOR 4.64K 1% .125W F TC=0+-100	16299	C4-1/8-T0-4641-F
A7R14	0757-0273		RESISTOR 3.01K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3011-F
A7R15	0757-0273		RESISTOR 3.01K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3011-F
A7R16	0684-3311	3	RESISTOR 330 10% .25W FC TC=-400/+600	01121	CB3311
A7R17	0684-3311		RESISTOR 330 10% .25W FC TC=-400/+600	01121	CB3311
A7R18	0757-0428	1	RESISTOR 1.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1621-F
A7R19	0757-0441	1	RESISTOR 8.25K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8251-F
A7R20	0684-1031		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A7R21	2100-2489	1	RESISTOR-VAR TRMR 5KOHM 10% C SIDE ADJ	19701	ET50X502
A7R22	0757-0407		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A7R23	0757-0407		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A7R24	0757-0290	3	RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
A7R25	0684-1031		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A7R26	0684-2221	2	RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A7R27	0757-0200	2	RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5621-F
A7R28	0757-0399	1	RESISTOR 82.5 1% .125W F TC=0+-100	24546	C4-1/8-T0-82R5-F
A7R29	0757-0200		RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5621-F
A7R30	0757-0417	1	RESISTOR 562 1% .125W F TC=0+-100	24546	C4-1/8-T0-562R-F
A7R31	0757-0317	1	RESISTOR 1.33K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1331-F
A7R32	0675-2221	1	RESISTOR 2.2K 10% .125W CC TC=0+882	01121	BB2221
A7R33	0683-1135	1	RESISTOR 11K 5% .25W FC TC=-400/+800	01121	CB1135
A7R34	0684-1031		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A7R35	0684-1031		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A7R36	0757-0446	3	RESISTOR 15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1502-F
A7R37	0757-0466		RESISTOR, 110K 1% .125W F TUBULAR	24546	C4-1/8-T0-1103-F
A7R38	0757-0462	1	RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7502-F
A7R39	0757-0449	2	RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
A7R40	0757-0449		RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
A7R41	0757-0454	1	RESISTOR 33.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3322-F
A7R42	0698-3268	1	RESISTOR 11.5K 1% .125W F TC=0+-100	16299	C4-1/8-T0-1152-F
A7R43	0757-0444		RESISTOR 12.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1212-F
A7R44	0757-1094	3	RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A7R45	0757-0274		RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1213-F
A7R46	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A7R47	0684-4731		RESISTOR 47K 10% .25W FC TC=-400/+800	01121	CB4731
A7R48	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A7R49	0757-0431	4	RESISTOR 2.43K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2431-F
A7R50	0757-0431		RESISTOR 2.43K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2431-F
A7R51	0687-2731	4	RESISTOR 27K 10% .5W CC TC=0+765	01121	EB2731
A7R52	0687-2731		RESISTOR 27K 10% .5W CC TC=0+765	01121	EB2731
A7R53	0757-0274		RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1213-F
A7R54	0757-0274		RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1213-F
A7R55	0757-0274		RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1213-F
A7R56	0757-0433	2	RESISTOR 3.32K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3321-F
A7R57	0757-0416		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A7R58	0757-1094		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A7R59	0757-0438		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A7R60	0684-1011		RESISTOR 100 10% .25W FC TC=-400/+500	01121	CB1011
A7R61	0757-0283	1	RESISTOR, 2K 1% .125W F TUBULAR	24546	C4-1/8-T0-2001-F
A7R62	0684-1031		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A7R63	0757-0443	2	RESISTOR 11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1102-F
A7R64	0684-1031		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A7R65	0757-0442		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A7R66	0757-0288		RESISTOR 9.09K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-9091-F
A7R67	0757-1094		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A7R68	0757-0274		RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1213-F
A7R69	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A7R70	0684-4731		RESISTOR 47K 10% .25W FC TC=-400/+800	01121	CB4731
A7R71	2100-2497	1	RESISTOR-VAR TRMR 2KOHM 10% C TOP ADJ	19701	ET50W202
A7R72	0757-0431		RESISTOR 2.43K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2431-F
A7R73	0757-0431		RESISTOR 2.43K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2431-F
A7R74	0687-2731		RESISTOR 27K 10% .5W CC TC=0+765	01121	EB2731
A7R75	0687-2731		RESISTOR 27K 10% .5W CC TC=0+765	01121	EB2731

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A7R76	0757-0274		RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1211-F
A7R77	0757-0274		RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1211-F
A7R78	0757-0416		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A7R79	0757-0274		RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1211-F
A7R80	0757-0433		RESISTOR 3.32K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3321-F
A7R81	0684-1011		RESISTOR 100 10% .25W FC TC=-400/+500	01121	CB1011
A7R82	0757-0283	1	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A7R83	0757-0443		RESISTOR, 11K 1% .125W F TUBULAR	24546	C4-1/8-T0-1102-F
A7R84*	0698-7096	2	RESISTOR 10 10% .125W CC TC=0+500 (NOT INSTALLED ON BOARD AT FACTORY)	01121	BB1001
A7R85	0698-7096		RESISTOR 10 10% .125W CC TC=0+500	01121	BB1001
A7R86	0684-1031		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A7S1	3101-1945	1	SWITCH	28480	3101-1945
A7U1	1820-0708	5	IC MULTIPLEXER	07263	93L09DC
A7U2	1820-0708		IC MULTIPLEXER	07263	93L09DC
A7U3	1820-0708		IC MULTIPLEXER	07263	93L09DC
A7U4	1820-0708		IC MULTIPLEXER	07263	93L09DC
A7U5	1820-0708		IC MULTIPLEXER	07263	93L09DC
A7U6	1820-0708		IC MULTIPLEXER	07263	93L09DC
A7U7	1820-0533		IC DM74L 00N	27014	DM74L00N
A7U8	1820-0713		IC MULTIPLEXER	07263	93L22DC
A7U9	1820-0054	4	IC SN74 00 N	01295	SN7400N
A7U10	1820-1117	4	IC GATE	07263	9L86DC
A7U11	1820-1117		IC GATE	07263	9L86DC
A7U12	1820-1117		IC GATE	07263	9L86DC
A7U13	1820-0704		IC COMPARATOR	07263	93L24DC
A7U14	1816-0352	1	IC MEMORY	28480	1816-0352
A7U15	1826-0188	2	IC MC 1408L-8	04713	MC1408L-8
A7U16	1826-0188		IC MC 1408L-8	04713	MC1408L-8
A7U17	1820-0054		IC SN74 00 N	01295	SN7400N
A7U18	1820-0321	3	IC COMPARATOR (ANALOG)	07263	710HC
A7U19	1820-0991	1	IC CD4016AE	02735	CD4016AE
A7U20	1820-0201	2	IC MC 1439G	04713	MC1439G
A7U21	1820-0201		IC MC 1439G	04713	MC1439G
A7U22	1810-0183		NETWORK-RES 9-PIN SIP .1-PIN-SPCG	28480	1810-0183
A7VR1	1902-0049		DIODE-ZNR 6.19V 5% DO-7 PD=.4W TC=+.022%	04713	SZ 10939-122
A7VR2	1902-0049		DIODE-ZNR 6.19V 5% DO-7 PD=.4W TC=+.022%	04713	SZ 10939-122
A8	01600-66508	1	BOARD ASSY, DIGITAL	28480	01600-66508
A8C1	0180-0228		CAPACITOR-FXD; 22UF+-10% 15VDC TA-SOLID	56289	150D226X9015B2
A8C2	0180-0228		CAPACITOR-FXD; 22UF+-10% 15VDC TA-SOLID	56289	150D226X9015B2
A8C3	0160-0168		CAPACITOR-FXD .1UF +-10% 200WVDC POLYE	56289	292P10492
A8C4	0180-0228		CAPACITOR-FXD; 22UF+-10% 15VDC TA SOLID	56289	150D226X9015B2
A8C5	0180-0230		CAPACITOR-FXD; 1UF+-20% 50VDC TA SOLID	56289	150D105X0050A2
A8C6	0180-0116		CAPACITOR-FXD; 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A8C7	0160-3508		CAPACITOR-FXD 1UF +80-20% 50WVDC CER	28480	0160-3508
A8C8	0180-0239	1	CAPACITOR-FXD; 1UF+75-10% 150VDC AL	56289	30D105G150BA2
A8C9	0180-0116		CAPACITOR-FXD; 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A8C10	0160-3443		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0160-3443
A8C11	0180-0116		CAPACITOR-FXD; 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A8C12	0160-0939	2	CAPACITOR-FXD 430PF +-5% 300WVDC MICA	28480	0160-0939
A8C13	0160-0939		CAPACITOR-FXD 430PF +-5% 300WVDC MICA	28480	0160-0939
A8C14	0180-0228		CAPACITOR-FXD: 22 UF +–10% 15VDC TA-SOLID	56289	150D226X901582
A8CR1	1901-0040		DIODE-SWITCHING 2NS 30V 50MA	28480	1901-0040
A8CR2	1901-0040		DIODE-SWITCHING 2NS 30V 50MA	28480	1901-0040
A8CR3	1901-0040		DIODE-SWITCHING 2NS 30V 50MA	28480	1901-0040
A8CR4	1901-0040		DIODE-SWITCHING 2NS 30V 50MA	28480	1901-0040
A8CR5	1901-0040		DIODE-SWITCHING 2NS 30V 50MA	28480	1901-0040
A8L1	9100-3139	1	COIL-FXD NON-MOLDED RF CHOKE 75UH 10%	28480	9100-3139
A8L2	9140-0137	1	COIL-FXD MOLDED RF CHOKE 1MH 5%	24226	15/104
A8P3	1251-3971		CONNECTOR, POST TYPE 16-MALE FXD CONTACT	27264	22-03-1161
A8P4	1251-3971		CONNECTOR, POST TYPE 16-MALE FXD CONTACT	27264	22-03-1161
A8P5	1251-3971		CONNECTOR, POST TYPE 16-MALE FXD CONTACT	27264	22-03-1161
A8P6	1251-3971		CONNECTOR, POST TYPE 16-MALE FXD CONTACT	27264	22-03-1161
A8P7	1251-3196		CONNECTOR 8-PIN M POST TYPE	27264	09-64-1081(2[illegible]8-08A)
A8Q1	1853-0036		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A8Q2	1853-0036		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A8Q3	1853-0036		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A8Q4	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A8R1	0684-1021		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A8R2	0684-3311		RESISTOR 330 10% .25W FC TC=-400/+600	01121	CB3311
A8R3	0684-1021		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A8R4	0684-1021		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A8R5	0684-1021		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021

See introduction to this section for ordering information

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A8R6	0684-1021		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A8R7	0684-1021		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A8R8	0684-2721	1	RESISTOR 2.7K 10% .25W FC TC=-400/+700	01121	CB2721
A8R9	0684-1021		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A8R10	0684-1031		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A8R11	0684-1031		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A8R12	0684-1021		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A8R13	0684-1031		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A8R14	0684-1031		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A8R15	0684-5621	3	RESISTOR 5.6K 10% .25W FC TC=-400/+700	01121	CB5621
A8R16	0757-0450	1	RESISTOR 22.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2212-F
A8R17	0757-0457		RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A8R18	0757-0465		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A8R19	0757-0472		RESISTOR 200K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2003-F
A8R20	0757-0452	1	RESISTOR 27.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2742-F
A8R21	0698-5450	3	RESISTOR 50K .1% .125W F TC=0+-50	19701	MF4C1/8-T2-5002-B
A8R22	0684-1021		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A8R23	0684-1021		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A8R24	0757-0438		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A8R25	0684-1011		RESISTOR 100 10% .25W FC TC=-400/+500	01121	CB1011
A8R26	0684-3921	1	RESISTOR 3.9K 10% .25W FC TC=-400/+700	01121	CB3921
A8R27	0684-1031		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A8R28	0684-1021		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A8R29	0684-2221		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A8R30	0757-0438		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A8R31	0757-0290		RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
A8R32	0757-0446		RESISTOR 15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1502-F
A8R33	0757-0290		RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
A8R34	0757-0278		RESISTOR 1.78K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1781-F
A8R35	0684-1031		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A8R36	0698-5450		RESISTOR 50K .1% .125W F TC=0+-50	19701	MF4C1/8-T2-5002-B
A8R37	0684-1021		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A8R38	0698-5450		RESISTOR 50K .1% .125W F TC=0+-50	19701	MF4C1/8-T2-5002-B
A8R39	0684-1021		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A8R40	0684-1021		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A8R41	0684-1021		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A8R42	0684-1031		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A8R43	0684-1021		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A8R44	0684-1031		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A8R45	0684-1031		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A8R46	0684-5621		RESISTOR 5.6K 10% .25W FC TC=-400/+700	01121	CB5621
A8R47	0684-5621		RESISTOR 5.6K 10% .25W FC TC=-400/+700	01121	CB5621
A8R48	0684-1011		RESISTOR 100 10% .25W FC TC=-400/+500	01121	CB1011
A8R49	0757-0448	1	RESISTOR 18.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1822-F
A8U1	1820-0596	6	IC DM74L 74N	27014	DM74L74N
A8U2	1820-0730		IC MULTIVIBRATOR	34335	96L02DC
A8U3	1820-0584		IC DM74L 02N	27014	DM74L02N
A8U4	1820-0054		IC SN74 00 N	01295	SN7400N
A8U5	1820-0778	1	IC COUNTER	07263	93L16DC
A8U6	1820-0077	1	IC SN74 74 N	01295	SN7474N
A8U7	1826-0119	1	IC NE 555T	18324	NE555T
A8U8	1820-1285	3	IC SN74LS 54 N	01295	SN74LS54N
A8U9	1820-0586	7	IC DM74L 04N	27014	DM74L04N
A8U10	1820-0321		IC COMPARATOR (ANALOG)	07263	710HC
A8U11	1820-0321		IC COMPARATOR (ANALOG)	07263	710HC
A8U12	1820-0063		IC SN74 51 N	01295	SN7451N
A8U13	1820-0584		IC DM74L 02N	27014	DM74L02N
A8U14	1820-1285		IC SN74LS 54 N	01295	SN74LS54N
A8U15	1820-0054		IC SN74 00 N	01295	SN7400N
A8U16	1820-0515		IC MULTIVIBRATOR	07263	9602DC
A8U17	1820-0691		IC SN74S 64 N	01295	SN74S64N
A8U18	1820-0658	2	IC MULTIPLEXER	07263	93L12DC
A8U19	1820-0584		IC DM74L 02N	27014	DM74L02N
A8U20	1820-0596		IC DM74L 74N	27014	DM74L74N
A8U21	1820-0587	1	IC DM74L 10N	27014	DM74L10N
A8U22	1820-0583		IC DM74L 00N	27014	DM74L00N
A8U23	1820-0596		IC DM74L 74N	27014	DM74L74N
A8U24	1820-0658		IC MULTIPLEXER	07263	93L12DC
A8U25	1820-0586		IC DM74L 04N	27014	DM74L04N
A8U26	1820-0584		IC DM74L 02N	27014	DM74L02N
A8U27	1820-0655	1	IC SN74 25 N	01295	SN7425N
A8U28	1820-0231	2	IC COUNTER	07263	9316DC
A8U29	1820-0231		IC COUNTER	07263	9316DC
A8U30	1820-0596		IC DM74L 74N	27014	DM74L74N

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A8U31	1820-0590	2	IC DM74L 51N	27014	DM74L51N
A8U32	1820-0590		IC DM74L 51N	27014	DM74L51N
A8U33	1820-0710		IC MULTIPLEXER	07263	93L22DC
A8U34	1820-0586		IC DM74L 04N	27014	DM74L04N
A8U35	1820-1285		IC SN74LS 54 N	01295	SN74LS54N
A8U36	1820-0586		IC DM74L 04N	27014	DM74L04N
A8U37	1820-0668	1	IC SN74 07 N	01295	SN7407N
A8U38	1820-0583		IC DM74L 00N	27014	DM74L00N
A8U39	1820-0586		IC DM74L 04N	27014	DM74L04N
A8U40	1820-0596		IC DM74L 74N	27014	DM74L74N
A8U41	1820-0585	2	IC DM74L 03N	27014	DM74L03N
A8U42	1820-0585		IC DM74L 03N	27014	DM74L03N
A8U43	1820-1117		IC GATE	07263	9L86PC
A8U44	1820-0596		IC DM74L 74N	27014	DM74L74N
A8U45	1820-0584		IC DM74L 02N	27014	DM74L02N
A8U46	1820-0586		IC DM74L 04N	27014	DM74L04N
A8U47	1818-0134	1	IC MM1101A/A1N	27014	MM1101A/A1N
A8U48	1820-0586		IC DM74L 04N	27014	DM74L04N
A8U49	1810-0183		NETWORK-RES 9-PIN SIP .1-PIN-SPCG	28480	1810-0183
A8U50	1810-0183		NETWORK-RES 9-PIN SIP .1-PIN-SPCG	28480	1810-0183
A8VR1	1902-3139	1	DIODE-ZNR 8.25V 5% DO-7 PD=.4W TC=+.053%	04713	SZ 10939-158
A8VR2	1902-0049		DIODE-ZNR 6.19V 5% DO-7 PD=.4W TC=+.022%	04713	SZ 10939-122
A8XA7	1251-2915	1	CONNECTOR; PC EDGE; 25-CONT; DIP SOLDER	71785	252-25-30-300
A9	0960-0430	1	ASSY, H.V. MULTIPLIER	28480	0960-0430
A10	01600-66510	1	BOARD ASSY, DIGITAL SWITCH	28480	01600-66510
A10S1	3100-3238	1	SWITCH, ROTARY	28480	3100-3238
A10W1	8120-0621		CABLE CA ASSY 14-COND 26AWG	28480	8120-0621
A10W2	8120-0621		CABLE CA ASSY 14-COND 26AWG	28480	8120-0621

Table 6-3. List of Manufacturers' Codes

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
GM005	DEUTSCHE VITROHM GMBH & CO	GERMANY	
01121	ALLEN BRADLEY CO	MILWAUKEE WI	53212
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS TX	75231
02735	RCA CORP SOLID STATE DIV	SOMMERVILLE NJ	08876
03888	PYROFILM CORP	WHIPPANY NJ	07981
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX AZ	85008
06560	AIRCO SPEER ELEK DIV AIR RDCN CO	NOGALES AZ	85621
07088	KELVIN ELECTRIC CO	VAN NUYS CA	91401
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW CA	94040
12697	CLAROSTAT MFG CO INC	DOVER NH	03820
13103	THERMALLOY CO	DALLAS TX	75247
14099	SEMTECH CORP	NEWBURY PARK CA	91320
16299	CORNING GL WK ELEC CMPNT DIV	RALEIGH NC	27604
18324	SIGNETICS CORP	SUNNYVALE CA	94086
19701	MEPCO/ELECTRA CORP	MINERAL WELLS TX	76067
24226	GOWANDA ELECTRONICS CORP	GOWANDA NY	14070
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD PA	16701
24995	ENVIRONMENTAL CONTAINER SYSTEMS INC	PALO ALTO CA	94304
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA CA	95051
27264	MOLEX PRODUCTS CO	DOWNERS GROVE IL	60515
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO CA	94304
32997	BOURNS INC TRIMPOT PROD DIV	RIVERSIDE CA	92507
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE CA	94086
34649	INTEL CORP	MOUNTAIN VIEW CA	94040
4G819	OVERLAND PRODUCTS CO	FREMONT NE	68025
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS MA	01247
71400	BUSSMAN MFG DIV OF MCGRAW-EDISON CO	ST LOUIS MO	63017
71450	CTS CORP	ELKHART IN	46514
71744	CHICAGO MINIATURE LAMP WORKS	CHICAGO IL	60640
71785	TRW ELEK COMPONENTS CINCH DIV	ELK GROVE VILLAGE IL	60007
72136	ELECTRO MOTIVE MFG CO INC	WILLIMANTIC CT	06226
73138	BECKMAN INSTRUMENTS INC HELIPOT DIV	FULLERTON CA	92634
73899	J F D ELECTRONICS CORP	BROOKLYN NY	11219
74276	SIGNALITE INC	NEPTUNE NJ	07753
75042	TRW INC PHILADELPHIA DIV	PHILADELPHIA PA	19108
80033	PRESTOLE EVERLOCK INC	TOLEDO OH	43605
82389	SWITCHCRAFT INC	CHICAGO IL	60630
84048	TRW INC ST PETERSBURG DIV	ST PETERSBURG FL	33702
84411	TRW CAPACITOR DIV	OGALLALA NE	69153
9D949	AMPHENOL SALES DIV OF BUNKER-RAMO	HAZELWOOD MO	63042

SECTION VII

MANUAL CHANGES AND OPTIONS

7-1. INTRODUCTION.

7-2. This section contains information required to backdate or update this manual for a specific instrument. Description of special options and standard options are also in this section.

7-3. MANUAL CHANGES.

7-4. This manual applies directly to the instrument having the same serial prefix shown on the manual title page. If the serial prefix of the instrument is not the same as the one on the title page, find your serial prefix in table 7-1 and make the changes to the manual that are listed for that serial prefix. When making changes listed in table 7-1, make the change with the highest number first. Example: if backdating changes 1, 2, and 3 are required for your serial prefix, do change 3 first, then change 2, and finally change 1. If the serial prefix of the instrument is not listed either in the title page or in table 7-1, refer to an enclosed MANUAL CHANGES sheet for updating information. Also, if a MANUAL CHANGES sheet is supplied, make all indicated ERRATA corrections.

Table 7-1. Manual Changes

Serial Prefix	Make Changes
No backdating changes	are required at this time.

7-5. SPECIAL OPTIONS.

7-6. Most customer special application requirements and/or specifications can be met by factory modification of a standard instrument. A standard instrument modified in this way will carry a special option number, such as Model 0000A/Option C01.

7-7. An operating and service manual and a manual insert are provided with each special option instrument. The operating and service manual contains information about the standard instrument. The manual insert for the special option describes the factory modifications required to produce the special option instrument. Amend the operating and service manual by changing it to include all manual insert information (and MANUAL CHANGES sheet information, if applicable). When these changes are made, the operating and service manual will apply to the special option instrument.

7-8. If you have ordered a special option instrument and the manual insert is missing, notify the nearest Hewlett-Packard Sales/Service Office. Be sure to give a full description of the instrument, including the complete serial number and special option number.

7-9. STANDARD OPTIONS.

7-10. Standard options are modifications installed on HP instruments at the factory and are available on request. Contact the nearest Hewlett-Packard Sales/Service Office for information concerning standard options.

Important

SERVICE
MANUAL
REQUEST

THIS PRELIMINARY SERVICE MANUAL
is supplied to you to permit earliest possible delivery of your instrument. The information included is as complete as possible at this time.

TO RECEIVE. . .
your copy of a complete Service Manual, when it is available, please fill out, detach self-addressed manual request card, and return (no postage necessary if mailed in the United States.)

NOTE: Manual will not be shipped until address card is received.