
# 1607A
# LOGIC STATE ANALYZER

## OPERATING AND SERVICE MANUAL



HEWLETT hp PACKARD
COLORADO SPRINGS DIVISION

## CERTIFICATION

*The Hewlett-Packard Company certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory. The Hewlett-Packard Company further certifies that its calibration measurements are traceable to the U.S. National Bureau of Standards to the extent allowed by the Bureau's calibration facility.*

## WARRANTY AND ASSISTANCE

This Hewlett-Packard product is warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products which prove to be defective during the warranty period provided they are returned to Hewlett-Packard. No other warranty is expressed or implied. We are not liable for consequential damages.

Service contracts or customer assistance agreements are available for Hewlett-Packard products that require maintenance and repair on-site.

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OPERATING AND SERVICE MANUAL

# MODEL 1607A
# LOGIC STATE ANALYZER

**SERIALS PREFIXED: 1530A**

Refer to Section VII for instruments with other serial prefixes.



HEWLETT-PACKARD COMPANY/COLORADO SPRINGS DIVISION
1900 GARDEN OF THE GODS ROAD, COLORADO SPRINGS, COLORADO, U.S.A.

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# SAFETY SUMMARY

*The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.*

**GROUND THE INSTRUMENT.**

*To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.*

**DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.**

*Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.*

**KEEP AWAY FROM LIVE CIRCUITS.**

*Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.*

**DO NOT SERVICE OR ADJUST ALONE.**

*Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.*

**DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.**

*Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.*

**DANGEROUS PROCEDURE WARNINGS.**

*Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.*

**WARNING**

*Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.*

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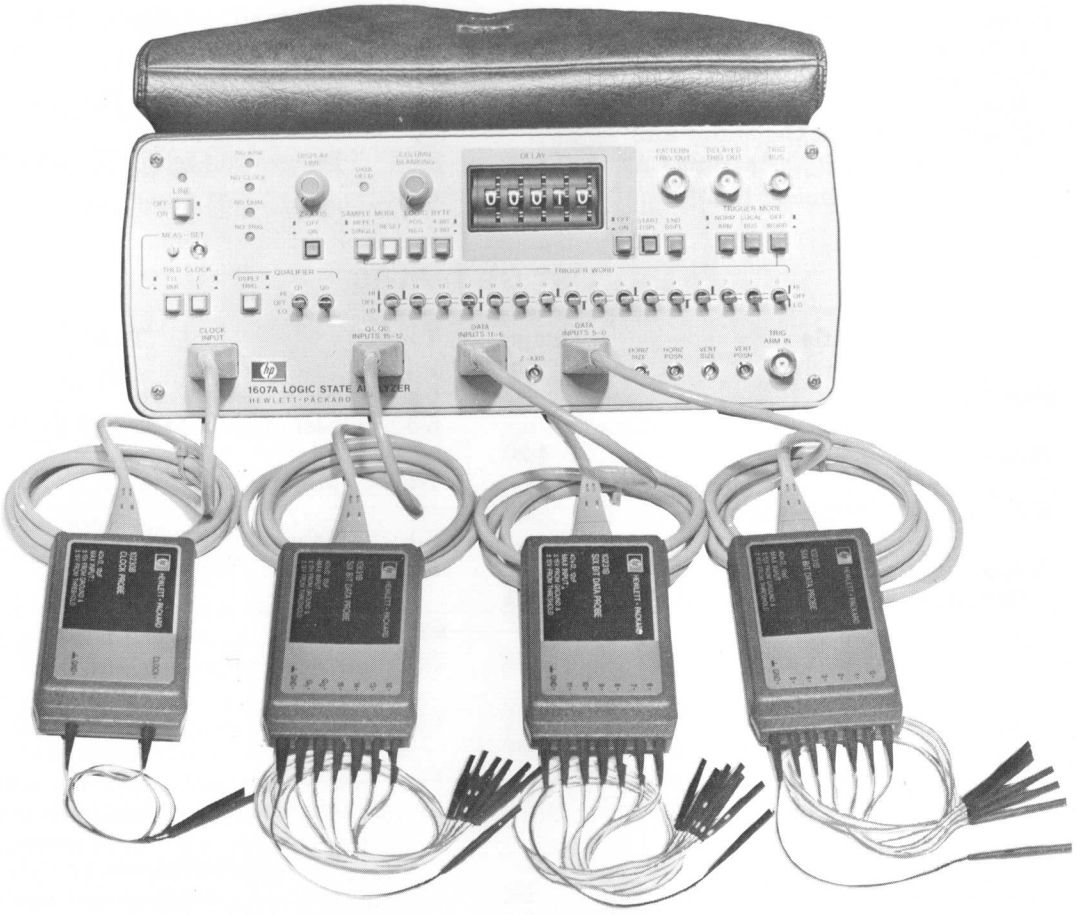



*Figure 1-1. Model 1607A Logic State Analyzer*

# SECTION I

# GENERAL INFORMATION

## 1-1. INTRODUCTION.

1-2. This manual provides operating and service information for the Hewlett-Packard Model 1607A Logic State Analyzer (figure 1-1).

1-3. This section of the manual contains performance specifications for the Model 1607A (table 1-1) and provides brief descriptive information on the instrument, accessories, and manual. Other sections provide information as follows:

Section II, Installation, contains information and procedures to perform an initial inspection, and to prepare the instrument for use, storage or shipment.

Section III, Operation, describes instrument controls, connectors, and panel features and provides operating checks and instructions.

Section IV, Principles of Operation, provides detailed descriptions and theory of instrument operation.

Section V, Maintenance, provides information required to verify that the instrument is performing in accordance with the specifications listed in table 1-1.

Section VI, Replaceable Parts, provides ordering information and a listing of replaceable parts.

Section VII, Manual Changes, provides manual change information (when applicable) to backdate this manual for use with instruments having serial prefix numbers lower than the one shown on the manual title page.

Section VIII, Service, provides information required to repair the instrument. Schematics, troubleshooting information, and service procedures are included.

1-4. On the title page of this manual, below the manual part number, is a "Microfiche" part number. This number can be used to order 4-by 6-inch microfilm transparencies of the manual. The microfiche package also includes the latest Manual Changes supplement.

## 1-5. DESCRIPTION.

1-6. The Model 1607A Logic State Analyzer is designed to aid in the analysis of digital systems that depend on sequences of logic states to control their operation. The Model 1607A provides horizontal, vertical and Z-axis signals that, when connected to the external horizontal, vertical and Z-axis inputs of an oscilloscope, convert the oscilloscope into a 16-channel logic state analyzer. The Model 1607A has vernier size and position controls with sufficient range to make interfacing possible with almost any display or oscilloscope. Display parameters required for interfacing with a Model 1607A are listed in table 1-1.

1-7. The Model 1607A can be operated with a Model 1600A Logic State Analyzer to form a 32-channel logic analyzer. The combined instruments permit analysis of machines using 32-bit word formats or dual-clock machines.

1-8. Data is synchronously loaded into the Model 1607A by the transition of the clock input corresponding to the clock slope selected. The Model 1607A will accept any convenient clock signal, such as a handshake signal on a data bus or other strobe or command lines, up to a 20-MHz rate. The Model 1607A has both a fixed TTL threshold and variable threshold selection, giving the Model 1607A the capability of interfacing with most logic families.

1-9. The Model 1607A provides a functional display of ones and zeros in tabular format of logic states at up to 16 variables in a digital system. Tabular data is displayed in a 16-word table of 16-bit words. A preset trigger word set on front-panel switches controls the reference of the sixteen-word display window to the input data stream. Depending on the sample mode selected, the display starts at the trigger word, ends at the trigger word (negative-time data capture), or is delayed up to 99 999 qualified input clock pulses after the trigger word.

1-10. During repetitive operation, the display is periodically updated by incoming data. To monitor infrequent or one-time-only events, the display can be set to a single-shot mode (SGL). In this mode, gathered data is retained and displayed until manually reset.

1-11. The Model 1607A has two qualifier channels that can function in either a trigger-qualified mode (TRIG) or a display-qualified mode (DSPLY). Trigger qualification allows the two qualifier channels to be used as additional undisplayed data channels, providing an 18-bit trigger word. Display qualification allows selective viewing of data by storing and displaying only those data words that occur on clock edges when qualifier conditions are true.

1-12. Other features of the Model 1607A include:

a. a trigger-arming circuit that increases triggering capability;

b. a partial-display mode to permit data to be displayed as it is single-stepped into the Model 1607A;

c. arrangement of the displayed words in bytes of three bits each (octal format) or in bytes of four bits each (hexadecimal or BCD format);

d. intensification of the trigger word;

e. the capability of blanking unrequired columns of bits, starting with the leftmost column;

f. two front-panel trigger outputs; one generated when the selected trigger word is detected, and the other generated when the delay is complete.

**1-14. ACCESSORIES SUPPLIED.** One Model 10230B Clock Probe and three Model 10231B Six Bit Data probes are supplied with the Model 1607A. The Model 10230B and Model 10231B are active probes providing compatible TTL (transistor-transistor logic) clock and data signals to the Model 1607A. Probe operating power is supplied by the Model 1607A. The probes connect to the Model 1607A front panel by means of 17-pin miniature snap-in connectors. Refer to the operating and service literature supplied with these probes for more detailed information.

**1-15. ACCESSORIES AVAILABLE.** A six-inch trigger interface cable (HP Model 10236A) and an 12-inch I/O interface cable (HP Model 10237A) are available

*Table 1-1. Specifications*

## CLOCK AND DATA INPUTS

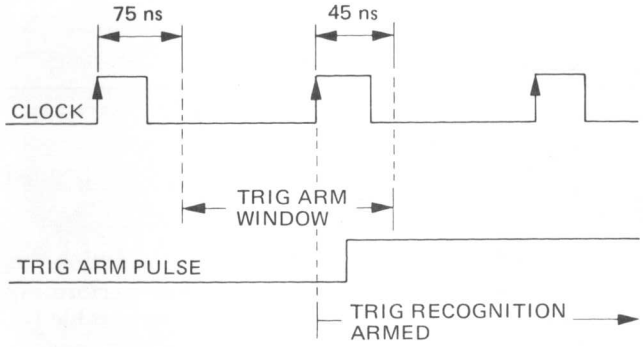
**REPETITION RATE:** 0 to 20 MHz.
**INPUT RC:** 40 kΩ ±3 kΩ shunted by ≤14 pF.
**INPUT BIAS CURRENT:** ≤30 μA.
**INPUT THRESHOLD:** TTL, fixed at approx +1.5 V; variable, ±10 Vdc.
**MAXIMUM INPUT**
**Level:** —15 to +15 Vdc.
**Swing:** 15 V peak from threshold.
**MINIMUM INPUT**
**Swing:** 0.5 V +5% of p-p threshold voltage.
**Clock Pulse Width:** 20 ns at threshold.
**Data Pulse Width:** 25 ns at threshold.
**Data Setup Time:** time data must be present prior to clock transition, 20 ns.
**Hold Time:** time data must be present after clock transition, 0 ns.

## PATTERN AND DELAYED TRIGGER OUTPUTS

**HIGH:** ≥2 V into 50Ω (line driver interface).
**LOW:** ≤0.4 V into 50Ω (line driver interface).
**PULSE DURATION**
**Delayed Trigger:** approx 25 ns (RZ format) at 1 V level.
**Pattern Trigger:** approx 25 ns in RZ format at 1 V level with delay set to zero or off. With delay on and not set to zero, pattern trigger output starts on receipt of a pattern trigger signal and ends when the delay ends.

## TRIGGER ARM INPUT

**IMPEDANCE:** 50Ω.
**LEVEL:** low state, 0 V to <0.4 V; high state, 2 V to <5 V.
**PULSE WIDTH:** 15 ns minimum at 1.5 V level.
**ARMING CONDITIONS:** if the arming pulse positive edge occurs <45 ns after a clock, triggering occurs on the same clock cycle that it is armed. If the arming pulse positive edge occurs >75 ns after a clock, triggering occurs on the next clock cycle.




## DISPLAY INTERFACE REQUIREMENTS

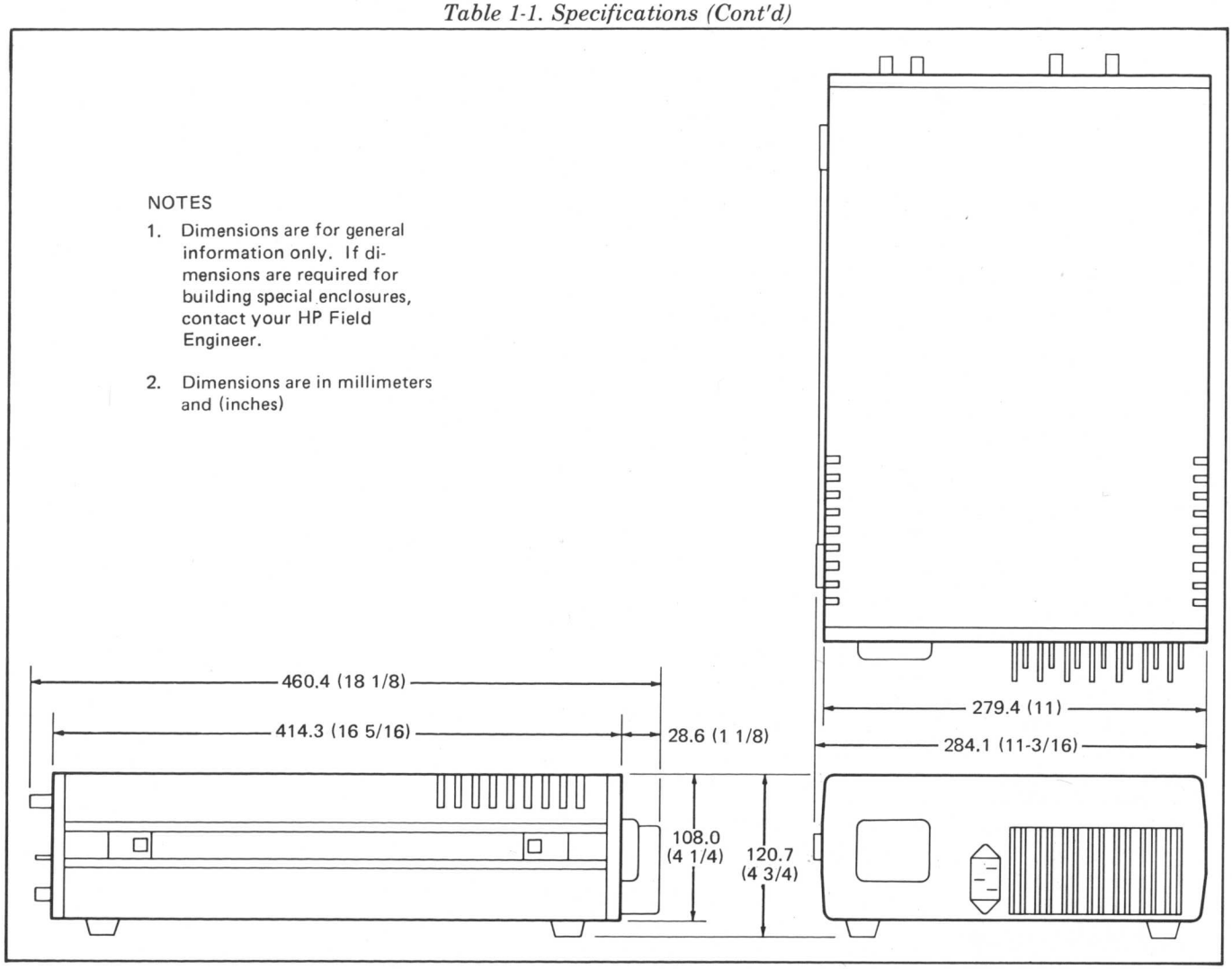
The 1607A interfaces with any oscilloscope or display with the following input parameters.

**X AND Y INPUTS:** 0.1 to 1 V/div deflection factors; dc coupled input; and >500 kHz bandwidth.
**Z-AXIS INPUT:** dc coupled with positive blanking; full blanking must occur with <10 V input at 10 mA.

## GENERAL

**DISPLAY TIME:** variable from <50 ms to >5 s.
**POWER REQUIREMENTS:** 100, 120, 220 or 240 Vac +5, —10%; 48 to 440 Hz, maximum power 120 VA (nominal 88 VA).
**DIMENSIONS:** see outline drawings.
**WEIGHT:** net 5.95 kg (13 1/8 lb); shipping, 7.77 kg (17 1/8 lb.)
**OPERATING ENVIRONMENT**
**Temperature:** 0°C to +55°C.
**Humidity:** to 95% at 40°C.
**Altitude:** to 4600 m (15 000 ft).
**Vibration:** vibrated in three planes for 15 min. each with 0.254 mm (0.010 in.) excursion, 10 to 55 Hz.

*Table 1-1. Specifications (Cont'd)*




for use with the Model 1607A. These cables are required to interface the Model 1607A with a Model 1600A in the bus mode.

## 1-16. INSTRUMENT AND MANUAL IDENTIFICATION.

1-17. Instrument identification by serial number is located on the rear panel. Hewlett-Packard uses a two-section serial number consisting of a four-digit prefix and a five-digit suffix, separated by a letter designating the country in which the instrument was manufactured. (A = U.S.A.; G = West Germany; J = Japan; U = United Kingdon.)

1-18. This manual applies to instruments with the serial numbers indicated on the title page. If changes have been made in the instrument since this manual was printed, a "Manual Changes" supplement supplied with the manual will define these changes. Be sure to record these changes in your manual. Backdating information in Section VII adapts the manual to instruments with serial numbers lower than that shown on the title page. Part numbers for the manual and the microfiche copy of the manual are also shown on the title page.

# SECTION II

# INSTALLATION

## 2-1. INTRODUCTION.

2-2. This section contains instructions for performing an initial inspection of the Model 1607A. Installation procedures and precautions are presented in step-by-step order. The procedures for making a claim for warranty repairs and for repacking the instrument for shipment are also described in this section.

## 2-3. INITIAL INSPECTION.

2-4. The instrument was inspected mechanically and electrically before shipment. Upon receipt, inspect it for damage that may have occurred in transit. Check for broken knobs, bent or broken connectors, and dents or scratches. If damage is found, refer to the claims paragraph in this section. Retain the packing material for possible future use.

2-5. Check the operation of the instrument immediately after receipt. Refer to Section III for the operator's checks and adjustments. The operator's check will determine whether or not the instrument is operating properly. If the instrument does not operate properly, refer to the claims paragraph in this section.

## 2-6. PREPARATION FOR USE.

**WARNING**

Read the Safety Summary at the front of this manual before installing or operating the instrument.

**2-7. POWER REQUIREMENTS.** The instrument requires a source of 100, 120, 220, or 240 volts ac +5%, —10%, single-phase, 48 to 440 Hz that can deliver approximately 120 volt-amperes. The instrument is normally shipped from the factory to operate from a 120-volt ac power source. The LINE SELECTOR slide switches on the rear panel select either 100-, 120-, 220-, or 240-volt operation. To check or change the position of the LINE SELECTOR switches, see figure 2-1 and proceed as follows:

a. Turn off instrument power and remove power cord from rear-panel connector.

b. For 100- or 120-volt operation, set LINE SELECTOR switches to 100 V or 120 V and install 1-ampere, time-delay fuse for F1.

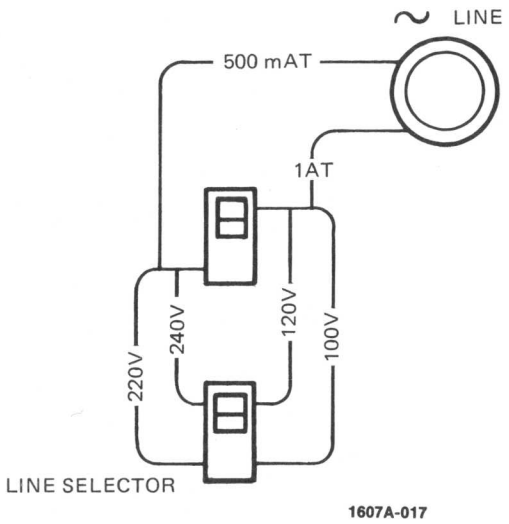



*Figure 2-1. Line Voltage Selection*

c. For 220- or 240-volt operation, set LINE SELECTOR switches to 220 V or 240 V and install 500-mA, time-delay fuse for F1.

d. Reconnect power cord.

**2-8. THREE-CONDUCTOR POWER CABLE.** This instrument is equipped with a three-conductor power cable that, when connected to an appropriate receptacle, grounds the instrument through the offset pin. The power cable required depends on the ac input voltage, and the country in which the instrument is to be used. Figure 2-2 illustrates the standard power receptacle (wall outlet) configurations that are used throughout the United States and in other countries. The HP part number shown adjacent to each receptacle drawing is the part number for a power cable equipped with a mating plug for that receptacle. If the appropriate power cable is not included with the instrument, notify the nearest Hewlett-Packard Sales/Service Office and a replacement cable will be provided.

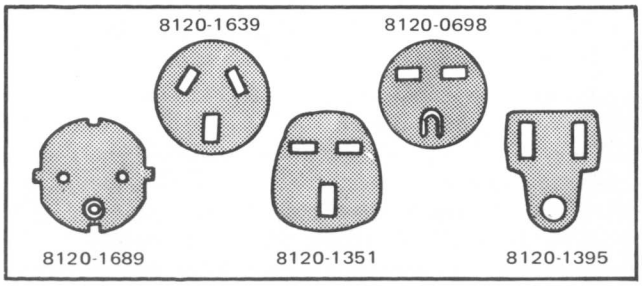



*Figure 2-2. Power Receptacles*

**2-9. INSTRUMENT COOLING.** The instrument is adequately cooled by normal air circulation. Install the Model 1607A in a location that provides at least 1.5 inches of clearance at the rear and one-inch clearance on both sides of the cabinet.

## 2-10. CLAIMS.

2-11. The warranty statement applicable to this instrument is printed inside the front cover of this manual. If physical damage is found or if operation is not as specified when the instrument is received, notify the carrier and nearest HP Sales/Service Office immediately (refer to the list in back of this manual for addresses). The HP Sales/Service Office will arrange for repair or replacement without waiting for settlement of the claim with the carrier.

## 2-12. REPACKING FOR SHIPMENT.

2-13. If the Model 1607A is to be shipped to an HP Sales/Service Office for service or repair, attach a tag showing owner (with address), complete instrument serial number, and a description of the service required.

2-14. Use the original shipping carton and packing material. If the original packing material is not available, the HP Sales/Service Office will provide information and recommendations on materials to be used.

# SECTION III

# OPERATION

## 3-1. INTRODUCTION.

3-2. This section contains an explanation of the Model 1607A operating controls, modes of operation, operator's checks and adjustments, and operating instructions for most applications.

**NOTE**

Paragraph 3-38 provides a detailed turn-on procedure for the Model 1607A.

## 3-3. CONTROLS AND CONNECTORS.

3-4. Figure 3-1 shows the Model 1607A front and rear panels and provides functional descriptions of operating controls, connectors, and indicators.

## 3-5. CLOCK, DATA, AND QUALIFIER INPUTS.

3-6. Clock, data and qualifier inputs to the Model 1607A are supplied by monitor probes which connect to the front-panel clock and data input connectors. Each monitor probe comprises connecting devices and buffer amplifier-comparators. Input threshold levels for the buffer amplifier-comparators are supplied by the Model 1607A. One clock probe and three six-channel data probes are required to operate the Model 1607A. Refer to the operating and service literature supplied with the probes for further information.

## 3-7. TRIGGERING REQUIREMENTS.

3-8. Triggering requirements for the Model 1607A are satisified when the input data word in sync with a qualified CLOCK INPUT pulse matches the TRIGGER WORD switch setting, and trigger arming and trigger bus conditions are met. The TRIGGER WORD switches are set to HI to recognize a positive logic state, LO to recognize a negative logic state, or to OFF for non-required or don't care input channels. Once triggering requirements are met, the Model 1607A will display 16 sequential words of input data in one of several modes.

## 3-9. SAMPLE MODES.

3-10. In the repetitive (REPET) sampling mode, displayed data is periodically updated approximately every 50 milliseconds to five seconds depending on the setting of the DISPLAY TIME control. In the single-shot (SINGLE) sampling mode new data is not displayed until the RESET button is pushed. Then one 16-word data block is displayed until RESET is pushed again.

**NOTE**

The intensified word may not necessarily be the trigger word if the START DSPL, END DSPL, or DELAY switch settings are changed after data acquisition in the single-sample mode.

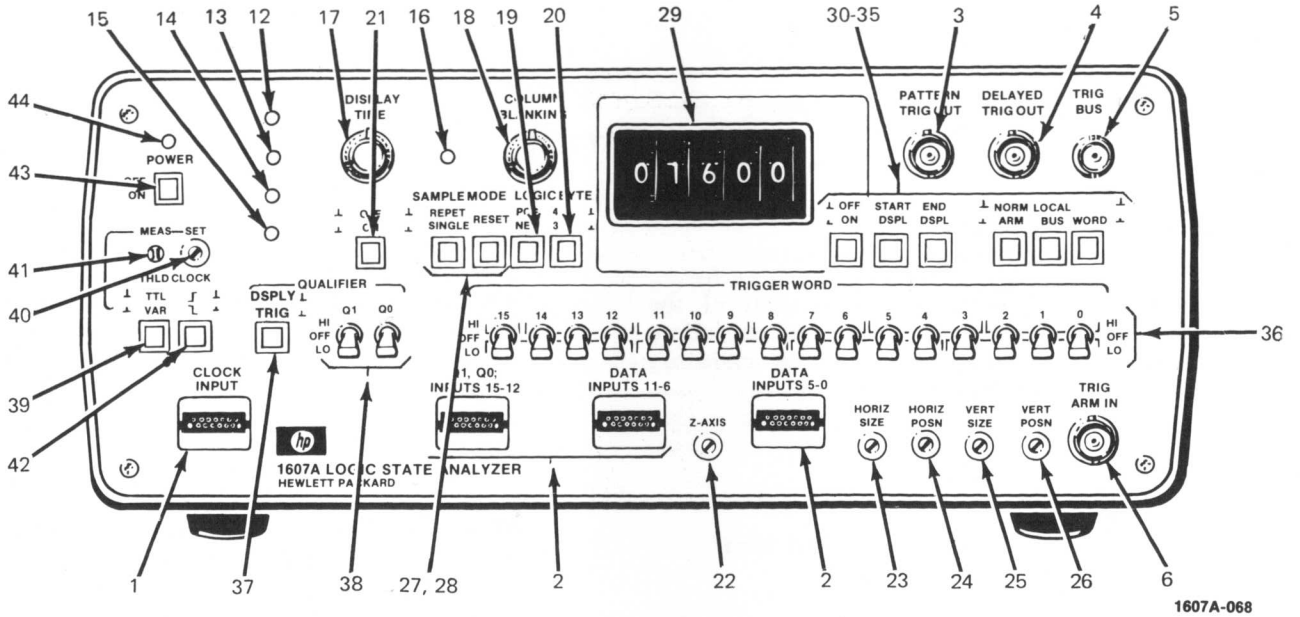
## 3-11. TRIGGER MODES.

**3-12. START DISPLAY.** In START DSPL with DELAY set to zero, the triggering word (the input data word matching the TRIGGER WORD settings) is positioned at the top of the display with the next 15 input data words positioned in order below the triggering word.

**3-13. END DISPLAY.** In END DSPL with DELAY set to zero, the 15 input data words preceding the triggering word are displayed in order from the top of the display with the triggering word positioned at the bottom.

**3-14. DELAY.** With DELAY ON/OFF in the ON position any 16-word data block from 0 to 99 999 qualified input clock pulses following the triggering word can be selected for display. In START DSPL, the DELAY sets the number of qualified clock pulses the first displayed word is delayed from the trigger word. In END DSPL, DELAY sets the number of qualified clock pulses the last displayed word is delayed from the trigger word. In either mode, DELAY sets the number of qualified clock pulses the DELAYED TRIG OUT pulse is delayed from the trigger word. Setting DELAY ON/OFF to OFF is equivalent to setting all DELAY thumbwheels to zero.

**3-15. NORM/ARM.** In NORM position, a trigger is produced anytime the Model 1607A trigger word and qualifier conditions are met. In the ARM position, the Model 1607A trigger generator cannot produce a trigger pulse until it has been armed by a positive-going transition on the TRIG ARM input. NORM/ARM permits selection of a trigger point that is dependent upon previously specified conditions (sequential triggering). EXAMPLE: The TRIG ARM input

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### INPUTS/OUTPUTS

1. **CLOCK INPUT.** Clocking signal input connector.

2. **Q1, Q0, INPUTS 15-12; DATA INPUTS 11-16; DATA INPUTS 5-0.** Monitored-data input connectors. Each connector supplies six parallel data channels.

3. **PATTERN TRIG OUT.** Output connector for trigger pulse generated when the input data meets triggering requirements. The trigger pulse remains high until the delay generator produces a pulse on DELAYED TRIG OUT.

4. **DELAYED TRIG OUT.** Output connector for trigger pulse delayed from PATTERN TRIG OUT by the number of display qualified clock pulses selected by DELAY.

5. **TRIG ARM IN.** Input connector for trigger recognition arming signal.

6. **TRIG BUS.** Connector for trigger bus signal. Connect TRIG BUS to TRIG BUS on a Model 1600A only.

7. **I/O PORT.** Connector for bidirectional data and control signal interface cable between the Model 1607A and a Model 1600A.

8. **LOGIC PROBE.** +5 V power connector for use with logic probes requiring less than 100 mA.

9. **HORIZ.** Connector for horizontal output signal. Connect to external horizontal input of oscilloscope or display.

10. **VERT.** Connector for vertical output signal. Connect to vertical input of oscilloscope or display.

11. **Z-AXIS.** Connector for Z-axis blanking signal. Connect to Z-axis input of oscilloscope or display.

### INDICATORS

12. **NO ARM.** Indicator light showing when the Model 1607A has remained unarmed for more than approximately 0.1 second.

13. **NO CLOCK.** Indicator light showing that the Model 1607A has not received a clock for more than approximately 0.1 second.

14. **NO QUAL.** Indicator light showing that the Model 1607A has not received a display qualifier for more than approximately 0.1 second. NO QUAL is disabled when the qualifier DSPLY/TRIG pushbutton is set to TRIG or the NO CLOCK light is on.

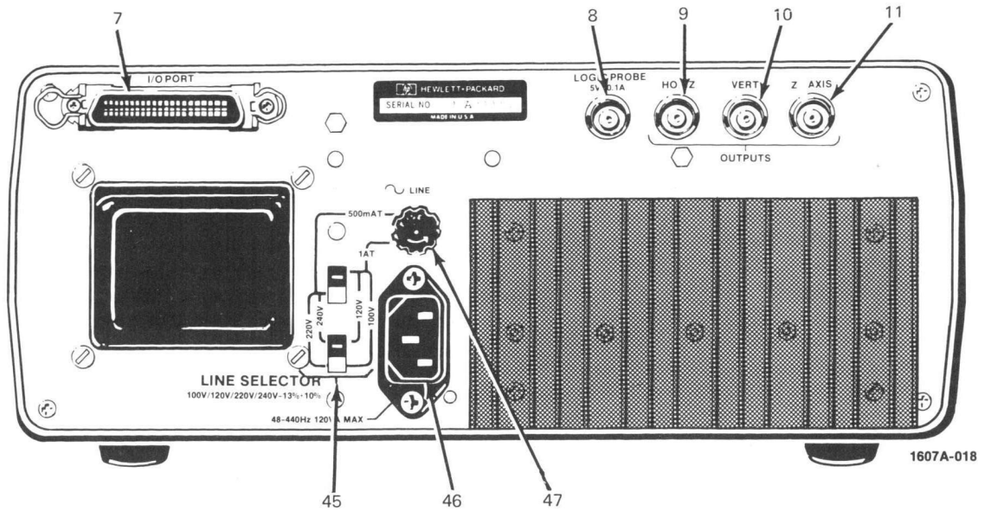
15. **NO TRIG.** Indicator light showing that the Model 1607A has not received a trigger for more than approximately 0.1 second. NO TRIG is disabled if NO ARM, NO CLOCK or NO QUAL are lit.

16. **DATA HELD.** Indicator light showing that the Model 1607A data has been displayed for more than approximately 0.3 second without being updated.

### DISPLAY

17. **DISPLAY TIME.** Control to adjust the length of time a display is retained on the CRT before being updated in the REPET mode.

*Figure 3-1. Front- and Rear-panel Controls, Connectors and Indicators*




18. **COLUMN BLANKING.** Control for blanking unused columns. Blanking begins with the most significant bit and the least significant bit cannot be blanked.

19. **LOGIC POS/NEG.** Matches sense of displayed characters to desired logic polarity. POS for positive logic (the most positive level is a 1), or NEG for negative logic (the most negative level is a 1).

20. **BYTE 4 BIT/3 BIT.** 4 BIT groups the 16-bit word format into bytes of 4 bits each. 3 BIT groups the 16-bit word format into bytes of 3 bits each with the MSB left over.

21. **Z-AXIS ON/OFF.** Control for turning Z-axis modulation on or off. OFF position turns off Z-axis modulation.

22. **Z-AXIS.** Screwdriver adjustment for setting level of Z-axis modulation signal for proper interface with an oscilloscope.

23. **HORIZ SIZE.** Screwdriver adjustment for setting the horizontal size of the 16-word display on the oscilloscope CRT.

24. **HORIZ POSN.** Screwdriver adjustment for setting the horizontal position of the 16-word display on the oscilloscope CRT.

25. **VERT SIZE.** Screwdriver adjustment for setting the vertical size of the 16-word display on the oscilloscope CRT.

26. **VERT POSN.** Screwdriver adjustment for setting the vertical position of the 16-word display on the oscilloscope CRT.

### SAMPLE MODE

27. **REPET/SINGLE.**
    a. REPET. With REPET (repetitive) selected, displayed data is updated every 50 ms to five seconds, depending on the setting of DISPLAY TIME.
    b. SINGLE. In SINGLE, data is acquired once each time RESET is pressed. The acquired data is displayed until RESET is pressed again.

28. **RESET.** RESET causes the Model 1607A to return immediately to the beginning of a data acquisition cycle.

### TRIGGER MODE

29. **DELAY.** IN START DSPL, DELAY sets the number of display-qualified clock pulses the first displayed word is delayed from the trigger word. In END DSPL, DELAY sets the number of display-qualified clock pulses the last displayed word is delayed from the trigger word. In either mode, DELAY sets the number of display-qualified clock pulses DELAYED TRIG OUT is delayed from the trigger word.

30. **DELAY ON/OFF.** Turns the delay generator on or off. The OFF position has the same effect as setting all DELAY thumbwheels to zero.

31. **START DSPL.** When selected, the trigger word is the first (top) displayed word and the next 15 qualified input clocks enter the remaining 15 displayed words in memory (DELAY off).

32. **END DSPL.** When selected, trigger word is last (bottom) word displayed with preceding 15 qualified words displayed above.

33. **NORM/ARM.** In ARM position, the trigger recognition circuit cannot produce a trigger until it has been armed by a positive-going transition on the TRIG ARM input. In NORM position, a trigger is produced any time trigger word and qualifier conditions are met.

34. **LOCAL/BUS.** In LOCAL position the Model 1607A will trigger whenever the incoming data meets the Model 1607A local triggering requirements, regardless of the status of other instruments on the trigger bus. In BUS position, a trigger is generated only when the incoming data on both bussed instruments match the settings of their combined TRIGGER WORD switches. When trigger bus cable is disconnected, Model 1607A functions in local mode regardless of switch setting.

35. **OFF/WORD.** The OFF position (out) disables the 16 TRIGGER WORD switches (equivalent to placing all TRIGGER WORD switches in the off position). OFF/WORD has no effect on qualifier channels.

36. **TRIGGER WORD.** Control switches for selecting trigger word. OFF is a "don't care" position.

### QUALIFIER

37. **DSPLY/TRIG.**
    a. DSPLY. Prohibits Model 1607A from displaying data or generating a trigger unless the conditions set by Q0 and Q1 are true when the clock edge occurs.
    b. TRIG. Prohibits the Model 1607A from generating a trigger unless the conditions set by Q0 and Q1 are true. TRIG extends TRIGGER WORD to 18 bits.

38. **Q1, Q0.** Control switches for setting the pattern that the qualifier bits must match for data to be displayed or a trigger to be generated. OFF is a "don't care" position.

### THRESHOLD

39. **THLD TTL/VAR.**
    a. TTL. Sets input threshold of the clock and data probes to +1.5 V.
    b. VAR. Allows input threshold of the clock and data probes to be varied from —10 V to +10 V.

40. **SET.** Screwdriver adjustment for adjusting the probe input threshold voltage over a range of ±10 V.

41. **MEAS.** Test point for monitoring SET threshold level.

42. **CLOCK.** Pushbutton selection of clock transition used to clock data into Model 1607A. Out position selects positive-going transition and in position selects negative-going transition.

### POWER

43. **LINE.** Model 1607A line power switch.

44. **Line Lamp.** Lights when the instrument is on.

45. **LINE SELECTOR.** Slide switches for selecting 100, 120, 220, or 240 Vac line operation.

46. **Power Input.** Power cable connector.

47. **FUSE.** 1 A time-delay fuse for 100- or 120-Vac operation, 500 mA time-delay fuse for 220- or 240-Vac operation.

*Figure 3-1.*
*Front- and Rear-panel Controls, Connectors and Indicators (Cont'd)*

could be the PATTERN TRIG OUT or DELAYED TRIG OUT pulse from another Model 1607A or a Model 1600A.

**3-16. LOCAL/BUS.** In the LOCAL position, the Model 1607A will trigger whenever the incoming data meets Model 1607A triggering requirements. In the BUS position, a trigger is generated only when the incoming data on both instruments connected to the trigger bus match the settings of their respective TRIGGER WORD switches. This feature allows two instruments to be bussed together to form up to a 32-bit-wide trigger (36-bits wide with TRIG qualification selected) enabling larger word-sized machines to be analyzed.

## 3-17. QUALIFIER MODES.

3-18. Display qualification prohibits the Model 1607A from recognizing any clock input unless the conditions set by Q0 and Q1 are true. On bus structures where data is being multiplexed such as in computers or microprocessors, display qualification permits selective viewing of data by ignoring unqualified clock edges. Trigger qualification prohibits the Model 1607A from generating a trigger unless the conditions set by Q0 and Q1 are true. With trigger qualification, Q0 and Q1 become two additional undisplayed channels, i.e., the trigger word becomes 18-bits wide.

3-19. When the DSPLY/TRIG switch is set to DSPLY, the Model 1607A will display only that data that is properly qualified when a clock occurs. When TRIG is selected, the instrument triggers on an 18-bit trigger word.

## 3-20. PARTIAL DISPLAYS.

3-21. In the partial display mode, the Model 1607A displays data words on the CRT one word at a time as they are received, not waiting until a complete 16-word data block is in memory. The Model 1607A will go into a partial display mode anytime the qualified clock rate is less than approximately 30 Hz. A slow qualified clock rate can be either a low-frequency clock or a high-frequency clock qualified infrequently.

3-22. In START DSPL, the CRT is blanked until the trigger word is found. The trigger word is then displayed and the following words are added to the display with subsequent clocks. In END DSPL, data words are displayed one word at a time as clocks are detected. After 16 words are displayed, each additional clock shifts the display up one word until the trigger word is displayed. The trigger word is intensified and held for the length of time set by DISPLAY TIME.

## 3-23. PATTERN TRIG OUT/DELAYED TRIG OUT.

3-24. PATTERN TRIG OUT and DELAYED TRIG OUT provide 50-ohm compatible trigger outputs. PATTERN TRIG OUT provides a pulse when the Model 1607A input data meets triggering requirements. The PATTERN TRIG OUT pulse remains high until the delay generator produces a pulse on DELAYED TRIG OUT. DELAYED TRIG OUT is delayed from PATTERN TRIG OUT by the number of display-qualified clock pulses selected by the DELAY thumbwheels. With DELAY set to zero, PATTERN TRIG OUT provides a RZ pulse approximately 25 ns wide.

## 3-25. DISPLAY FEATURES.

3-26. The following controls enable the Model 1607A operator to select the most usable display for his application.

**3-27. DISPLAY TIME.** The DISPLAY TIME control determines the length of time a given 16-word data block is displayed on the CRT before being updated by new input data. The time between data block updates can be set from approximately 50 milliseconds (fully ccw) to approximately five seconds (full cw). DISPLAY TIME is used to reduce display flicker at low data acquisition rates.

**3-28. COLUMN BLANKING.** The COLUMN BLANKING control is used to eliminate unused vertical columns on the display. Blanking begins with the most significant bit column. The least significant bit cannot be blanked. EXAMPLE: When monitoring a series of eight-bit data words, the eight unused vertical columns can be removed from the CRT display by adjustment of COLUMN BLANKING.

**3-29. LOGIC NEG/POS.** The POS position (out) causes the most-positive input voltage level to be displayed as a one, and the most-negative level to be displyed as a zero. In NEG (in position), the most negative input level is displayed as a one, and the most positive level is displayed as a zero.

**3-30. BYTE 4 BIT/3 BIT.** In the 4 BIT (BCD or hexadecimal format) position (out) display data is arranged into four-bit bytes. In the 3 BIT (octal format) position (in) display data is arranged into three-bit bytes.

## 3-31. BUS OPERATION.

**NOTE**

A Model 10236A Trigger Interface Cable and a Model 10237A I/O Interface Cable are required to bus the Model 1607A with a Model 1600A Logic State Analyzer.

3-32. There are two buses in the Model 1600A and Model 1607A. The Trigger Bus (TRIG BUS) is used to expand triggering capability and the I/O bus (I/O PORT) is used to transfer and control display information.

**3-33. TRIGGER BUS.** The trigger bus permits the Model 1607A and a Model 1600A to be connected together to form a 32 bit trigger word. Trigger-bus operation is controlled by the LOCAL/BUS switch. In LOCAL position, the instrument will trigger whenever the monitored data meets the instrument's local triggering requirements, regardless of the status of the other instrument on the bus. With LOCAL/BUS set to BUS, the instrument will generate a trigger only when the data monitored by both bused instruments is in agreement with their composite trigger word.

**3-34. I/O BUS.** Whenever the Model 1607A and Model 1600A are connected together with the I/O interface cable, they automatically go into I/O bus operation. In I/O bus operation, the combined instruments perform as a 32-bit logic state analyzer with table A data provided by the Model 1600A and table B provided by the Model 1607A. STORE A→B is disabled in I/O bus operation.

3-35. With the I/O bus connected, the combined instruments can be operated with either a single clock or two independent clocks. Using a single clock, the Model 1600A can display one table of sixteen 32-bit words or two tables of sixteen 16-bit words each. Thirty-two sequential 16-bit words can be displayed by setting LOCAL/BUS on both instruments to LOCAL and triggering the Model 1607A on the word occuring 16 clock pulses after the Model 1600A trigger word. With dual-clock operation, "handshake" operations between two independent machines can be observed on the same display with 16 channels devoted to each machine and independent clocks for each machine.

3-36. Model 1607A controls and indicators function in the same manner in I/O bus operation as they do when the Model 1607A operated separately with the following exception: The Model 1600A DISPLAY TIME controls both instruments in the bus mode. As shipped from the factory, the Model 1607A can be manually reset from the Model 1607A RESET button only. If it is desirable to control both the Model 1600A and the Model 1607A with the Model 1600A RESET, modify the Model 1607A Display Board Assembly A2 as detailed in Section V of this manual.

3-37. Detailed instructions for operating the instruments in the bus mode are provided in the Model 1600A Operating and Service Manual.

## 3-38. TURN-ON PROCEDURE.

**CAUTION**

Do not operate the Model 1607A with a storage oscilloscope. Turn off the oscilloscope or turn down intensity before turning off Model 1607A power. Otherwise the oscilloscope CRT could be burned.

3-39. An oscilloscope with external Z-axis, vertical and horizontal inputs as specified in table 1-1, or a Model 1600A Logic State Analyzer must be used to display Model 1607A data. Perform the following procedure to check Model 1607A operation with an oscilloscope. Model 1607A operation with a Model 1600A is described in the Model 1600A Logic State Analyzer Operating and Service Manual.

**NOTE**

Clock and Data probes need not be connected for this procedure.

a. Set oscilloscope controls to obtain defocused spot on the center on the CRT screen.

b. Connect vertical output of Model 1607A to vertical oscilloscope or display input and adjust oscilloscope for one volt/div sensitivity.

c. Connect Model 1607A horizontal and Z-axis outputs to oscilloscope or display external horizontal and Z-axis inputs.

d. Set Model 1607A controls as follows:

| | |
|---|---|
| POWER | OFF |
| Sample Mode | SINGLE |
| COLUMN BLANKING | full CCW |
| Z-AXIS | ON |

e. Apply power and adjust oscilloscope focus.

f. Adjust Model 1607A HORIZ SIZE for 6-division wide display and Model 1607A VERT SIZE for 8-division high display.

g. Center display with HORIZ POSN and VERT POSN controls.

h. Adjust Z-AXIS for blanking of trace between one's and zero's and complete blanking by COLUMN BLANKING control.

## 3-40. OPERATOR'S CHECKS AND ADJUSTMENTS.

3-41. The following procedure verifies the functional operation of the Model 1607A.

a. Perform the turn-on procedure detailed in paragraph 3-38. Observe that a focused 16-word table of ones and zeros is displayed.

b. Set Model 1607A controls as follows:

| | |
|---|---|
| OFF/WORD | WORD |
| TRIGGER WORD | all OFF |
| QUALIFIER Q0, Q1 | OFF |

c. Set BYTE to 3 BIT and observe that display format changes from four-bit bytes to three-bit bytes.

d. Set LOGIC to NEG and observe that all zeros change to ones, and that all ones change to zeros.

e. Rotate COLUMN BLANKING cw and observe that vertical columns are blanked starting with most significant bit (MSB).

f. Rotate COLUMN BLANKING fully cw and observe that least significant bit (LSB) column remains on CRT.

g. Rotate COLUMN BLANKING fully ccw.

h. Set Trigger Mode to START DSPL and observe that first word is intensified.

i. Set Trigger Mode to END DSPL and observe that last word is intensified.

j. Set DELAY ON/OFF to ON. Observe that setting DELAY thumbwheels from 0 to 15 will move the word on the display. Observe that intensified word is not displayed for delays greater than 15.

## 3-42. OPERATING PROCEDURE.

3-43. The Model 1607A operating procedure is provided in a flow-diagram format in figure 3-2.

1. CONNECT MODEL 1607A HORIZ, VERT AND Z-AXIS OUTPUTS TO OSCILLOSCOPE EXTERNAL HORIZONTAL, VERTICAL AND Z-AXIS INPUTS.

2. ADJUST OSCILLOSCOPE FOR 1 VOLT/DIV SENSITIVITY AND ADJUST MODEL 1607A HORIZ SIZE, VERT SIZE, AND Z-AXIS ADJUSTMENTS FOR 6-DIVISION WIDE BY 8-DIVISION HIGH DISPLAY WITH TRACES BETWEEN ONE'S AND ZERO'S BLANKED. CENTER DISPLAY USING POSN CONTROLS.

3. CONNECT CLOCK AND DATA MONITOR PROBES TO CIRCUITRY UNDER TEST.

4. SELECT CLOCK SLOPE.

SET CLOCK (42) TO MATCH CLOCK PULSE SLOPE REQUIREMENTS OF CIRCUITRY UNDER TEST: OUT POSITION FOR POSITIVE-EDGE TRIGGERING, IN POSITION FOR NEGATIVE-EDGE TRIGGERING.

5. SELECT THRESHOLD.

SET THLD (39) TO MATCH THRESHOLD OF CIRCUITRY UNDER TEST. SELECT TTL WHEN LOGIC THRESHOLD IS +1.5 V. FOR OTHER THRESHOLD LEVELS, SELECT VAR AND ADJUST SET TO THRESHOLD OF SYSTEM UNDER TEST USING DVM CONNECTED TO MEAS OR ADJUST SET TO CENTER OF RANGE WHERE NO CLOCK LIGHT IS OUT.

6. ADJUST DISPLAY TIME AND COLUMN BLANKING CONTROLS FULLY CCW.

7. SELECT SAMPLE MODE.

| REPET 27 | SINGLE 27 | RESET 28 |
|---|---|---|
| SELECT REPET TO RESET THE DISPLAY REPETITIVELY AT A RATE SELECTED BY DISPLAY TIME. AFTER RESET NEW DATA IS THEN DISPLAYED WHEN THE SYSTEM UNDER TEST MEETS TRIGGERING REQUIREMENTS. | SELECT SINGLE TO CAUSE MODEL 1607A TO ACQUIRE AND DISPLAY ONE 16-WORD BLOCK OF DATA EACH TIME RESET IS DEPRESSED. | PUSH RESET TO CAUSE THE MODEL 1607A TO IMMEDIATELY RETURN TO THE BEGINNING OF A DATA ACQUISITION CYCLE. |

8. SELECT TRIGGER MODE.

| DELAY 29 | DELAY ON/OFF 30 | START DSPL 31 | END DSPL 32 | NORM/ARM 32 | LOCAL/BUS 34 | WORD 35 |
|---|---|---|---|---|---|---|
| SET NUMBER OF CLOCK PULSES DISPLAY AND DELAYED TRIG OUT ARE TO BE DELAYED FROM SELECTED TRIGGER WORD. IN START DSPL MODE, START OF DISPLAY IS DELAYED FROM TRIGGER WORD BY DELAY SETTING. IN END DSPL MODE, END OF DISPLAY IS DELAYED FROM TRIGGER WORD BY DELAY SETTING. | SELECT IN POSITION TO TURN DELAY GENERATOR ON. OFF POSITION HAS SAME EFFECT AS SETTING ALL DELAY THUMBWHEEL SWITCHES TO ZERO. | SELECT START DSPL TO DISPLAY TRIGGERING WORD (POSITIONED AT TOP OF DISPLAY) AND FOLLOWING 15 INPUT DATA WORDS. | SELECT END DSPL TO DISPLAY TRIGGERING WORD (POSITIONED AT BOTTOM OF DISPLAY) AND PRECEDING 15 INPUT DATA WORDS. | SELECT NORM TO ALLOW TRIGGER GENERATOR TO PRODUCE A TRIGGER WHENEVER THE TRIGGER WORD AND QUALIFIER CONDITIONS ARE MET. SELECT ARM TO INHIBIT TRIGGER GENERATOR FROM PRODUCING A TRIGGER UNTIL IT HAS BEEN ARMED BY A POSITIVE-GOING TRANSITION ON THE TRIG ARM INPUT. | SELECT LOCAL TO OBTAIN A TRIGGER ANYTIME THE MODEL 1607A INPUT DATA MEETS TRIGGERING REQUIREMENTS. SELECT BUS WHEN THE MODEL 1607A IS TO BE USED WITH A MODEL 1600A. IN BUS, A TRIGGER IS GENERATED ONLY WHEN THE TRIGGER REQUIREMENTS ARE MET ON BOTH BUSSED INSTRUMENTS. | SELECT ON POSITION TO ENABLE TRIGGER WORD SWITCHES. THE OFF POSITION EFFECTIVELY PLACES ALL TRIGGER WORD SWITCHES IN THE OFF OR DON'T CARE POSITION. |

9. SELECT TRIGGER WORD.

SET SWITCHES TO MATCH REQUIRED TRIGGERING WORD OF INPUT DATA STREAM. HI TO RECOGNIZE A POSITIVE LOGIC STATE, LO TO RECOGNIZE A NEGATIVE LOGIC STATE OR OFF FOR A NON-REQUIRED INPUT.

10. SELECT QUALIFIER MODE.

| DSPLY 37 | TRIG 37 |
|---|---|
| SELECT DSPLY (OUT POSITION) TO SELECTIVELY ACCEPT CLOCKS. WHEN THE TWO-BIT QUALIFIER CONDITION IS MET, THE INPUT CLOCK FROM THE CIRCUIT UNDER TEST IS RECOGNIZED. IF QUALIFIER CONDITION IS NOT MET, THE MODEL 1607A IGNORES THE CLOCKS FROM THE CIRCUIT UNDER TEST. THE DSPLY QUALIFIER ALLOWS COMPRESSION OF DATA FOR DISPLAY. | SELECT TRIG (IN POSITION) TO USE QUALIFIER AS EXTERNAL SYNCHRONOUS TRIGGER OR TO EXPAND THE LENGTH OF THE TRIGGER RECOGNITION WORD TO 18 BITS. |

11. SELECT QUALIFIER.

SET QUALIFIER SWITCHES Q1 and Q2 TO MATCH REQUIRED TRIGGERING BITS OF INPUT DATA. HI TO RECOGNIZE A POSITIVE LOGIC STATE, LO TO RECOGNIZE A NEGATIVE LOGIC STATE, OR OFF FOR A NON-REQUIRED INPUT.

12. SET UP DISPLAY FEATURES.

| DISPLAY TIME 17 | COLUMN BLANKING 18 | LOGIC POS/NEG 19 | BYTE 4 BIT/3 BIT 20 |
|---|---|---|---|
| ADJUST FOR MAXIMUM USABLE FLICKER RATE. | ADJUST TO BLANK OUT NON-REQUIRED VERTICAL COLUMNS. | SET TO POS TO DISPLAY MOST POSITIVE INPUT LOGIC LEVEL AS A 1. SET TO NEG TO DISPLAY MOST NEGATIVE INPUT LOGIC LEVEL AS A 1. | SELECT 4 BIT (OUT POSITION) TO DISPLAY 4-BIT BYTES. SELECT 3-BIT (IN POSITION) TO DISPLAY 3-BIT BYTES. |

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*Figure 3-2.*
*Model 1607A Operating Procedure*

# SECTION IV

# PRINCIPLES OF OPERATION

## 4-1. INTRODUCTION.

4-2. This section of the manual is divided into three major parts: (1) a functional description of the Model 1607A based on a simplified instrument algorithm and functional algorithms of the major sections of the Model 1607A, (2) a functional block diagram description, and (3) a detailed circuit theory of operation.

4-3. The simplified algorithm presents the Model 1607A in its most basic form. The functional algorithms explain the operation of each section of the instrument. The functional block diagram description describes the purpose of each block on the block diagram (figure 8-4). Detailed block diagrams are included to help explain how each block functions. The detailed circuit description is limited to circuits that are unique or unusually complicated. No attempt is made to explain basic circuits.

## 4-4. BASIC INFORMATION.

4-5. The following paragraphs explain logic conventions that are used in describing the Model 1607A principles of operation.

**4-6. LOGIC STATES.** The terms HI and LO describe the output states of logic circuit elements. HI indicates the most positive dc level and LO indicates the most negative dc level produced by a given circuit element.

**4-7. LOGIC CIRCUITRY.** Most integrated circuits in the Model 1607A are in the TTL (transistor-transistor logic) and CMOS (complementary metal-oxide semiconductor) families of digital devices. A LO output from a TTL device is <+0.4 V and a HI output is >+2.5 V. A LO output from a CMOS device in the Model 1607A is approximately 0 V and a HI output is approximately +5.0 V.

**4-8. MNEMONICS.** A mnemonic is a brief letter designator symbol that describes the active state and function of a signal line. A prefix letter (H, L, P or N) indicates the active state of the signal; the remaining letters indicate its function. An H prefix indicates the function is active in the HI state, and an L prefix indicates the function is active in the LO state. For edge-controlled devices, the prefix P indicates the function is active on the positive-going transition, and the prefix N indicates the function is active on the negative-going transition.

4-9. Mnemonic functional definitions and points of origin are listed alphabetically in table 4-1.

## 4-10. FUNCTIONAL DESCRIPTION.

4-11. Figure 4-1 presents the functional sequence of events within the Model 1607A. The 1607A alternates between a data acquisition cycle and a display cycle.

4-12. During the data acquisition cycle, each word of input data is temporarily stored before being loaded into the memory. The input data (after temporary storage) is compared with the front-panel TRIGGER WORD switch positions. When an input word matches the preset TRIGGER WORD and trigger arming, bus, and qualifier conditions are met, the Model 1607A performs a data acquisition algorithm. The operation of the data acquisition algorithm is determined by the display and trigger modes selected. The algorithm controls memory loading and determines when gathered data is ready for display. When all algorithmic requirements have been satisfied, HDR occurs and transfers the Model 1607A into a display cycle.

4-13. The display cycle begins with the occurrence of HDR. Information stored in the memory during the previous data acquisition cycle is read out and displayed one word at a time. At the end of each displayed word, the Model 1607A increments to the next data word position on the CRT. This process continues until the end of the sixteenth displayed word. At the end of the sixteenth word, the Model 1607A checks the SAMPLE MODE selected and the DISPLAY TIME control setting to determine if new data is required. When new data is not required, the display cycle repeats. When new data is required, LRST occurs. The occurrence of LRST transfers the Model 1607A into a data acquisition cycle.

**4-14. DIGITAL DELAY AND TRIGGER GENERATOR.** The functional operation of the digital delay and trigger generator circuitry is shown in figure 4-2. The AND of trigger word recognition with qualifier recognition and LΔT produce HBTRG and HLTRG. HBTRG and HLTRG are applied to the bus and local flip-flops.

4-15. The bus and local flip-flops are enabled by LARM and HARM from the trigger arm flip-flop. When the ARM trigger mode is selected, an external arming signal is required to clock LARM and HARM true. When the NORM trigger mode is selected, LARM and HARM are held in the true state. With LARM and HARM true, the occurrence of HBTRG and HLTRG force the $\overline{Q}$ outputs of the bus and local flip-flops HI, generating HB and HL. HB and HL enable the delay

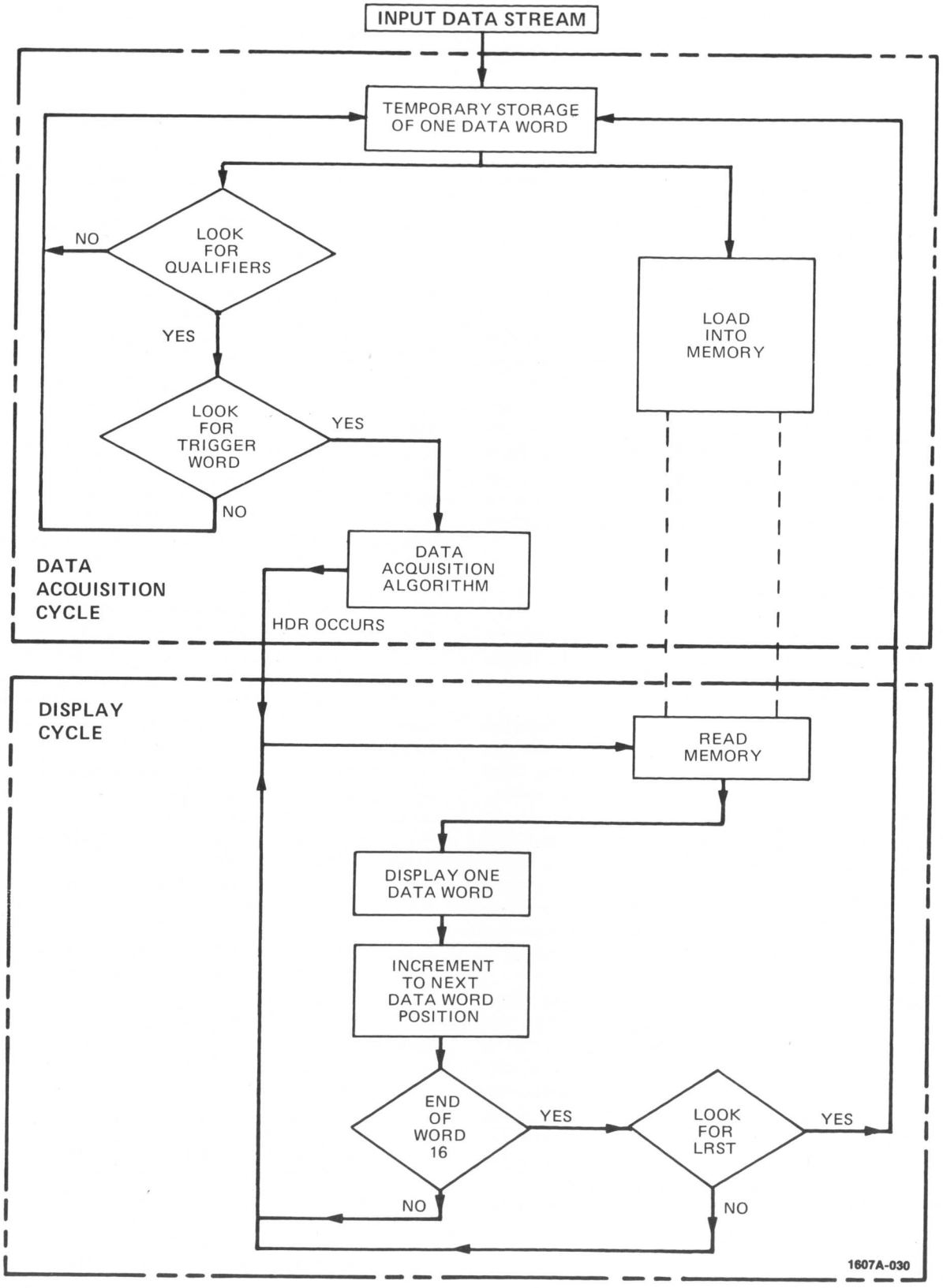



*Figure 4-1. Functional Sequence of Events*

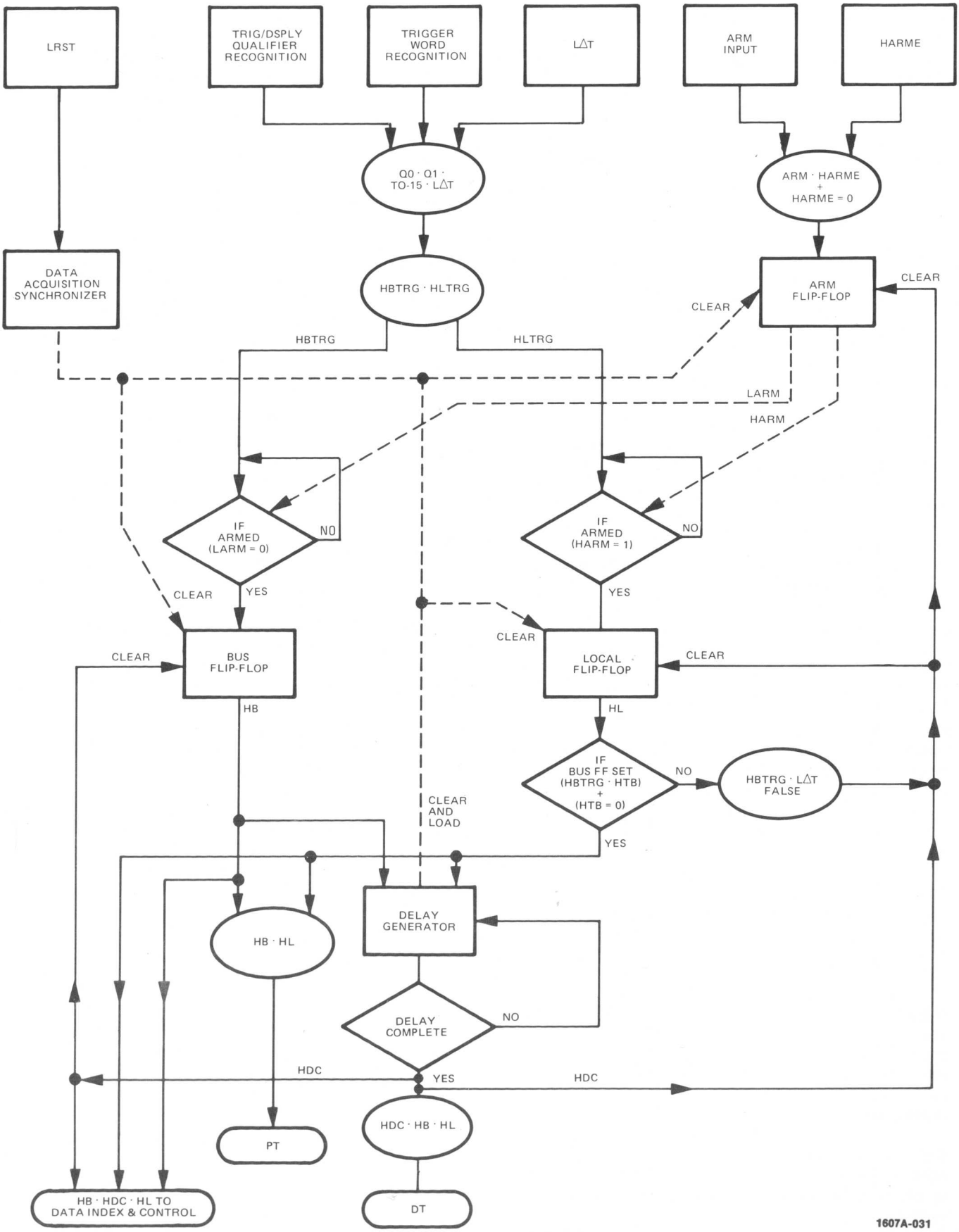



*Figure 4-2. Digital Delay/Trigger Generator Algorithm*

generator and their AND generates the pattern trigger output (PT). If HB is false (bus flip-flop not set), the local and arm flip-flops are cleared and the Model 1607A waits for the next trigger word.

4-16. Once enabled, the delay generator counts out the delay set on the DELAY thumbwheels. When the delay is complete, HDC goes true. The AND of HDC with HB and HL generates the delayed trigger output (DT). In addition, HDC is used to clear the local, arm, and bus flip-flops on the occurrence of LRST.

**4-17. DATA INDEX AND CONTROL.** Figure 4-3 shows the functional operation of the data index and control circuit. The data index and control circuit controls the read and write functions of the memory and determines when a data acquisition cycle is complete.

4-18. When the start display mode is selected, the occurrence of the trigger word and the subsequent completion of the delay (HB • HL • HDC) set the start flip-flop. The outputs of the start flip-flop are LTRG and HTRG*. LTRG is inverted (HTRG) and used as a control signal for the blanking circuit. HTRG* enables the data index counter. Once enabled, the data index counter counts the number of words written into memory. When the count reaches terminal count (16 words written into memory), HTC goes HI setting the end flip-flop. Setting the end flip-flop generates HDR, initiating a display cycle.

4-19. When the end display mode is selected, HSTR is LO, which sets the start flip-flop. The data index counter is enabled. When terminal count is reached, HTC goes HI and remains in that state. Since the trigger word has not been detected, data words continue to refresh the memory with the current input data word being written into the bottom of memory and the oldest word being bumped out the top. When the trigger word is detected and the delay generator counts out, HB•HL•HDC•HTC sets the end flip-flop initiating a display cycle.

**4-20. DISPLAY CYCLE.** The functional operation of the display section is shown in figure 4-4. At the end of a data acquisition cycle, HR1•$\overline{\text{HNCQ}}$ generates HDSPR which resets the horizontal and vertical state counters. The horizontal state count addresses each bit of the current word, displaying it on the CRT. If the trigger word is currently being displayed, the intensity counter is enabled, causing the current word to be written four times, resulting in that word being intensified. Once a word is written, the vertical counter is incremented to the next word address and the cycle is repeated.

4-21. At the end of word sixteen, the instrument checks the selected sample mode. If the Model 1607A is set to SINGLE, it increments the horizontal and vertical state counters, and rewrites the same data. If the Model 1607A is set to REPET, it checks display time. If display time is not complete, the instrument again increments the horizontal and vertical counters and rewrites the same data. When display time is complete, or when the RESET button is pressed, LRST goes LO, initiating a data acquisition cycle. At the same time, HDSPR goes HI, resetting the horizontal- and vertical-state counters and blanking the CRT during the data acquisition cycle.

## 4-22. BLOCK DIAGRAM.

4-23. The Model 1607A block diagram is shown on figure 8-4. Heavy lines enclose circuitry contained on a numbered schematic. The Model 1607A contains two major sections: (1) a data acquisition section and (2) a display section. The data acquisition section consists of circuitry shown on schematics 3 through 10. The display section circuitry is shown on schematics 11 through 15.

### 4-24. DATA ACQUISITION SECTION.

**4-25. Data Input. (See figure 4-5.)** Inputs to the Model 1607A are supplied by a clock probe and three data probes. The input threshold level for the clock and data probes is provided by the Model 1607A threshold supply. With TTL selected, the threshold level is fixed at +1.5 V. With VAR selected, the threshold level is variable from —10 V to +10 V by VAR SET. Clock Select supplies two clock slope commands (SS and SI) to the clock probe. These commands, controlled by the CLOCK pushbutton, determine which transition of the input clock signal transfers input data into the Model 1607A.

4-26. The clock probe supplies two buffered inputs: PCLK and NCLK. The leading-edge transitions of PCLK and NCLK are synchronous with data inputs from the data probes. When CLOCK is out (⎍), the leading-edge transition of PCLK is a positive-going transition, and the leading-edge transition of NCLK is a negative-going transition. With these conditions, data is clocked into the Model 1607A on the positive-going transition of the input clock signal. When CLOCK is in (⏉), the leading-edge transition of PCLK is a negative-going transition, and the leading-edge transition of NCLK is a positive-going transition. With CLOCK in (⏉), data is clocked on the negative-going transition of the input clock signal. PCLK transfers input data into temporary storage and is used by the timing generator to derive the internal data acquisition clocking signals. NCLK clocks the NO CLOCK indicator control logic.

**4-27. Temporary Data Storage.** Input data from the data probes is applied to a series of D flip-flops for temporary storage. The flip-flop outputs are the data word and its complement (T0 through T15 and $\overline{\text{T0}}$ through $\overline{\text{T15}}$), and the two qualifier bits and their complements (TQ0/TQ1 and $\overline{\text{TQ0}}$/$\overline{\text{TQ1}}$). The rising edge of PCLK loads new data into the temporary

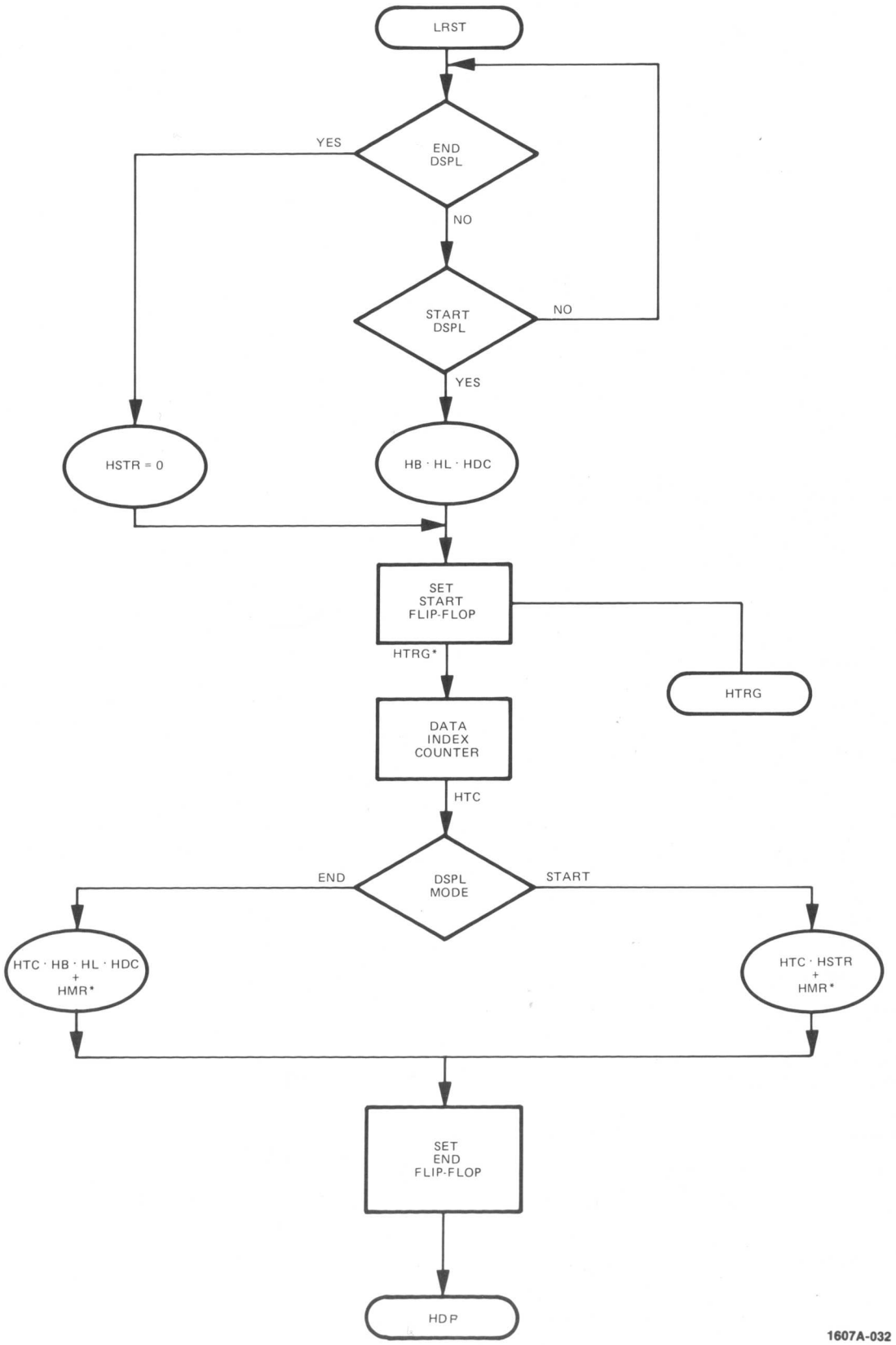



*Figure 4-3. Data Index and Control Algorithm*

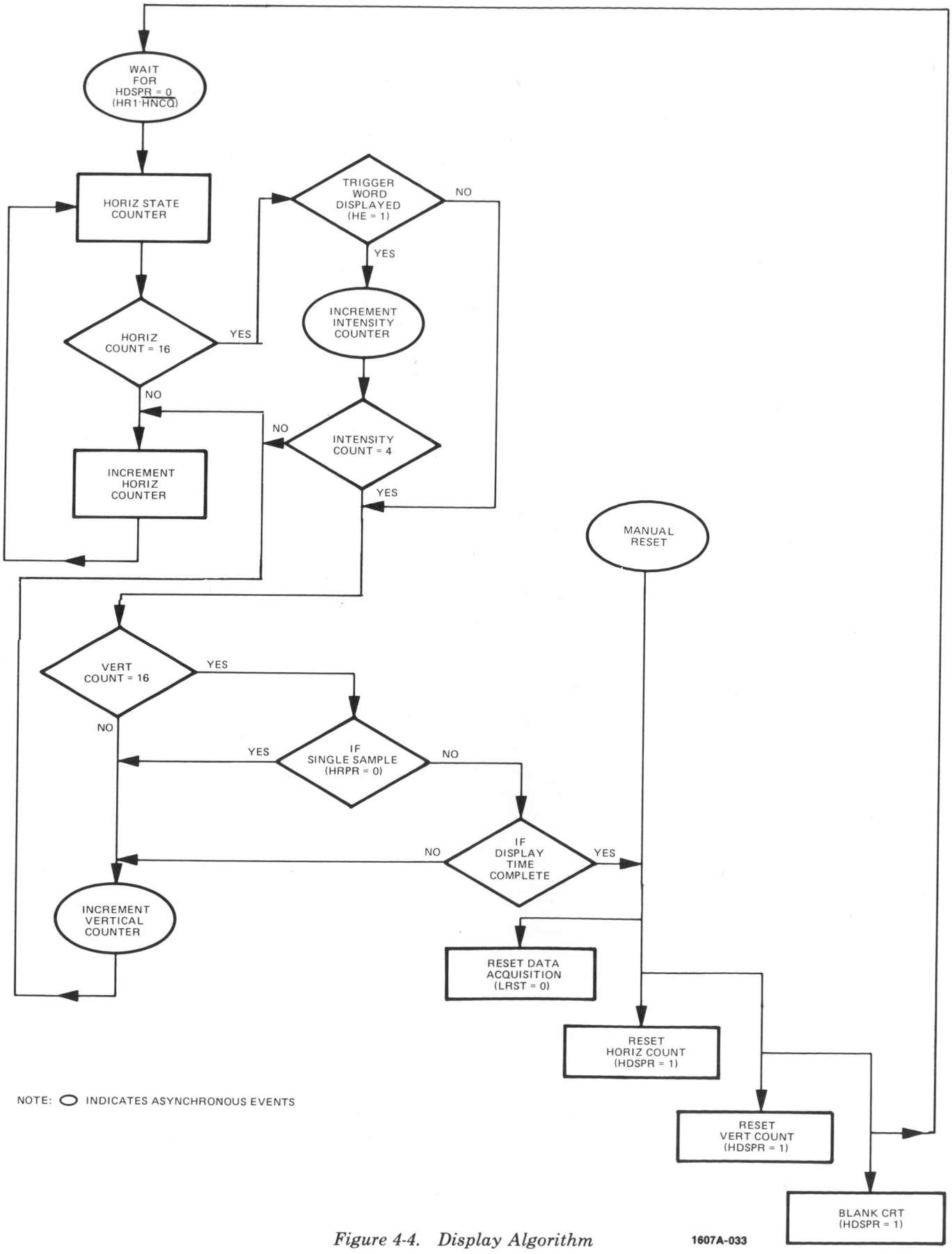



*Figure 4-4. Display Algorithm* 1607A-033

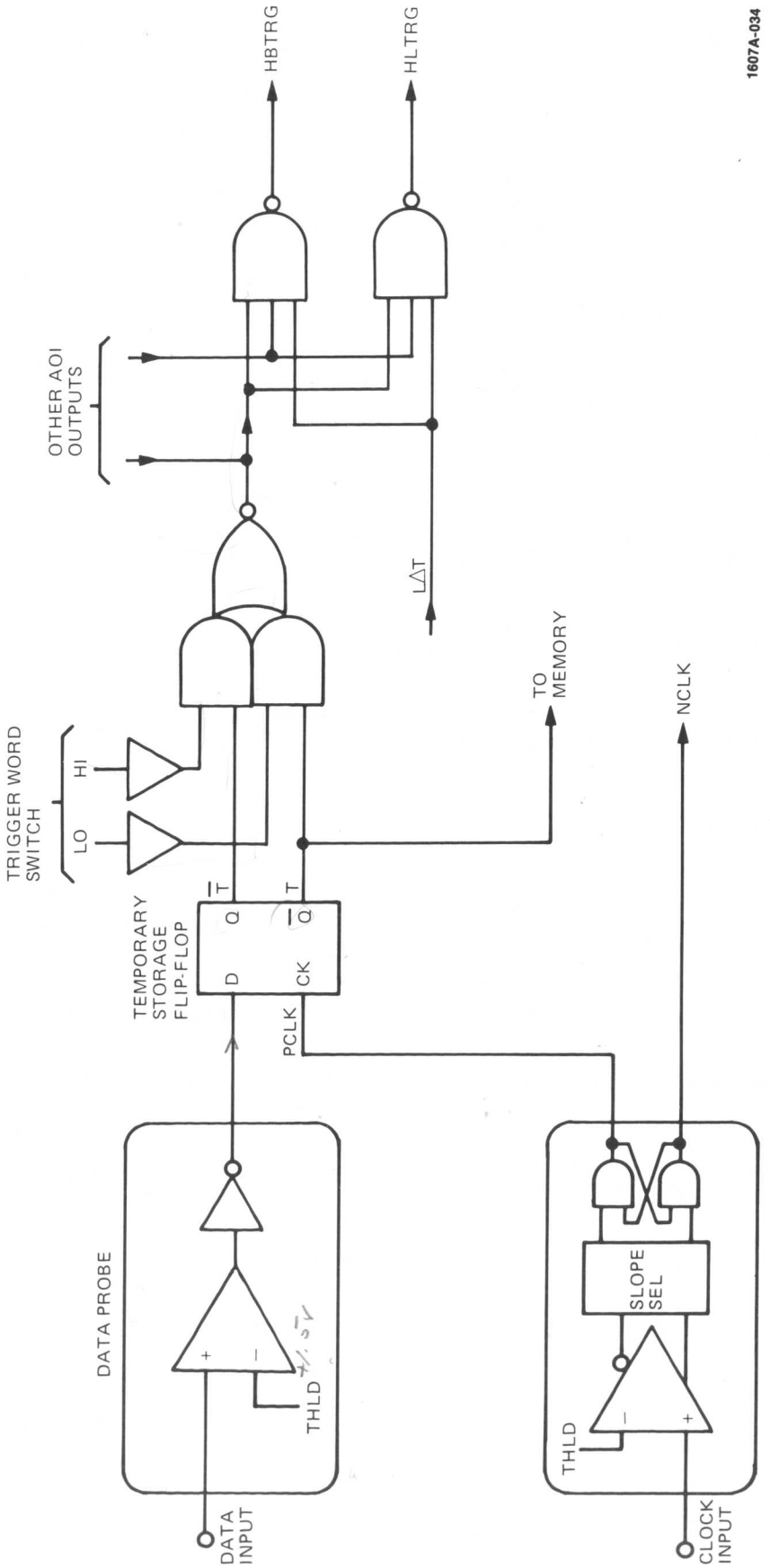



*Figure 4-5. Data Input, Temporary Storage, and Pattern Recognition*

storage flip-flops. The outputs of the D flip-flops are connected to the pattern recognition gates and A-memory.

**4-28. Pattern Recognition.** The pattern recognition gates compare the TRIGGER WORD and QUALIFIER switch settings with the input data and qualifier lines. When a match occurs, HBTRG and HLTRG (enabled by LΔT) are produced. HBTRG is wire ANDED with the trigger bus. Thus, all inputs to the bus must be high before HBTRG will rise above threshold. When DSPLY qualifier mode is selected, the pattern recognition circuit generates HCLQ which is used to qualify timing signals in the Model 1600A.

**4-29. Digital Delay and Trigger Generator. (See figure 4-6.)** Once pattern recognition occurs, HLTRG is clocked into the local flip-flop. If BUS trigger mode is selected, the rising edge of HBTRG sets the bus flip-flop. When both flip-flops are set, HB and HL generate the pattern trigger (PT) and enable the delay generator. If the delay generator is set to zero, PT and DT (delayed trigger) are generated when the local and bus flip-flops are set. For delays other than zero, PT goes HI when the bus and local flip-flops are set and remains HI while the delay generator is running. When the delay has timed out, HDC occurs. DT is generated by HDC and PT is terminated. The delay generator and local flip-flop clock are qualified so that a trigger is recognized only when qualifier conditions are met.

4-30. When trigger arming is selected, the arm flip-flop disables the local and bus flip-flops until an arming pulse is received. Once an arming pulse is received, the local and bus flip-flops are enabled. When trigger and qualifier conditions are met, PT is generated, and the arm flip-flop is reset.

**4-31. Memory/Multiplexer and Data Index and Control. (See figure 4-7.)** When the display section generates LRST, a data acquisition cycle is initiated. The data index counters, and the start and end flip-flops are reset. When a qualified clock is detected, the memory address lines are switched to the write address counter and a memory write enable pulse (LWE) is generated. While LWE is true, one word is written in memory. At the trailing-edge of LWE, the write address counter is incremented and the memory address lines are switched back to the display or computed address (CA0-3).

4-32. With the start display mode selected, the data index counter is incremented by LWE2 only after the start flip-flop is set. The start flip-flop is set when a trigger word is detected and the digital delay is complete. When the data index counter reaches terminal count, the end flip-flop generates HDR. HDR indicates that memory data is complete and initiates a display cycle.

4-33. With the end display mode selected, the start flip-flop is preset enabling the data index counter to

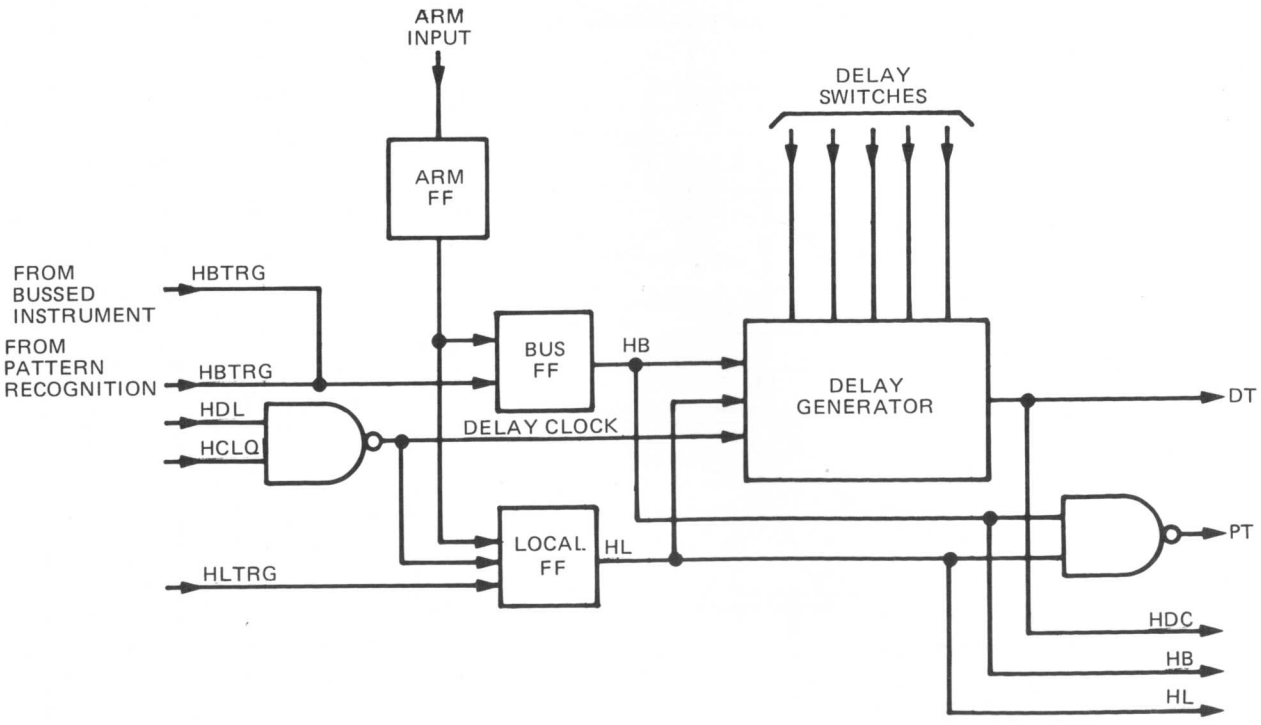



*Figure 4-6. Digital Delay/Trigger Generator Block Diagram* 1607A-035

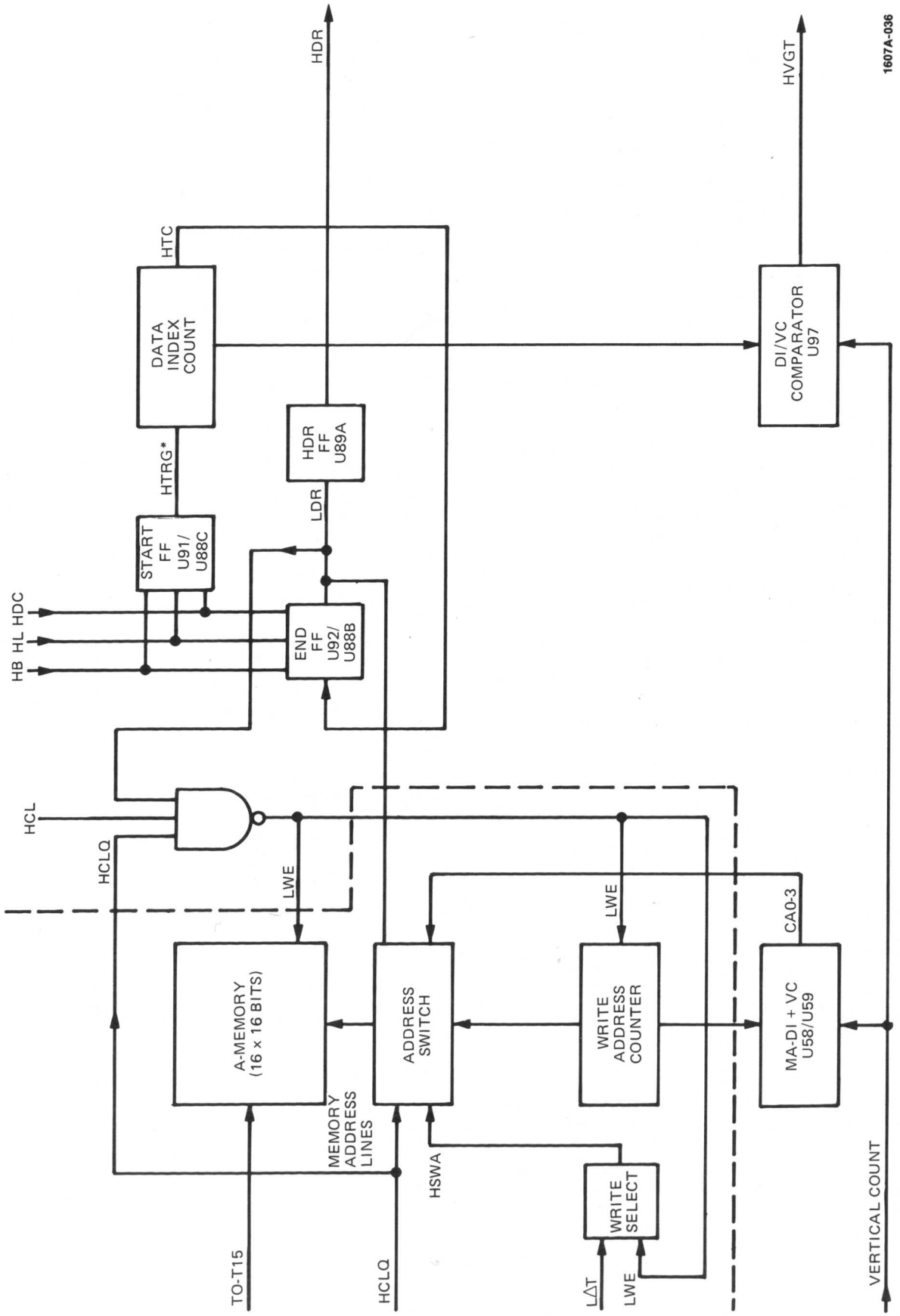



*Figure 4-7. Memory and Data Index/Control Block Diagram*

run prior to trigger word recognition. When the data index counter reaches terminal count, the end flip-flop is enabled to receive a trigger. The occurrence of a trigger after terminal count is reached generates HDR, which initiates a display cycle.

4-34. The data index counter keeps track of the number of valid words written into memory. The write address counter points to the next address in memory to be written into. The difference of the output of the two counters is taken in U58 to determine where the first word in memory is located. This computed first word address is added to the vertical state count from the display section to determine the address of the words to be read from memory during a display cycle.

3-35. Whenever the qualified clock rate drops below 30 Hz during a data acquisition cycle, the partial display mode is enabled. The vertical state counter reads partial memory data through U58/U59 and U97. When the vertical state count exceeds the data index count, i.e. addresses invalid data, comparator U97 provides HVGT to the display section. HVGT blanks the CRT so that only valid data is displayed.

**4-36. Timing Generator.** The timing generator develops four internal clocking signals in the Model 1607A based on the clock from the system under test. HCL is gated in the memory index control circuit to derive the write enable pulse (LWE). HDL is the clock for the delay generator. LΔT clocks the pattern recognition circuit and HΔT is used to clock the reset circuit for the local flip-flop in the trigger generator.

**4-37. Indicator Light Control.** The indicator light control logic provides a hierarchy that determines the sequence in which the indicator lights are enabled. When the NO CLOCK light is on, the NO QUAL and NO TRIG lights are disabled. When a clock is present and the NO QUAL light is on, NO TRIG is disabled. The NO ARM light also disables the NO TRIG light. Otherwise, the NO ARM light functions independently of the other lights.

4-38. The indicator light logic also provides HNCQ to the display section. When the qualified clock rate is less than 30 Hz, HNCQ places the display section in the partial display mode.

**4-39. DISPLAY SECTION.** The display section of the Model 1607A contains the circuitry required to generate horizontal, vertical and blanking drive to an oscilloscope CRT. These output signals provide information that positions the CRT electron beam and also determines whether a one or a zero is displayed. Data words are displayed from top to bottom, with specific bits displayed from right to left (least-significant bit to most-significant bit).

4-40. The horizontal and vertical drive circuits are synchronized together during a display cycle. When a display cycle begins, both the horizontal and vertical circuits are enabled and data is applied to the CRT. When the first data word has been displayed, the vertical circuitry moves the CRT electron beam to the second word position and the next data word is displayed. This process continues until the end of the sixteenth data word. If new data is required, LRST occurs and a new data acquisition cycle is initiated. If new data is not required, the memory contents are re-read and displayed as required.

**4-41. Display Control and Reset.** Figure 4-8 shows a functional block diagram of the display control and reset circuit. This portion of the display section consists of the reset circuit, the horizontal and vertical state counters, the word intensity control, and the circuitry for generating LZER which controls the one/zero switch.

4-42. At the end of a data acquistion cycle, HDR initiates a display cycle. HDR enables the vertical state counter which has been cleared previously by HDSPR. The vertical state counter counts the horizontal carry outputs (LHORC) from the horizontal state counter. The horizontal state counter outputs (H0-H3) address each bit of the current word addressed by the vertical state counter. The horizontal- and vertical-state counts are applied to a D/A converter to generate the horizontal and vertical drives for the CRT. When one complete word is written on the CRT, the horizontal-state counter generates LHORC. LHORC increments the vertical-state counter to the next word position and the cycle is repeated.

4-43. If the current word addressed by the vertical state counter is the trigger word (HE is true), the word intensity control logic inhibits LHORC's to the vertical state counter and enables the word intensify counter. The word intensify counter then counts LHORC's. At the count of four, Q3 of the word intensify counter goes HI, once again enabling LHORC's to the vertical state counter. This operation results in the trigger word being written on the CRT four times causing that word to be intensified.

4-44. When the last word is written on the CRT, the vertical state counter generates LVRTC. LVRTC is routed to the repetitive reset circuit, enabling that circuit. The repetitive reset circuit is controlled by the DISPLAY TIME control. When the repetitive reset circuit times out, HRPR is generated. If the repetitive sample mode is selected, the AND of HRPR with HRPS generates LRST. LRST switches the Model 1607A into a data acquisition cycle and forces HDSPR HI which resets the display section. If the Model 1607A is in the single sample mode, the display cycle is repeated until manually reset.

4-45. When the Model 1607A is connected to a Model 1600A through the I/O bus, the display cycle is controlled by the Model 1600A. In I/O bus operation, H1600 transfers control of the horizontal and vertical

state counters and the repetitive reset function to the Model 1600A. The horizontal and vertical state counts are then parallel loaded from the Model 1600A. The Model 1607A display section can be reset by the Model 1600A repetitive reset, the Model 1600A manual reset (after special modification), or the Model 1607A manual reset in the bus mode.

**4-46. Clock Generator and Analog Circuitry.** The clock generator and analog circuitry consists of the horizontal and vertical drive circuitry and the 100-kHz oscillator used for character generation. Figure 4-9 is a functional block diagram of the clock generator and analog circuitry.

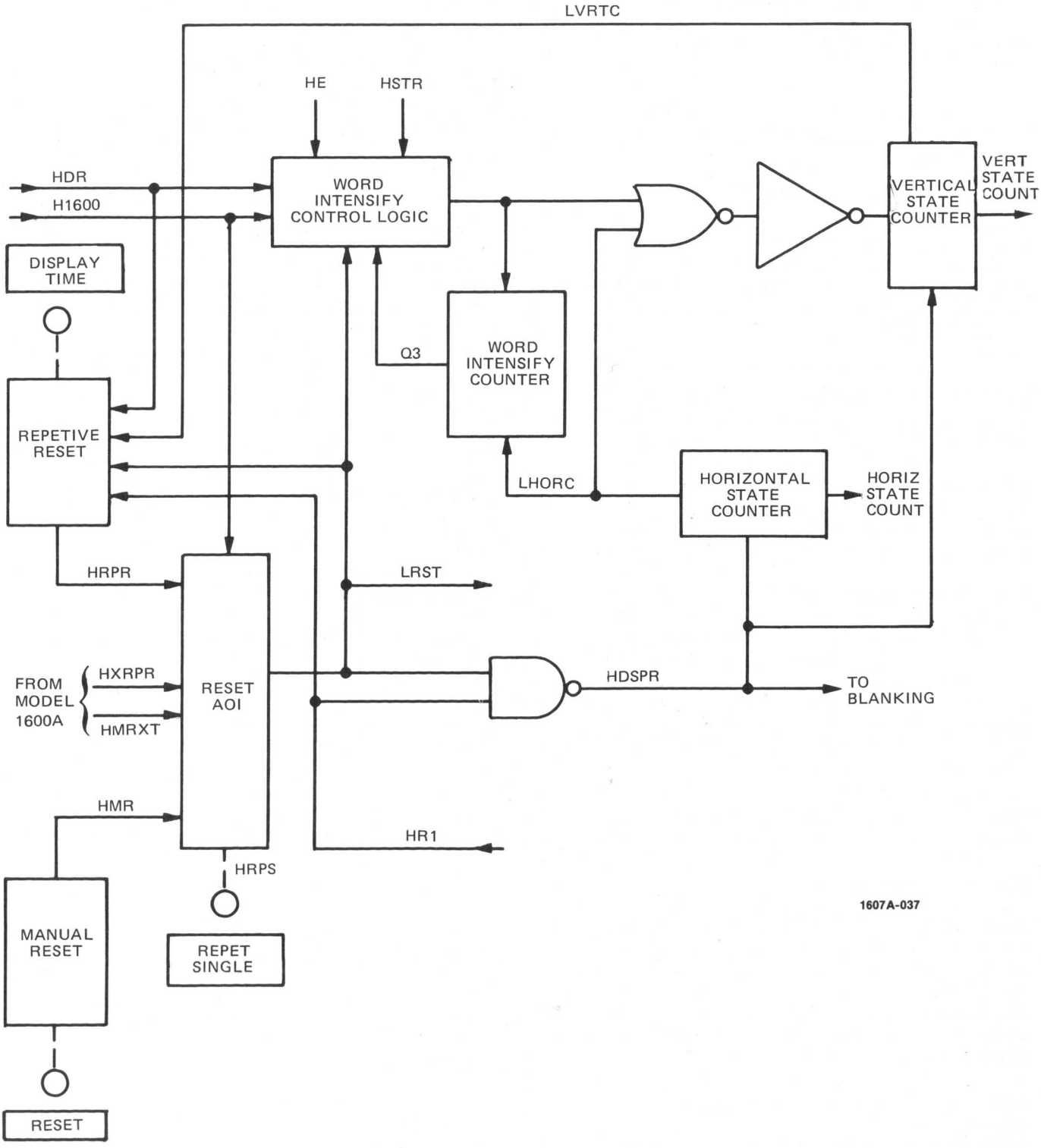



*Figure 4-8. Display Reset and Control Block Diagram*

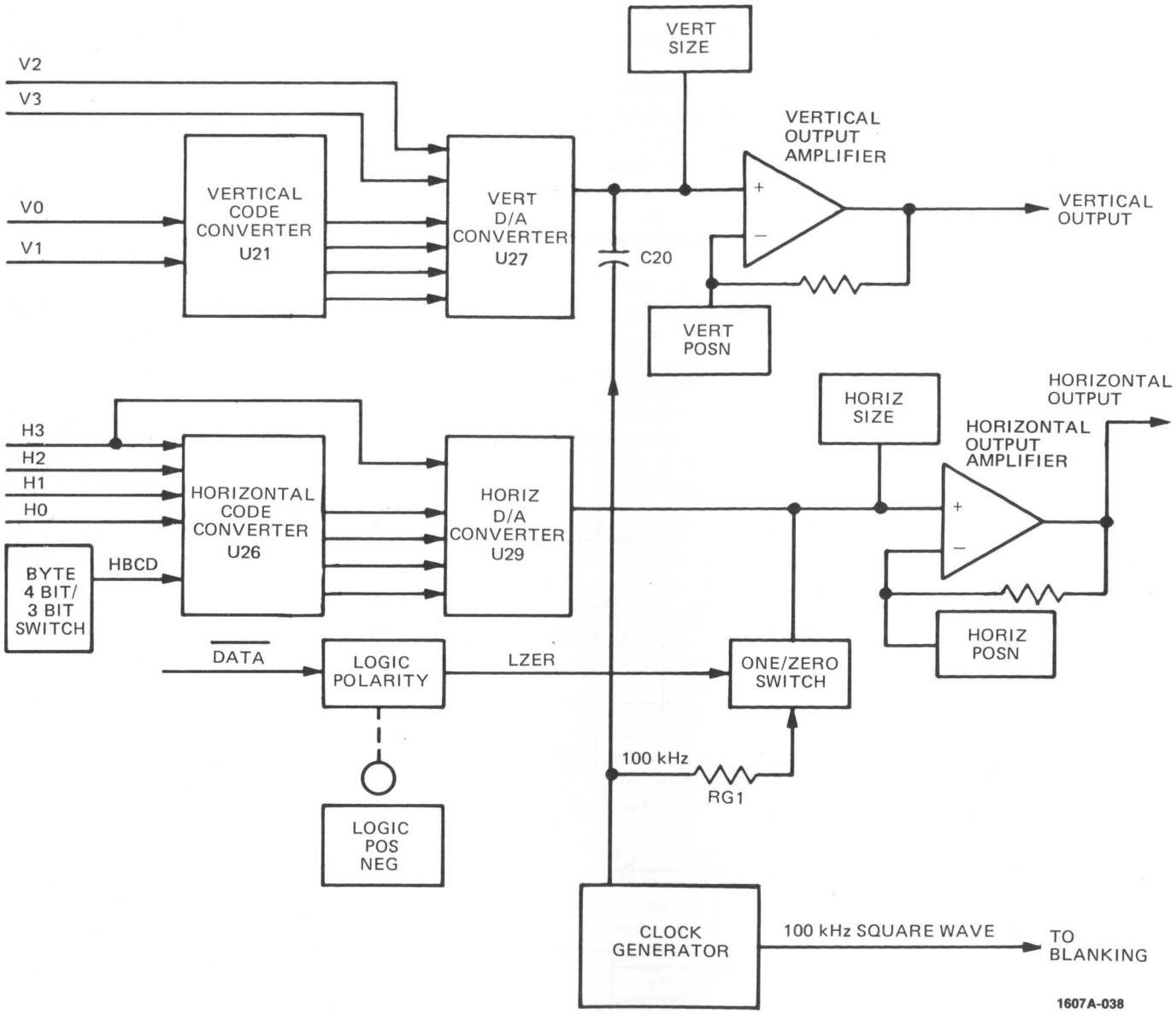



*Figure 4-9. Clock Generator and Analog Circuit Block Diagram*

4-47. The vertical drive circuitry is composed of the vertical code converter, D/A converter, and output amplifier. V0 and V1 of the vertical state count are applied to the code converter which is a two-input multiplexer. The code converter coverts V0 and V1 to a series of 16 4-bit coded words. The multiplexer output words, together with V2 and V3, are converted by the vertical D/A converter to produce a sixteen-position, staircased, vertical-drive voltage ramp. 100 kHz is superimposed on the vertical ramp for character generation. C20 provides 90 degrees of phase shift with respect to the horizontal 100-kHz sine-wave to generate Lissajous figures.

4-48. The vertical-drive voltage ramp drives an internally-compensated operational amplifier to produce the vertical-drive output. VERT SIZE determines the gain of the amplifier, and thus the vertical size of the characters. VERT POSN provides a variable offset on the output signal that determines the vertical position of the display.

4-49. The horizontal drive circuitry consists of the horizontal code converter (a read-only memory), D/A converter, one/zero switch, and output amplifier. The horizontal state count (H0-H3) and HBCD are applied to the horizontal code converter ROM. The code converter converts H0 through H3 and HBCD to a series of 16 4-bit coded words. HBCD determines the format of the displayed word. When HBCD is HI, the word is displayed in four 4-bit bytes. When HBCD is LO, the word is displayed in five 3-bit bytes with the most-significant bit left over.

4-50. The ROM output words, along with H3, are converted by the horizontal D/A converter to produce

a sixteen-step, staircased, horizontal-drive voltage ramp. 100 kHz is superimposed on the horizontal ramp through the one/zero switch. The one/zero switch is a CMOS transmission gate controlled by LZER. LZER is derived from $\overline{\text{DATA}}$ from the memory/multiplexer circuitry. When an input data bit is to be displayed as a zero, LZER is LO, enabling the 100-kHz sine wave to be superimposed on the horizontal ramp. When an input data bit is to be displayed as a one, LZER is HI inhibiting the application of the 100-kHz sine wave to the horizontal ramp. For each step of the vertical ramp, one sixteen-step horizontal ramp is produced. The horizontal voltage ramp drives an internally compensated operational amplifier identical to the vertical output amplifier. The aspect ratio of the displayed characters (height to width) is determined by R61.

**4-51. Blanking.** Figure 4-10 is a block diagram of the blanking circuit. The blanking select gate is controlled by a combination of inputs. The column blanking circuit converts the horizontal state count to a dc voltage by means of a discrete D/A converter. The dc voltage is proportional to the bit location in the displayed word. This voltage is compared with the COLUMN BLANKING setting to determine if the bit should be blanked. The column blanking circuit is either HI, indicating the column is to be blanked, or LO indicating the column is to be displayed. The least-significant bit cannot be blanked.

4-52. Another input to the blanking select gate is CLOCK. CLOCK goes HI for two clock generator intervals whenever LHORC occurs. The HI level blanks the CRT for a length of time sufficient to allow the horizontal amplifier (in the oscilloscope or other display that is being used with the Model 1607A) to settle down before writing each line. CLOCK also blanks the CRT when the display section is being reset (HDSPR = HI).

4-53. When no display-qualified clock occurs during an interval longer than 30 ms, HNCQ goes HI. When HNCQ is HI, LSC is LO and the Model 1607A goes into the partial display mode. LSC is combined with HEND+HTRG in NOR gate U1D. Therefore, when the

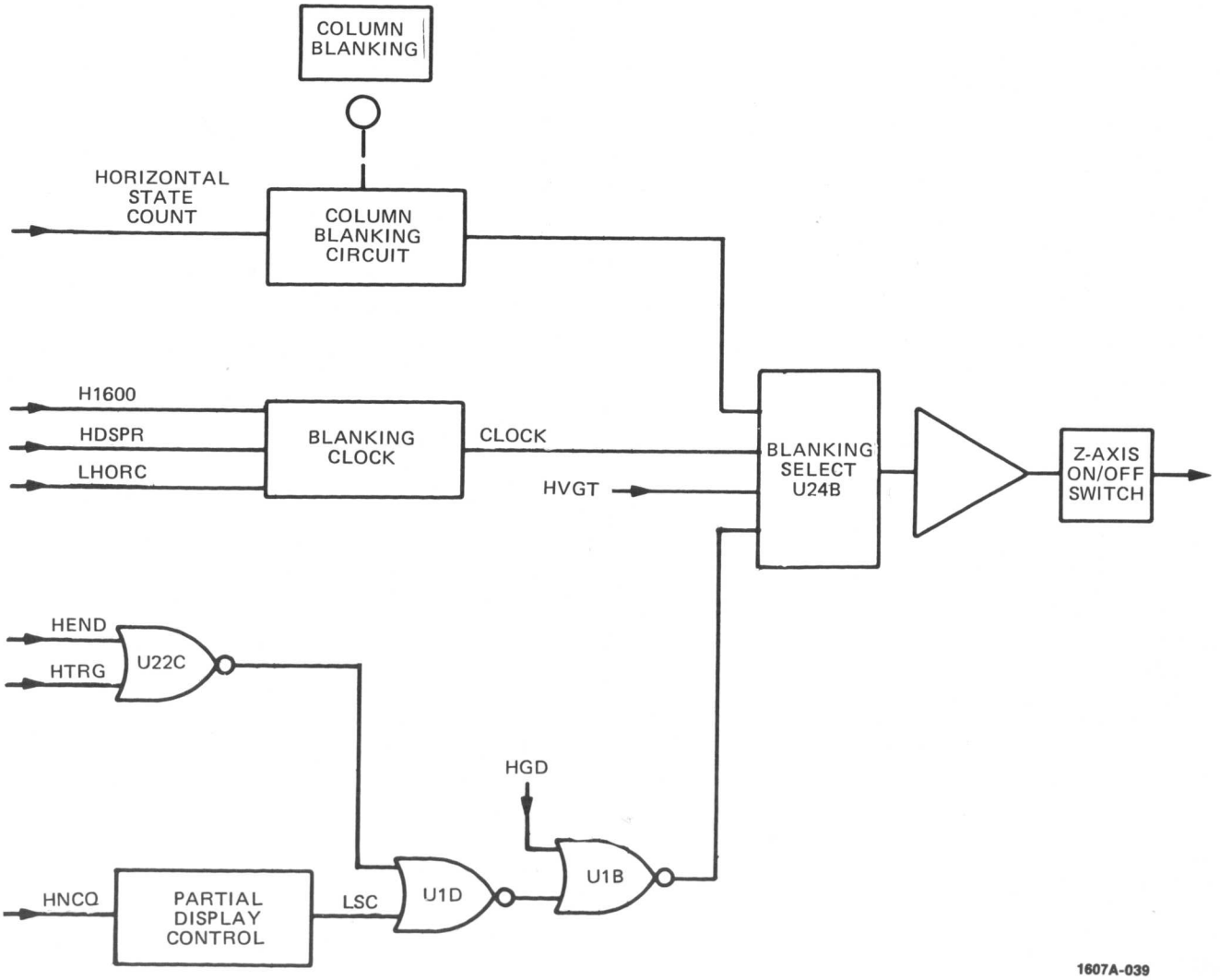



*Figure 4-10. Blanking Block Diagram*

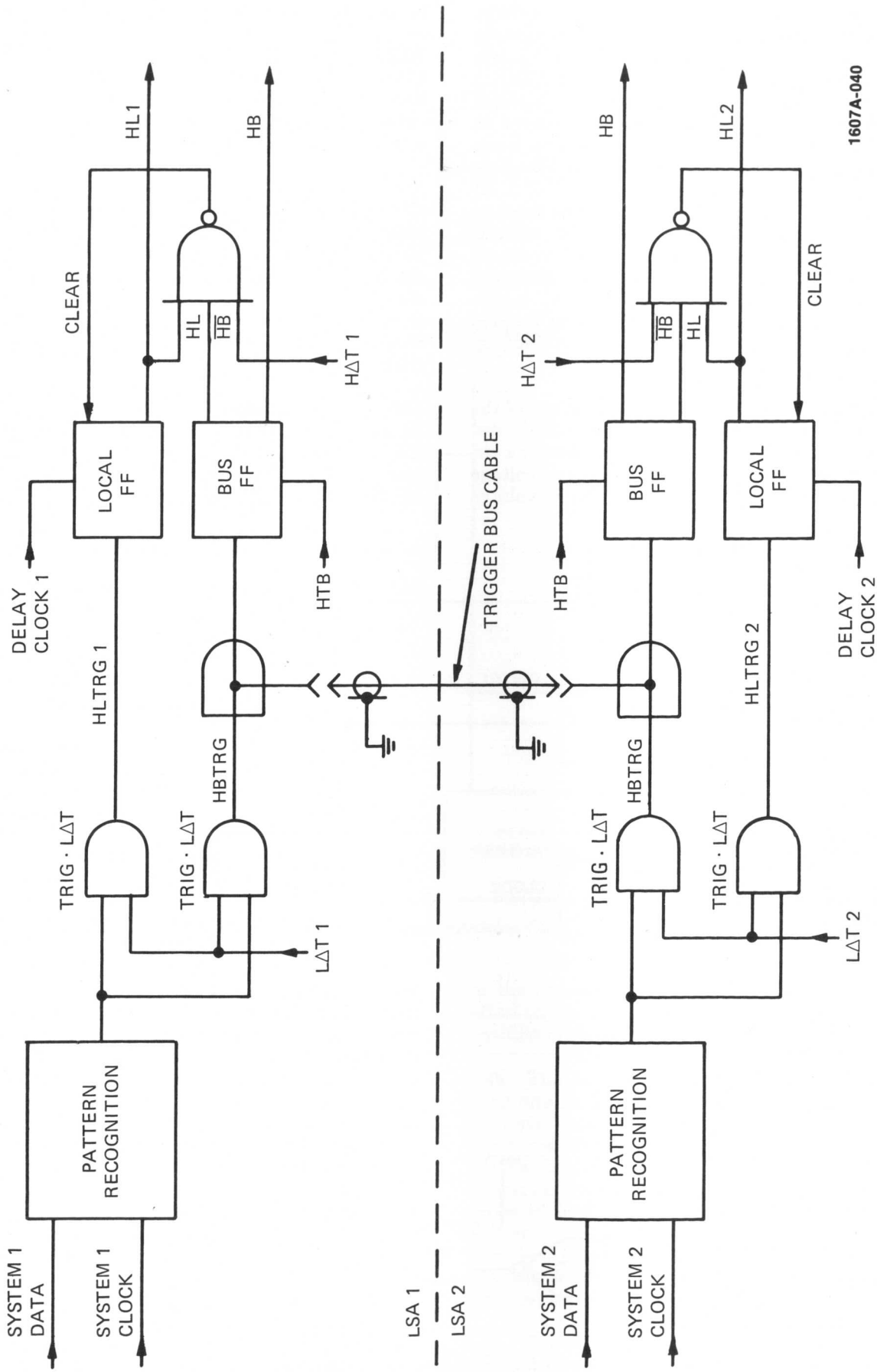



*Figure 4-11. Trigger Bus Simplified Schematic*

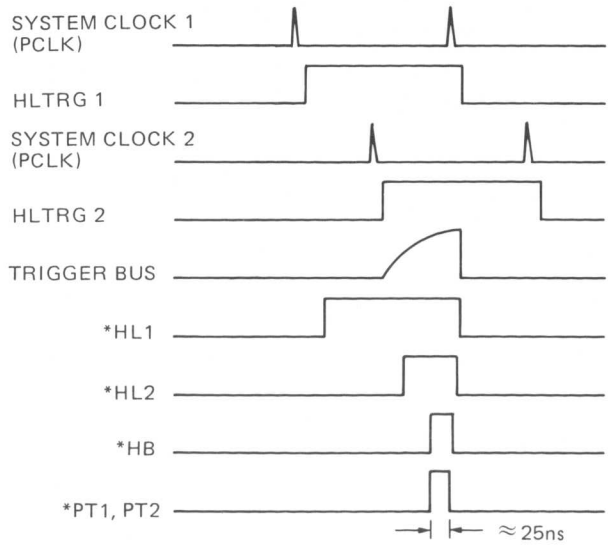
start display mode is selected and trigger word has been detected, LSC gates the output of U1D LO. This enables HGD to control blanking. HGD goes HI only after the trigger word is detected, unblanking the the CRT and allowing data to be displayed. The trigger word is written at the top of the display and the following 15 words are then written on the display one word at a time as they are clocked into the instrument. When end display is selected in the partial display mode, LSC unblanks the CRT allowing data to be displayed one word at a time as it is written into memory. When 16 words have been displayed, the the next word into memory is written in the bottom position and the top word is bumped from the display. This continues until the trigger word is detected, disabling the memory write function. HGD then goes HI, displaying the data in memory until the display section is reset. In the partial display mode, HVGT blanks memory locations which do not contain new data.

4-54. When LSC is HI (the qualified clock rate is greater than 60 Hz) HGD controls blanking.

## 4-55. DETAILED CIRCUIT DESCRIPTION.

4-56. The following detailed circuit description is limited to circuits that are unique or unusually complicated. No attempt is made to explain basic circuits or circuits using simple combinatorial logic.

**4-57. TRIGGER BUS. (See figures 4-11 and 4-12.)** The asynchronous trigger-bus circuit allows two logic state analyzers (LSA's) that are operating at different clock rates to be triggered simultaneously. The trigger bus circuit allows the 16-bit trigger words of the Model 1607A and a Model 1600A to describe a 32-bit state (trigger word) that must occur in the two circuits under test simultaneously.




*WAVEFORMS SHOWN ARE TRUE WHEN DELAY IS OFF. WITH DELAY SELECTED, PULSES REMAIN HI UNTIL DELAY IS COMPLETE.

1607A-041

*Figure 4-12. Trigger Bus Timing Diagram*

4-58. The clock rates of systems 1 and 2 need not be harmonically or phase related. The only condition that must be met is that the trigger words of both LSA's must occur simultaneously, i.e., HBTRG's in both LSA's are HI at the same time. The trigger-bus circuits in the Model 1607A and the Model 1600A are identical. The open collector AND of the two trigger-bus circuits, formed through the trigger bus cable results in the 32-bit trigger word.

4-59. HBTRG rises when HLTRG1 and HLTRG2 occur simultaneously, setting the bus flip-flop. The pattern trigger outputs (PT) in both LSA's occur when both the local and bus flip-flops are set (HB•HL). The local flip-flop is set when the local trigger conditions are met and the delay clock rises. When the local flip-flop in either LSA is set and the bus flip-flop is not set, the local flip-flop is cleared when the next system clock (PCLK) occurs, i.e., during LΔT. Thus, residues of local trigger conditions in either LSA are not carried over from one clock cycle to the next.

4-60. The dependence of the individual LSA on the trigger bus is determined by HTB. Whenever the LOCAL/BUS switch on an LSA is set to LOCAL, HTB is LO. HTB=LO holds the bus flip-flop in the clear state, forcing HB HI. Therefore, LSA operation is dependent only on local trigger conditions.

4-61. LΔT clears the trigger bus at the beginning of the PCLK cycle through AND gates A1U25A, A1U25B, and A1U25C in either LSA. Thus, with the trigger word turned off or during periods where the trigger conditions are met for multiple clock cycles, HBTRG will occur on each system clock, setting the bus flip-flops and generating pattern triggers.

**4-62. DISPLAY QUALIFIER. (See figure 4-13 and schematics 5, 6, 8, and 9.)** The display qualifier permits selective viewing of data in a parallel digital system, such as a computer or microprocessor, by allowing data to be clocked into the Model 1607A only when the inputs on the qualifier channels are true. For example, the two qualifier channels could be used to decode status lines in a computer system so that the Model 1607A would clock data into memory only when instructions are present on the monitored bus. Thus, the Model 1607A would display only instruction words and ignore all other data on the bus.

4-63. The display qualifier circuit functions in the following manner. Qualifier status (Q0, Q1) is stored in temporary storage flip-flops for one period of the system clock (PCLK). During this time interval, the qualifier status is tested against the qualifier conditions preset by the front-panel Q1/Q0 switches. When the qualifier status agrees with the preset conditions, HCLQ changes to a high level. HCLQ remains high

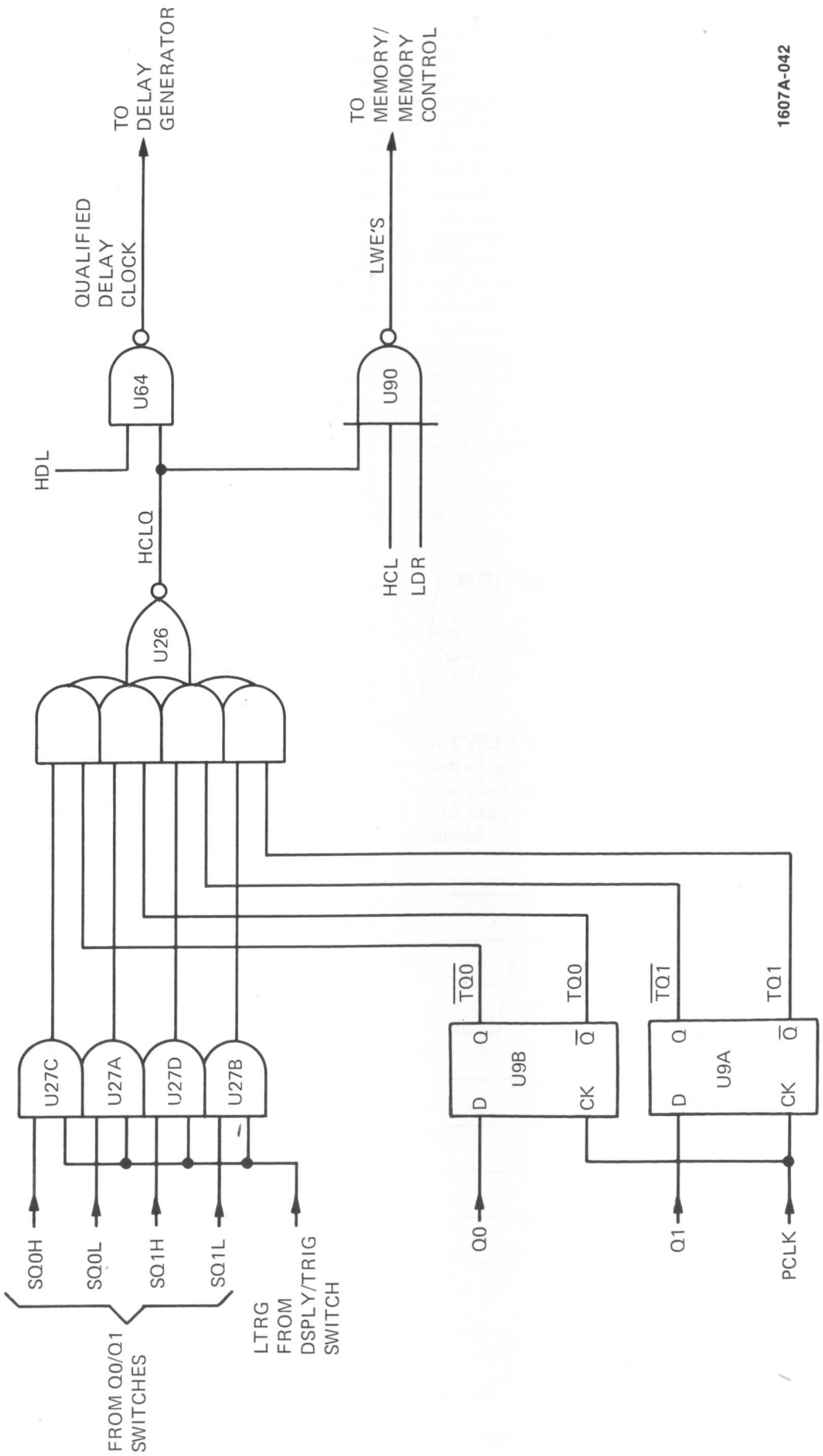



*Figure 4-13. Simplified Display Qualifier Circuit*

until either the status lines change or the qualification conditions are changed.

4-64. The delay clock and LWE1 have a fixed time relationship to PCLK set by the timing generator. The time relationship of HDL and HCL to PCLK make it possible to gate the two clock signals with HCLQ. Whenever HCLQ is high, HDL is gated through to the delay generator. During a data acquisition cycle, LDR is false. HCLQ then allows HCL to clock A1U90, generating LWE1 and LWE2. LWE equals $\overline{HCLQ \bullet LDR \bullet HCL}$. The NAND of HCLQ with HDL permits the delay generator to count only those clocks which occur when the qualifier conditions are true. The LWE pulses allow the Model 1607A to write into memory only data that occurs when the qualifiers are true.

4-65. In addition, the comparison of the qualifiers with the preset qualifier conditions is ANDed with the trigger recognition. Thus the Model 1607A can generate a pattern trigger only when the qualifiers are true. When the TRIG qualifier mode is selected, HCLQ is held in the true state by LTRQ.

**4-66. DELAY GENERATOR. (See schematic 6.)** The delay generator consists of two sections: the units-decade counter A1U70, and the four upper-decade counters A2U73 through A2U76. When the local and bus flip-flops are set (HB and HL are true), the units-decade counter is enabled, i.e., CEP and CET inputs are high. The clock for A1U70 is the NAND of HCLQ and HDL (A1U64, pin 8). When A1U70 reaches a binary count of 8, its Q3 output goes high. The Q3 output of A1U70 is routed to AOI gate A1U87 to provide the upper-decades clock. The upper-decades clock is a divide-by-ten of the delay clock. The Q3 output of A1U70 is also combined with the $\overline{Q}$ output of flip-flop A1U84A in AOI A1U81. When the upper-decade counters have reached terminal count (A1U84A, $\overline{Q}$ is HI), A1U81A, pin 8 goes low when A1U70, Q3 is high. This allows A1U84B to change states on the next delay clock, generating HDC.

4-67. When the TC output of the most significant decade (MSD) A1U76 occurs, the tens-decade counter A1U73 counts eight more clocks, setting its Q3 output HI. The NAND of the tens-decade Q3 output with the TC output of the MSD parallel enables the upper-decade counters. During the next TC output of A1U70, A1U84A is enabled to change states (through A1U66B). On the delay clock, the $\overline{Q}$ output of A1U84A goes high. This indicates that the upper-decade counters have reached terminal count. When the Q3 output of A1U70 goes low, the upper-decades of the delay generator are preset to the nines complement of the delay thumbwheel switch settings.

4-68. Functionally, A1U84A and A1U84B can be viewed as state nine of the tens-decade counter and the units-decade counter respectively. Assume the DELAY thumbwheels are set to 90. The upper-decade counters count 80 clocks and then are preset. Flip-flop A1U84A is latched, retaining the fact that the upper decades have reached terminal count. Units-decade counter A1U70 counts to 8 and is then preset. While A1U70 is being preset, A1U84B performs the last count for the units-decade. Therefore, the delay generator is ready to count again on the next clock pulse.

4-69. When the upper-decades of the DELAY thumbwheel switches are all set to zero, NAND gate A1U78 sets the $\overline{Q}$ output of A1U84B HI. Thus HDC occurs as soon as the units-decade completes its count. When all thumbwheel switches are set to zero, NAND gate A1U66A holds HDC HI. When the DELAY ON/OFF switch is set to OFF, LNDLY holds HDC in the HI state.

**4-70. TRIGGER GENERATOR. (See schematic 6.)** The trigger generator consists of the trigger arm flip-flop, the bus flip-flop, the local flip-flop, and some associated combinatorial logic.

4-71. When the NORM/ARM switch is set to NORM, LARM and HARM are held in the true state. When the NORM/ARM pushbutton is set to ARM, the occurrence of an external arming pulse clocks the arm flip-flop, generating LARM and HARM. When LARM and HARM are true, the local and bus flip-flops are enabled to operate until a trigger word is detected (HB and HL go true) and the delay is complete (HDC goes true). HB and HL are ANDed by A1U63C and A1U62A to generate PT (pattern trigger ontput pulse). HB•HL presets flip-flop A1U71B which generates HPTS. HPTS indicates the presence of a trigger and is a control signal for the NO TRIG indicator light. A1U71B is clocked clear when either HB or HL is false.

4-72. At the completion of the digital delay, the AND of HDC with HB and HL in NAND gates A1U69C and A1U62B generates the delayed trigger output (DT). DT remains HI for approximately 25 ns (determined by capacitor A1C30 and A1U63B). The trailing edge of the delayed trigger terminates the pattern-trigger output. HL•HB•HDC resets the trigger, arming, and terminal count flip-flops through A1U77 and A1U65.

**4-73. DATA ACQUISITION SYNCHRONIZER. (See schematic 6.)** Monostables A1U61 and A1U68A/B generate a timing sequence used to reset the delay and trigger generators to their initial conditions (waiting for a trigger). The three monostables also force the thumbwheel settings to be loaded into the decade counters. On the negative-going edge of LRST, A1U61 provides a low-level signal approximately 1 $\mu$s in width. This signal disables the delay clock AOI A1U64. A1U68A outputs a high-level signal (HRES) that resets the local, bus, arming, and terminal-count flip-flops and parallel enables the decade counters. During the time HRES is true, HRCL clocks the delay generator through A1U64, loading the nines-

complement of the DELAY thumbwheel switch settings into the decade counters.

**4-74. TIMING GENERATOR. (See schematic 7.)** The timing generator provides four timing signals used in the data acquisition section of the Model 1607A. HΔT is used in the reset circuitry for the local flip-flop. LΔT is a clock signal for the pattern recognition circuit and memory index and control. HCL is a clock signal used in memory index and control, and memory. HDL is the clock for the delay generator and is also used in the data index and control circuit.

4-75. The timing diagram for the four timing signals is shown on schematic 7. The negative-going LΔT pulse remains LO for an interval of time determined by transistor array A1U45 and the time constants of A1R48, A1R49, and A1C33. Shortly before the positive-going transition of LΔT, the output of A1U45, pin 8, clocks J/K flip-flop A1U43B and resets LΔT (A1U42, pin 10). The Q output of A1U43B goes HI, generating HCL. HCL remains HI for approximately 25 ns. Shortly after the positive-going edge of HCL, HDL goes HI. The negative-going transition of HDL occurs 5 ns before the negative-going transition of HCL. The widths of the timing signals and the time relationship between them are determined by A1C33 (LΔT), A1C37 (HDL), A1C41 (HCL), and A1R49 (LΔT). A complete adjustment procedure for the timing generator is provided in Section V.

4-76. All three circuits in the timing generator operate essentially in the same manner. When the input to the transistor array goes LO, its emitters ramp down at a rate determined by the RC network tied to the emitters. The ramp continues until it reaches threshold voltage minus $V_{be}$ of the second transistor in the pair. The threshold voltage is approximately 0.5 volt and is supplied by A1U44, pin 10. When the emitters reach threshold voltage minus $V_{be}$, the undriven transistor turns on. The collector of the undriven transistor then goes LO presetting the flip-flop. A1U42A/B form an RS flip-flop, and A1U43A and A1U43B are JK flip-flops.

4-77. As soon as the flip-flop is preset, the input to to the transistor array goes HI, pulling the emitter up. When the emitters go up, the undriven transistor turns off and the timing generator waits for another PCLK.

**4-78. MEMORY/MULTIPLEXER. (See schematic 8.)** The memory/multiplexer circuit consists of four random access memories (RAM's) that store the incoming data from the system under test, associated memory address control circuitry, and a multiplexer that serializes the parallel memory outputs for display on the CRT.

**4-79. Memory.** A1U28, A1U30, A1U32, and A1U34 are random access memories. Inverters A1U29, A1U31 and A1U33 delay the data from the temporary storage flip-flops to provide proper time relationships between the data and other operations in the data acquisition section. Write address counter A1U60 addresses memory during a write operation. The computed address (CA0-CA3) addresses memory during a read operation. AOI's A1U54, A1U55, A1U56, and A1U57 switch between the computed address and the write address counter.

4-80. The AOI's are controlled by several signals. When LDR and HDR* are true (Model 1607A in a display cycle), the AOI's point to the computed address. When the Model 1607A is in a data acquisition cycle, address selection is a function of the clock rate and the display qualifiers. If HCLQ or HSWA is LO, the AOI's point to the computed address. If HCLQ and HSWA are both HI, the AOI's point to the write address counter.

4-81. HSWA is generated by JK flip-flop A1U46B. A1U46B is controlled by LWE1 and LΔT. LΔT presets the flip-flop, generating HSWA and LSWA. LWE1 goes LO shortly after the positive-going edge of LΔT. On the positive-going edge of LWE1, A1U46B is clocked, forcing HSWA and LSWA false. The data stored in the temporary storage flip-flops is written into memory during the time interval that LWE1 and HSWA are true. The width of HSWA is 60 nanoseconds.

4-82. The operation described in the preceding paragraph can occur only at clock rates less than 15 MHz. When the qualified clock rate exceeds 15 MHz. LΔT's overlap the LWE1's and flip-flop A1U46B is never cleared out. Therefore HSWA and LSWA remain in the true state.

4-83. Thus, at clock rates below 15 MHz, the memory is addressed by the computed or display address between write cycles. The partial display mode which occurs at clock rates below 60 Hz utilizes this feature.

**4-84. Multiplexer.** Multiplexer A1U39 serializes the parallel output of the memories for display on the CRT screen. The horizontal state count sequences through the 16 parallel bits on the multiplexer input and provides a serial representation of the 16 bits at its output with bit 0 first.

**4-85. DATA INDEX AND CONTROL. (See schematic 9 and figure 4-14.)**

**4-86. Reset.** At the end of a display cycle LRST resets the data index and control circuit and initializes a data acquisition cycle. The trailing-edge of LRST clocks JK flip-flop A1U93A, setting HR1 and LRHS in the true state. LRHS resets the start flip-flop U88C/U91 and pulls the J input of flip-flop A1U89B LO. HR1 pulls the J input of flip-flop A1U93B and the K input of A1U89B HI. HR1 is also routed to the display section where it performs several functions. The first LΔT after LRST sets JK flip-flop A1U93B. The Q output of A1U93B (LR2) resets the end flip-flop

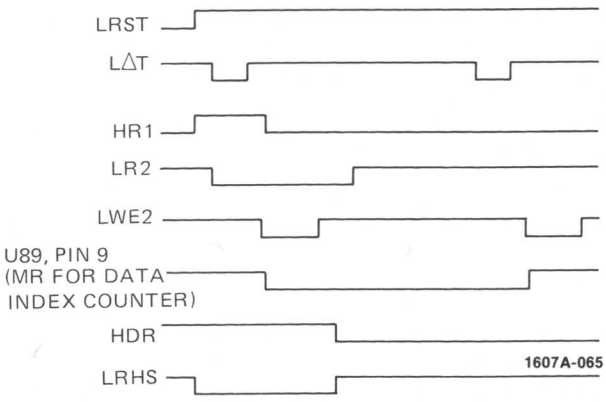



*Figure 4-14. Data Index and Control Reset Timing Diagram*

A1U92/U88B. The negative-going transition of the first LWE after LRST clocks the Q output of A1U89B HI. The Q output of A1U89B resets the data index counter A1U94 and stops the clock to terminal-count flip-flop A1U94B. LWE2 presets flip-flop A1U93A and clears A1U94A. On the trailing-edge of LWE2, HWE clears out flip-flop A1U89A which sets HDR LO. This causes the K input of A1U93A to go LO, prohibiting any additional LRST's.

4-87. On the next LΔT, A1U93B is cleared by the negative-going transition. On the negative-going transition of LWE2, A1U89B is cleared. This releases the data index counter master reset line. LWE2 also enables NAND gate A1U96A to pass HDL's.

**4-88. Start Display Mode.** In the start display mode, HSTR enables flip-flop A1U88C/A1U91. When LRHS is HI and a trigger word is detected (HB•HL•HDC), LTRG and HTRG go true. HTRG enables the data index counter to start counting qualified clocks. Count 14 of the data index counter is detected by NAND gate A1U96C, which applies a high level to the input of JK flip-flop A1U94B. On the next clock after state 14, A1U94B counts the 15th state. The $\overline{Q}$ output of A1U94B parallel enables the data index counter, locking it in the terminal count state. Thus, the data index terminal count is generated by A1U94B. This reduces the propagation delay from clock to terminal count of the data index counter. At the same time that the data index counter is parallel enabled, HTC sets the end flip-flop. This generates LDR which turns off further LWE's so that data is no longer written into memory. LDR indicates to the display section that memory is loaded with good data by presetting flip-flop A1U89A through NAND gate U96B. This generates HDR, which initiates a display cycle.

**4-89. End Display Mode.** In the end display mode, HSTR is LO which holds the start flip-flop preset. This holds LTRG and HTRG* in the true state. Thus, the first LWE2 after LRST increments the data index counter. When the data index counter reaches terminal count (HTC is true), the end flip-flop waits for HB, HL and HDC. When a trigger word is detected and the digital delay is complete, HDC•HB•HL•HTC sets the end flip-flop which generates LDR. LDR does not occur until the memory index counter is in the TC state indicating a full memory.

**4-90. Read Address Computation.** During the display cycle, the memory data read to the display section is addressed by the computed address (CA0-CA3). The computed address is derived in four-bit adders A1U58 and A1U59. A1U58 and A1U98A through A1U98D subtract the data index count from the write address count (WA0-WA3). The difference appears on the four sum outputs of A1U58. This difference is the address of the memory location containing the first word acquired during the data acquisition cycle. The first word address is added to the vertical state count in A1U59. The output of A1U59 is the computed address which is the sum of the first word address and the vertical state count.

4-91. During a partial display, the data index counter and write address counter are incremented; but the first word address will not change as long as there are fewer than 16 words in memory. As soon as 16 words are written into memory in the end display mode, the data index counter value becomes a fixed constant. However, the write address counter will continue to be incremented. Thus, the first word address changes. The instrument then keeps adding words at the bottom of the display and bumping a word out the top. This results in rolling the display on the CRT screen. As soon as the trigger word is detected, LWE2 is turned off and the write address counts stops counting. Thus, the output of U58 becomes constant. The output of A1U59 now changes as a function of the vertical state count.

**4-92. HVGT Comparator.** Comparator A1U97 compares the data index count with the vertical state count. Whenever the vertical state count exceeds the data index count, HVGT is true. HVGT indicates to the display section that the data stored in the memory location currently being addressed has not been updated during the present data acquisition cycle and is therefore invalid. The CRT is blanked whenever HVGT is true.

**4-93. Manual Reset.** Whenever a manual reset occurs, HMR* sets the end flip-flop, forcing LDR to the true state. HMR* also toggles JK flip-flop A1U94A. This generates HRBL, forcing HVGT HI. HVGT blanks the CRT. HMR* is followed by LRST which resets the data index and control circuit.

**4-94. WORD INTENSIFY CIRCUIT. (See schematic 11.)** The word intensify circuit determines when the vertical state count is addressing the trigger word location in memory. When the vertical state count addresses the trigger word, the trigger word intensify comparator A1U86 generates HE. HE is applied to the word intensify control logic (schematic 12). When HE is HI, the word intensify control logic causes the current

word being addressed in memory to be intensified on the display.

4-95. Multiplexer A1U83 and 4-bit adder A1U79 perform a code conversion on the DELAY thumbwheel switch outputs. A1U79 performs the following addition of the thumbwheel switch outputs:

| | | | | |
|---|---|---|---|---|
| | 2D3 | 1D3 | 1D2 | 1D1 |
| + | 2D0 | $\overline{2D0}$ | 1 | 2D0 |
| Carry (C4) | | Σ3 | Σ2 | Σ1 |

where 1D1-1D3 are units-decade switch output bits 1-3, and 2D0, 2D3 are tens-decade switch output bits 0 and 3.

The outputs of the adder are applied to the $I_0$ inputs of multiplexer A1U83, and $\overline{HSTR}$ is applied to the $I_1$ inputs of the multiplexer.

4-96. Selection of either the $I_0$ data from the adder or $I_1$ data from NAND gate A1U85B for output by the multiplexer is determined by the output of NAND gate A1U85C. $I_0$ data is selected when the output of A1U85C is LO; $I_1$ data is selected when the output of A1U85C is HI. A1U85C is LO only when LNDLY is false and the selected delay is 15 or less. Therefore, in the end display mode with a selected delay of 15 or less, the vertical state count is compared with the output code from the adder. When they match, the A = B output (HE) of comparator A1U86 goes HI. When the delay is greater than 15, the A4 input of A1U86 is LO, forcing HE to the false state.

4-97. When the start display mode is selected, the comparator is enabled only when the delay is set to 0. For all other delays, the A4 and B4 inputs of the comparator are held at different levels; holding HE false.

4-98. When LNDLY is true, the select input of the multiplexer is held HI. Therefore the multiplexer always points to the $I_1$ inputs. With HSTR true, the $I_1$ inputs are all LO, causing the first word on the display to be intensified. With HSTR false, the $I_1$ inputs are all HI, causing the last word on the display to be intensified.

*Table 4-1. Model 1607A Mnemonics*

| MNEMONIC | FUNCTION | ORIGIN |
|---|---|---|
| AM0-AM15 | Memory output data. Data stored in memory for display. | Schematic 8, A1U28, A1U30, A1U32, A1U33 PINS 5, 7, 9, and 11 |
| ARM | Arming input signal from TRIG ARM IN connector. | Schematic 6, TRIG ARM IN Connector J3 |
| CLOCK | 50 kHz display clock. CLOCK provides clock signal for horizontal state counter and blanking. | Schematic 14, A2U14D, PIN 11 |
| CA0-CA3 | Computed Address. Memory address used to read memory during display cycle. Computed address = vertical state count + (Write Address Count - Data Index Count). | Schematic 9, A1U59, PINS 2, 6, 9, and 15 |
| $\overline{DATA}$ | Serialized data output from memory used to derive LZER and XDSPD. | Schematic 8, A1U39, PIN 10 |
| DT | Delayed Trigger. Trigger generator output signal applied to DELAYED TRIG OUT connector. | Schematic 6, A1U62B, PIN 8 |
| D0-D15 | Input data bits 0 through 15 from Data Probes. | Schematic 3, A1J2, PINS 13 - 16; A1J3, PINS 11 - 16; A1J4, PINS 11 - 16 |
| HARM | HI, Armed. Complement of LARM. | Schematic 6, A1U71A, PIN 7 |
| HARME | HI, Arm Enable. Data acquisition control signal (dc level). HARME = HI when NORM/ARM is set to ARM position (in). When HI, the Model 1607A must be armed before it will recognize a trigger. | Schematic 10, NORM/ ARM Switch A2S2D |

*Table 4-1. Model 1607A Mnemonics (Cont'd)*

| MNEMONIC | FUNCTION | ORIGIN |
|---|---|---|
| HB | HI, Bus. Data acquisition control signal. HB = HI when bus flip-flop is set. | Schematic 6, A1U67A, PIN 7 |
| HBCD | HI, BCD. Display control signal (dc level) for Horizontal Code Converter U26. When HI, displayed word format is four four-bit bytes. When LO, displayed word format is five three-bit bytes with MSB left over. | Schematic 13, BYTE 4 BIT/3 BIT switch A2S1E |
| HBR | HI, Brighten. Control signal to Model 1600A HBR = HI indicates current displayed character in table B should be intensified. | Schematic 12, A2U23E, PIN 12 |
| HBTRG | HI, Bus Trigger. Trigger signal (HI state) indicating both Model 1607A and Model 1600A Trigger words have occurred simultaneously in the trigger bus mode. | Schematic 5, A1U25B, PIN 8 |
| HCL | HI, Clock. Clocking signal from timing generator used to clock data index and control. HCL is derived from PCLK. | Schematic 7, A1U43B, PIN 7 |
| HCLQ | HI, Clock Qualifier. DSPLY qualification signal. HCLQ is HI when DSPLY qualifier requirements are met. | Schematic 5, A1U26, PIN 8 |
| HDC | HI, Delay Complete. Data acquisition control signal. HDC = HI when delay generator has counted out the delay set on DELAY thumbwheels. | Schematic 6, A1U84B, PIN 9 |
| HDL | HI, Delay Clock. Clocking signal from timing generator used to clock delay generator. HDL is derived from PCLK. | Schematic 7, A1U43A, PIN 6 |
| HDR | HI, Data Ready. HI state occurs at the end of a data acquisition cycle. | Schematic 9, A1U89A, PIN 5 |
| HDR* | HI, Data Ready*. Memory Address control signal indicating trigger word has been found and memory is loaded with valid data. When HI, HDR* enables reading of memory by display section. | Schematic 9, A1U88B, PIN 8 |
| HDSPR | HI, Display Reset. Reset signal for all display functions. | Schematic 12, A2U14E PIN 4 |
| HΔT | HI, Delta T. Clocking signal for local flip-flop reset gate. HΔT is derived from PCLK. | Schematic 7, A1U42A, PIN 6 |
| HE | HI, Equal. Control signal for word intensify circuit. HI when trigger word is being addressed by display section. | Schematic 11, A1U86, PIN 14 |
| HEND | HI, End. Display control signal (dc level). HEND = HI when END DSPL is selected. HEND = LO when START DSPL is selected. | Schematic 10, START DSPL Switch A2S2B |
| HGD | HI, Good Data. True state indicates current data in memory is valid and should be displayed. HGD = HDR • $\overline{\text{HR1}}$ latched at end of each display cycle. | Schematic 2, A2U23F, PIN 15 |
| HLTRG | HI, Local Trigger. Trigger signal (HI state) indicating Model 1607A has met local triggering requirements. | Schematic 5, A1U25C, PIN 12 |
| HMAP | HI, Map. Control signal for delay generator and data index and control. HMAP is always LO. | Schematic 12, GND |

*Table 4-1. Model 1607A Mnemonics (Cont'd)*

| MNEMONIC | FUNCTION | ORIGIN |
|---|---|---|
| HMR | HI, Manual Reset. Manual reset pulse. HMR goes HI on trailing edge of HMR*. | Schematic 12, A2U4A. PIN 3 |
| HMR* | HI, Manual Reset*. Manual reset signal for data index and control circuit. | Schematic 12, A2U4A, PIN 3 |
| HMRXT | HI, Manual Reset External. External manual reset pulse from Model 1600A. | Schematic 15, I/O PORT Connector J5, PIN 16 |
| HNCQ | HI, No Clock or No Qualifier. Signal used to derive LSC. HNCQ = HI when no qualified clock has occurred for more than approximately 20 ms. | Schematic 10, A1U47C, PIN 8 |
| HNQL | HI, No Qualifier. NO QUAL indicator light control signal. HNQL = HI when no display qualifier has occurred for more than approximately 100 ms. | Schematic 10, A1U49C, PIN 10 |
| HNTRG | HI, No Trigger. NO TRIG indicator light control signal. HNTRG = HI when no trigger has occurred for more than approximately 100 ms. | Schematic 10, A1U49A, PIN 1 |
| HPTS | HI, Pattern Trigger Stored. Control signal for indicator light logic. When HPTS is HI, NO TRIG light is held off. | Schematic 6, A1U71B, PIN 10 |
| HRBL | Hi, Reset Button Latched. Data index control signal. When HRBL goes HI, HVGT is forced HI. | Schematic 9, A1U94A, PIN 5 |
| HRECL | HI, Reset Clcok. Clocking signal for digital delay and trigger generator during reset function (LRST = LO). | Schematic 6, A1U68B, PIN 6 |
| HRES | HI, Reset. Reset pulse used in digital delay and trigger generator circuit. HRES is derived from LRST. | Schematic 6, A1U68A, PIN 10 |
| HR1 | HI, Reset 1. When HI, HR1 indicates that a reset has been requested and will happen on next input clock. | Schematic 9, A1U93A, PIN 6 |
| HRPS | HI, Repetitive selected. Display control signal (dc level). HRPS = HI when REPET/SINGLE switch is set to REPET. | Schematic 12, REPET/ SINGLE Switch A2S1B |
| HSSS | HI, Single Sample Start. Disables HVGT at instrument turn-on ensuring display on CRT in SINGLE mode. HSSS = HI at instrument turn-on. Once reset occurs, HSSS remains LO. | Schematic 12, A2U19E, PIN 12 |
| HSTR | HI, Start. Data acquisition/display control signal (dc level). HSTR = HI when START DSPL is selected. | Schematic 10, END DSPL Switch A2S2C |
| HSWA | HI, Select Write Address. Address control signal. When HSWA is HI, memory is addressed by write address counter. | Schematic 8, A1U46B, PIN 9 |
| HL | HI, Local. Data acquisition control signal. HL = HI when local flip-flop is set. | Schematic 5, A1U67B, PIN 9 |

*Table 4-1. Model 1607A Mnemonics (Cont'd)*

| MNEMONIC | FUNCTION | ORIGIN |
|---|---|---|
| HTB | HI, Trigger Bus. Data Acquisition control signal (dc level). HTB = HI when SRC LOCAL/BUS switch is set to BUS. When HI, Model 1607A will trigger only when its trigger word and the Model 1600A trigger word are true simultaneously in the trigger bus mode. | Schematic 10, SRC LOCAL/BUS Switch A2S2E |
| HTC | HI, Terminal Count. Data index control signal. HTC = HI when data index counter is at terminal count. | Schematic 9, A1U94B, PIN 9 |
| HTRG | HI, Trigger. HTRG goes HI when trigger word is found and remains HI until data acquisition section is reset. | Schematic 9, A1U88D, PIN 11 |
| HTWO | HI, Trigger Word ON. Data acquisition control signal (dc level). HTWO enables TRIGGER WORD switches. HTWO = HI when OFF/WORD switch is set to WORD (in position). | Schematic 10, WORD OFF/ON Switch A2S2F |
| HVGT | HI, Vertical Greater Than. Display control signal to blank CRT when display section addresses invalid data in memory. HVGT = HI when vertical state count is greater than data index count. | Schematic 9, A1U97, PIN 15 |
| HWE | HI, Write Enable. Data index control signal. HWE = HCLQ • HCL • LDR | Schematic 9, A1U88A, PIN 3 |
| HXRPR | HI, External Repetitive Reset. External repetitive reset signal from Model 1600A. | Schematic 15, I/O PORT J5, PIN 17 |
| H0-H3 | Horizontal State Count. Each four-bit word indicates address of a specific bit of current displayed word. | Schematic 12, A2U25, PINS 3, 2, 6, and 7 |
| H1600 | HI. H1600. Control signal from Model 1600A derived from L1600. H1600 = HI when Model 1607A is connected to Model 1600A via I/O Bus. | Schematic 12, A2U15B, PIN 4 |
| LARM | LO, Armed. Control signal for trigger generator circuit and indicator and control logic. LARM = LO when ARM and HARME are both HI, or when HARME = LO. | Schematic 6, A1U71A, PIN 6 |
| LBNK | LO, Blank. Display blanking control signal. Display is blanked when LBNK = LO. | Schematic 14, A2U23A, PIN 2 |
| LCLQ | LO, Clock Qualified. Complement of HCLQ. | Schematic 5, AU41C, PIN 8 |
| LDR | LO, Data Ready. Control signal used to initiate display cycle. LDR goes LO when data acquisition is complete. | Schematic 9, A1U92, PIN 8 |
| LDSPR | LO, Display Reset. Model 1600A table B reset signal. Used in I/O Bus operation. | Schematic 2, A2U19C, PIN 6 |
| LΔT | LO, Delta T. Clocking signal for pattern recognition, data index and control, and memory. LΔT is derived from PCLK. | Schematic 7, A1U42B, PIN 8 |
| LECMP | LO, Enable Compare. Enable signal for trigger word intensify comparator A1U86. | Schematic 5, DSPLY/ TRIG Switch A1S1C |

*Table 4-1. Model 1607A Mnemonics (Cont'd)*

| MNEMONIC | FUNCTION | ORIGIN |
|---|---|---|
| LHORC | LO, Horizontal Carry. Carry output from horizontal state counter. LHORC = 0 occurs following writing MSB of each displayed word. | Schematic 12, A2U25, PIN 12 |
| LNARM | LO, No Arm. NO ARM indicator light control signal, LNARM = LO when no arming signal has occurred for more than approximately 100 ms. | Schematic 10, A1U72B, PIN 8 |
| LNCK | LO, No Clock. NO CLOCK indicator light control signal. LNCK = LO when no qualified clock signal has occurred for more than approximately 100 ms. | Schematic 10, A1U47D, PIN 11 |
| LNDLY | LO, No Delay. Data acquisition control signal (dc level) LNDLY = LO when DELAY OFF/ON switch is set to OFF. | Schematic 10, DELAY OFF/ON Switch A2S2A |
| LRHS | LO, Reset HI Start. Start flip-flop reset signal. | Schematic 9, A1U93A, PIN 5 |
| LRST | LO, Reset. Reset signal for data acquisition section. LRST occurs at end of display cycle. | Schematic 2, A2U9, PIN 8 |
| LR2 | LO, Reset 2. Data index and control reset signal. | Schematic 9, A1U93B, PIN 7 |
| LSC | LO, Slow Clock. Blanking control signal enabling words to be written one at a time as they are written in memory in partial display mode with END DSPL selected. LO when clock rate is less than approximately 50 Hz. | Schematic 14, A2U1C, PIN 10 |
| LSWA | LO, Select Write Address. Complement of HSWA. | Schematic 8, A1U46B, PIN 7 |
| LTRG | LO, Trigger. LTRG is inverted and routed to display section to control blanking. | Schematic 9, A1U91, PIN 8 |
| LTRQ | LO, Trigger Qualified. Qualifier control signal. When LTRQ = LO, HCLQ is held HI. | Schematic 5, DSPLY/ TRIG Switch A1S1C |
| LVRTC | LO, Vertical Carry. Carry output from vertical state Counter. LVRTC occurs following writing of last word on display. | Schematic 12, A2U20, PIN 12 |
| LWE1 | LO, Write Enable 1. Memory address control signal. LWE1 = LO enables HSWA and LSWA. | Schematic 9, A1U90A, PIN 6 |
| LWE2 | LO, Write Enable 2. Clock signal for write address counter. | Schematic 9, A1U90B, PIN 8 |
| LXMR | LO, External Manual Reset. External manual reset signal from Model 1600A for data index and control circuitry. | Schematic 15, I/O PORT Connector J5 |
| LXPG | LO, External Plugged. DC level applied to Model 1600A indicating Model 1607A is connected on I/O Bus. LXPG is always LO. | Schematic 12, A2U15C, PIN 6 |
| LZER | LO, Zero. Determines whether a one or a zero is displayed on the CRT. When 100 kHz is applied to the horizontal output a zero is displayed. | Schematic 12, A2U2A, PIN 3 |

*Table 4-1. Model 1607A Mnemonics (Cont'd)*

| MNEMONIC | FUNCTION | ORIGIN |
|---|---|---|
| L1600 | LO, 1600. Control signal from Model 1600A enabling that instrument to exercise control of the Model 1607A display section. | Schematic 15, I/O PORT Connector J5 |
| NCLK | Negative (Transition) Clock. A buffered TTL reproduction of the clocking signal from the system under test, the complement of PCLK. | Schematic 3, CLOCK INPUT Connector A1J1, PIN 11 |
| Q0, Q1 | Qualifiers 0 and 1. Input qualifier bits 0 and 1 from data probes. | Schematic 3, Q1, Q0/ INPUTS 15 - 12 Connector A1J2, PINS 11 and 12 |
| SI | Slope Invert. Clock slope command signal to the Clock Probe. The complement of SS. SI = HI when CLOCK is ⎍ (out) and LO when CLOCK is ⎏ (in). | Schematic 3, CLOCK/ Switch A1S1B |
| SQ0H, SQ1H | Buffered QUALIFIER Q0/Q1 switch outputs for HI position. TERM = +5 V when applicable switch is set to HI and ≈0 V when set to OFF or LO. | Schematic 4, A1U24A, PIN 2; A1U24B, PIN 4 |
| SQ0L, SQ1L | Buffered QUALIFIER Q0/Q1 switch outputs for LO position. TERM = +5 V when applicable switch is set to LO and ≈0 V when set to OFF or HI. | Schematic 4, A1U24C, PIN 6; A1U24F, PIN 15 |
| SS | Slope Switch. Clock slope command signal to Clock Probe. SS and SI control PCLK and NCLK leading edge transitions in reference to clocking signal from system under test. SS = LO when CLOCK is ⎍ (out) and HI when CLOCK is ⎏ (in). | Schematic 3, CLOCK ⎍/⎏ Switch A1S1B |
| S0H-S15H | Buffered TRIGGER WORD switch outputs for HI position. TERM = +5 V when applicable switch is set to HI and ≈0 V when set to OFF or LO. | Schematic 4, A1U19 thru U24 |
| S0L-S15L | Buffered TRIGGER WORD switch outputs for LO position. TERM = +5 V when applicable switch is set to HI and ≈0 V when set to OFF or HI. | Schematic 4, A1U19 thru U24 |
| THRESHOLD | A dc level applied to the Clock and Data Probes which matches probe comparator switching threshold to the switching threshold of the system under test. | Schematic 3, A1U48, PIN 6 |
| TQ0, TQ1 | Temporary Storage flip-flop qualifier output bits 0 and 1. | Schematic 5, A1U9, PINS 6 and 8 |
| $\overline{TQ0}$, $\overline{TQ1}$ | Complemented Temporary Storage flip-flop qualifier output bits 0 and 1. | Schematic 5, A1U9, PINS 5 and 9 |
| T0-T15 | Temporary Storage flip-flop output bits 0 through 15. | Schematic 5, A1U1 thru U8, PINS 6 and 8 |
| V0-V3 | Vertical State Count. Four-bit address of word currently being displayed. | Schematic 12, A2U20, PINS 3, 2, 6, and 7 |
| WA0-WA3 | Write Adress Count. WA0 - WA3 address memory during write function. | Schematic 8, A1U6, PINS 14, 13, 12, and 11 |

*Table 4-1. Model 1607A Mnemonics (Cont'd)*

| MNEMONIC | FUNCTION | ORIGIN |
|---|---|---|
| XDSPD | External Display Data. Value of bit currently being addressed by V0 - V3 and H0 - H3. Signal is routed to Model 1600A via I/O Bus for display on table B. | Schematic 12, A2U15D, PIN 8 |
| XH0-XH3 | External Horizontal State Count. Bit address from Model 1600A display section. | Schematic 15, I/O PORT Connector, PINS 6, 7, 8, and 9 |
| XV0-XV3 | External Vertical State Count. Word address from Model 1600A display section. | Schematic 15, I/O PORT Connector, PINS 10, 11, 12, and 13 |
| 1D0-3, 2D0, 2D3, 3D0, 3D3, 4D0, 4D3, 5D0, 5D3 | Outputs from DELAY switch used to derive HE. Term is XDY where X = decade and Y = bit of 4-bit code. | Schematic 6, A10S1 |

# SECTION V

# PERFORMANCE CHECK AND ADJUSTMENTS

## 5-1. INTRODUCTION.

5-2. This section contains performance checks and adjustment procedures for your instrument. The performance tests, which begin with paragraph 5-7, verify that your instrument meets its published specifications (table 1-1). Adjustment procedures, beginning with paragraph 5-24, are provided to help you maintain your instrument within specification limits.

## 5-3. RECOMMENDED TEST EQUIPMENT.

5-4. Equipment required for the performance checks, adjustment procedures, and troubleshooting is listed in table 5-1. Any equipment that satisfies the critical specifications given in the table may be substituted for the recommended model(s).

## 5-5. CHECK RECORD.

5-6. A Performance Check Record form is provided at the end of this section for the purpose of recording the results of the performance checks. This form may be removed from your manual and retained as a permanent record of the incoming inspection or routine maintenance performed on the instrument. Be sure to include the instrument serial number on the record for identification.

## 5-7. PERFORMANCE CHECK.

5-8. The following checks verify that your instrument is operating within the specifications outlined in table 1-1 of this manual. If it has been determined, after completing the performance check, that the instrument does not meet one or more of its specifications; refer to paragraph 5-24, Adjustment procedures.

**5-9. INITIAL OPERATIONAL CHECK.** Perform the operator's checks listed in Section III to verify proper operation of the display functions in the Model 1607A. To verify proper operation of the instrument acquisition functions, perform the following procedure.

**NOTE**

The test equipment setup for the initial operational check is used for several functional and specification checks.

a. Connect equipment as shown in figure 5-1.

b. Apply waveform shown in figure 5-2A to clock probe input. Apply waveform shown in figure 5-2B to data probe inputs 0-15.

c. Set Model 1607A controls as follows:

| | |
|---|---|
| CLOCK | ⌐¯ |
| THLD | TTL |
| QUALIFIER Q1, Q0 | OFF |
| SAMPLE MODE | REPET |
| START DSPL | ON |
| TRIGGER MODE | |
| NORM/ARM | NORM |
| LOCAL/BUS | LOCAL |
| WORD | ON |
| TRIGGER WORD | all HI |

d. Alternately switch each TRIGGER WORD switch to LO and back to HI. Observe that NO TRIG lamp turns on and loss of display occurs when switch is set to LO.

e. Ground each data probe separately. Observe loss of display and NO TRIG indication when probe is grounded.

**5-10. SPECIFICATION CHECK.** The following paragraphs check the instrument performance to specifications listed in table 1-1.

**5-11. Repetition Rate.** Specification: 0 to 20 MHz.

a. Set Model 1607A controls per paragraph 5-9, step c and apply waveforms shown in figure 5-3.

b. Observe that display is all 1's and NO CLOCK and NO TRIG indicators are off. This check verifies that the Model 1607A is properly accepting data at the maximum specified repetition rate.

**5-12. Input RC:** Specification: Probe, 40 kΩ +3 kΩ shunted by less than 14 pF.

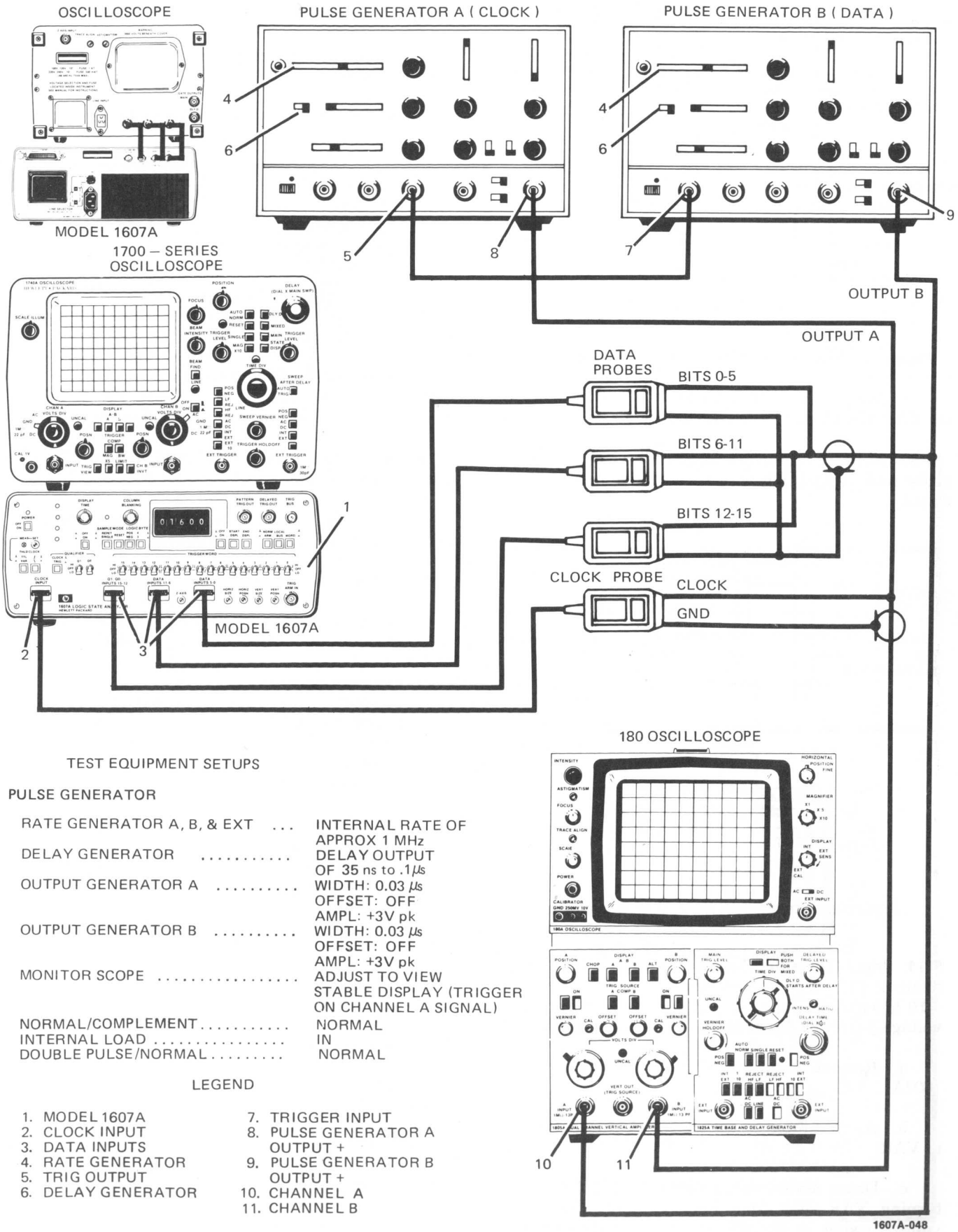
a. Using a multimeter, measure the resistance between each data-probe input and ground. Also measure the resistance between clock-probe input and ground. Observe that input impedance of clock and data probes is 40 kΩ ±3 kΩ.

b. Using LCR meter, measure shunt capacitance between each data- and clock-probe input and ground. Observe that each input capacitance is less than 14 pF.

**5-13. Input Bias Current.** Specification: Less than 30 μA.

*Table 5-1. Recommended Test Equipment*

| Instrument | | Required Characteristics | Required For |
|---|---|---|---|
| Type | Model | | |
| Clock Probe | HP 10230B | No substitute | Performance Check and Troubleshooting |
| Six-bit Data Probe | HP 10231B | No substitute | Performance Check and Troubleshooting |
| Waveform Monitoring Oscilloscope | HP 180 Mainframe with plug-ins | General purpose, >100 MHz; Sweep Speeds of 10 ns/DIV | Performance Check, Adjustments, and Troubleshooting |
| Vertical Plug-in | HP 1805A | 50-ohm input, 100-MHz bandwidth | Performance Check and Troubleshooting |
| Time Base Plug-in | HP 1825A | 10 ns/div, 100-MHz bandwidth | Performance Check and Troubleshooting |
| Pulse Generators (2) | HP 8013B | Adjustable 0 to 20 MHz; Adjustable 0 to 5 V pk amplitude; Positive and Negative Polarity; Adjustable 20 ns to 0.5-$\mu$s width; Adjustable 0 to 5-V offset | Performance Check and Troubleshooting |
| Multimeter | HP 3469B | Dc current 0 to 30 $\mu$A; dc voltage, 0 to 10 V; Resistance, 0 to 43 kilohms | Performance Check, Adjustments, and Troubleshooting |
| LCR Meter | HP 4332A | Capacitance, 0 to 25 pF | Performance Check and Troubleshooting |
| 50-ohm BNC feedthrough | HP 11048B | 50-ohm feedthrough termination | Performance Check |
| Function Generator | HP 3310A | ±10 V offset | Performance Check |
| Counter | HP 5300A HP 5302A | Period Measurement | Performance Check |
| Logic Analyzer | HP 1601A | Pattern recognition and State Display | Troubleshooting |
| Logic Trouble-shooting Kit | HP 5015T | Logic Pulser, Logic Probe, Logic Clip | Troubleshooting |
| Display Monitoring Oscilloscope | HP 1700-Series | External X and Y Inputs: 0.1 to 1-volt sensitivity, DC to >500 kHz bandwidth. Z-axis Input: DC coupled positive blanking. Must be able to fully blank with <10 V input at 10 mA. | Performance Check, Adjustments, and Troubleshooting |




TEST EQUIPMENT SETUPS

PULSE GENERATOR

| | |
|---|---|
| RATE GENERATOR A, B, & EXT ... | INTERNAL RATE OF APPROX 1 MHz |
| DELAY GENERATOR ..... | DELAY OUTPUT OF 35 ns to .1 $\mu$s |
| OUTPUT GENERATOR A ..... | WIDTH: 0.03 $\mu$s<br>OFFSET: OFF<br>AMPL: +3V pk |
| OUTPUT GENERATOR B ..... | WIDTH: 0.03 $\mu$s<br>OFFSET: OFF<br>AMPL: +3V pk |
| MONITOR SCOPE ..... | ADJUST TO VIEW STABLE DISPLAY (TRIGGER ON CHANNEL A SIGNAL) |
| NORMAL/COMPLEMENT..... | NORMAL |
| INTERNAL LOAD ..... | IN |
| DOUBLE PULSE/NORMAL..... | NORMAL |

LEGEND

1. MODEL 1607A
2. CLOCK INPUT
3. DATA INPUTS
4. RATE GENERATOR
5. TRIG OUTPUT
6. DELAY GENERATOR
7. TRIGGER INPUT
8. PULSE GENERATOR A OUTPUT +
9. PULSE GENERATOR B OUTPUT +
10. CHANNEL A
11. CHANNEL B

*Figure 5-1. Operational Check Test Setup*

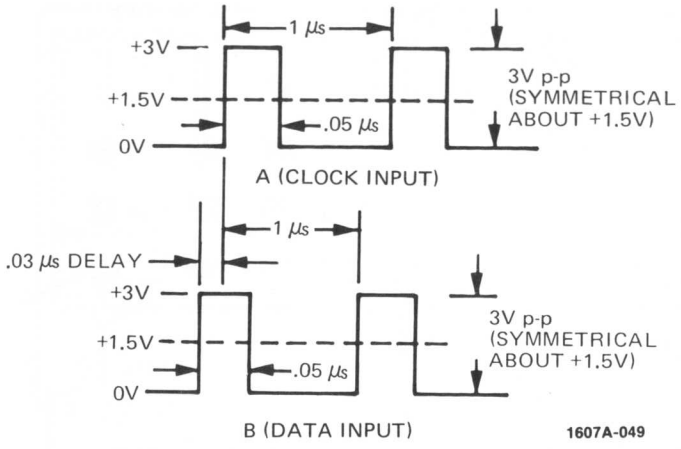



*Figure 5-2. Operational Check Input Waveforms*

a. Set THLD to VAR. Using a multimeter, monitor VAR MEAS and adjust VAR SET for —10 Vdc.

b. Measure current between each clock and data probe and ground. Observe that current is less than 30 μA.

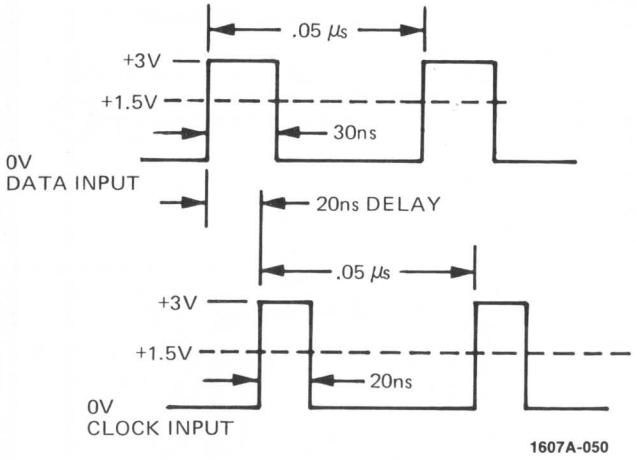



*Figure 5-3. Repetition Rate Test Waveforms*

**5-14. Input Threshold/Swing.** Input threshold specification: TTL, fixed at approximately 1.5 Vdc; variable, —10 to +10 Vdc. Input swing: 0.5 V +5% of threshold voltage p-p (min). Input level: —15 Vdc to +15 Vdc.

a. Remove data and clock probes from Model 1607A.

b. Apply power to Model 1607A and set THLD to VAR.

c. Using multimeter, monitor VAR MEAS while turning VAR SET from limit to limit. Verify that voltage swing is smooth and that limits exceed or equal to —10 to +10 Vdc.

d. Connect test equipment as shown in figure 5-4.

e. Apply test waveform shown in figure 5-5A to clock- and data-probe inputs of the Model 1607A.

f. Set Model 1607A controls as follows:

| | |
|---|---|
| CLOCK | ⌐‾ |
| THLD | TTL |
| START DSPL | ON |
| WORD | ON |
| QUALIFIER | |
| DSPLY/TRIG | TRIG |
| Q1, Q0 | HI |
| TRIGGER WORD | Bits 0-15 HI |

g. Observe that front-panel indicator lights are off.

h. Alternately switch each TRIGGER WORD switch to LO and back to HI. Observe that NO TRIG indicator lamp comes on when switch is set to LO.

i. Apply test waveform shown in figure 5-5B to clock- and data-probe inputs.

j. Set THLD to VAR and adjust VAR SET for valid clock and data inputs (indicator lights off).

k. Repeat step h.

l. Remove 50-ohm oscilloscope load and connect function-generator output directly to clock and data probes.

m. Apply test waveform shown in figure 5-5C to clock- and data-probe inputs.

n. Adjust VAR SET for valid data and clock inputs (indicator lights off).

o. Repeat step h.

p. Apply test waveform shown in figure 5-5D to clock- and data-probe inputs.

q. Adjust VAR SET for valid clock and data inputs (indicator lights off).

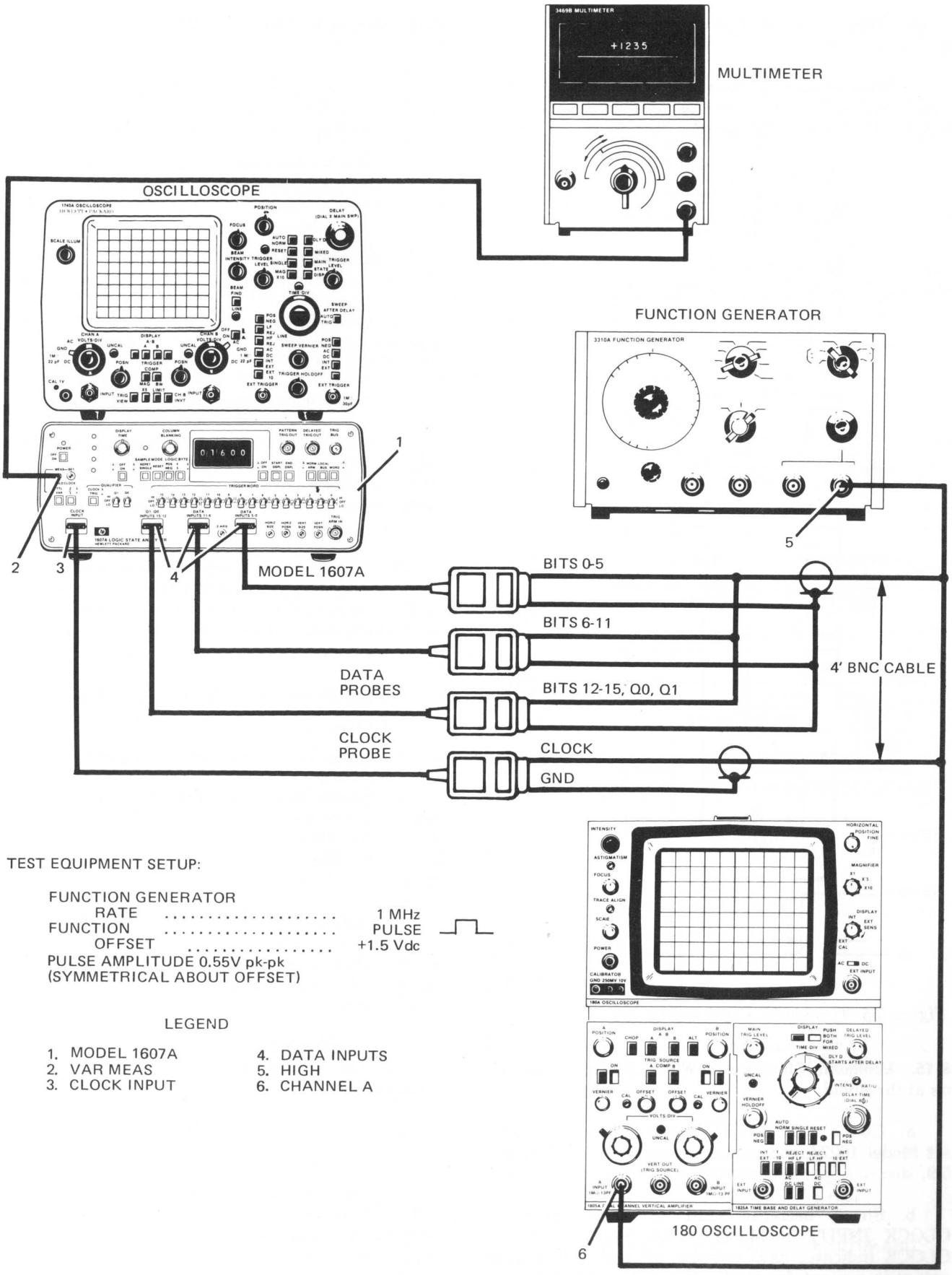
r. Repeat step h.

s. Apply test waveform shown in figure 5-5E to clock- and data-probe inputs.

t. Adjust VAR SET for valid clock and data inputs (indicator lights off).

u. With multimeter connected to VAR MEAS, adjust VAR SET from —1 Vdc to —10 Vdc. Verify that Model 1607A remains triggered.

v. Apply test waveform shown in figure 5-5F to clock- and data-probe inputs.




TEST EQUIPMENT SETUP:

FUNCTION GENERATOR
RATE ..... 1 MHz
FUNCTION ..... PULSE
OFFSET ..... +1.5 Vdc
PULSE AMPLITUDE 0.55V pk-pk
(SYMMETRICAL ABOUT OFFSET)

LEGEND

1. MODEL 1607A
2. VAR MEAS
3. CLOCK INPUT
4. DATA INPUTS
5. HIGH
6. CHANNEL A

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*Figure 5-4. Threshold/Logic Swing Test Setup*

w. Adjust VAR SET to obtain trigger (indicator lights off).

x. With multimeter connected to VAR MEAS, adjust VAR SET from +1 Vdc to +10 Vdc. Verify that Model 1607A remains triggered.

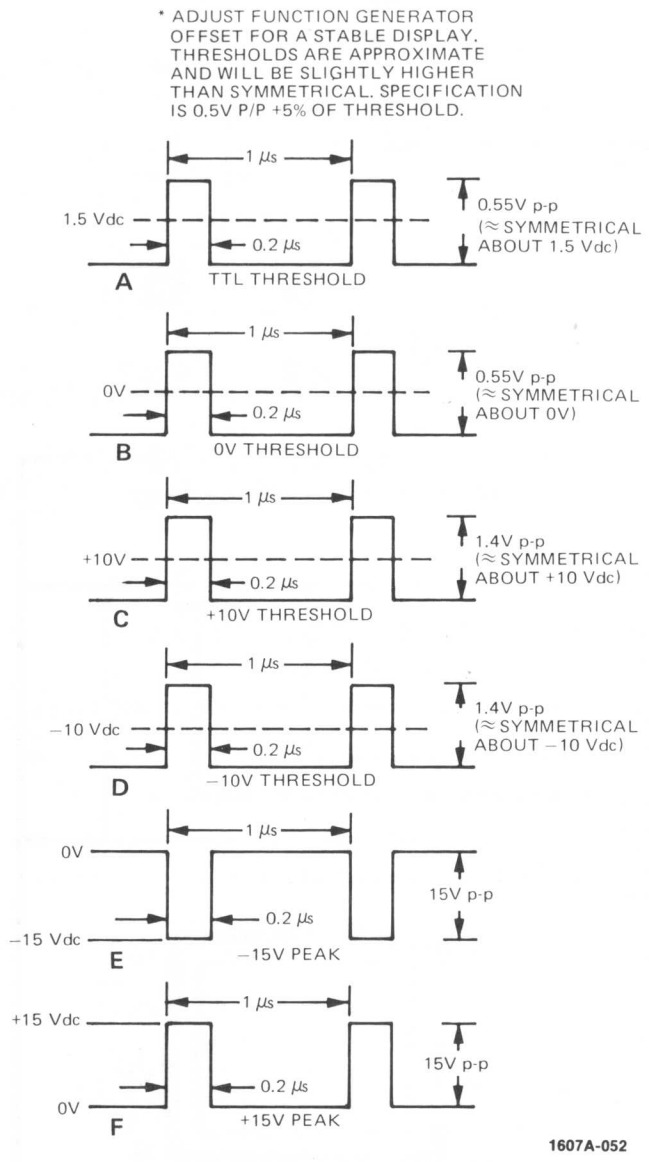



*Figure 5-5. Threshold/Logic Swing Test Waveforms*

**5-15. Minimum Clock-pulse Width.** Specification: 20 ns at threshold.

a. Connect test setup as shown in figure 5-1 and set Model 1607A controls as described in paragraph 5-9, step c. Apply test waveforms shown in figure 5-3.

b. Slowly decrease width of pulse applied to CLOCK INPUT of Model 1607A. Verify that NO CLOCK indicator light remains off and that trigger output is present for clock-pulse widths greater than or equal to 20 ns.

**5-16. Minimum Data-pulse Width.** Specification: 25 ns at threshold.

a. Connect test setup as shown in figure 5-1 and set Model 1607A controls as described in paragraph 5-9, step c. Apply test waveforms shown in figure 5-3.

b. Slowly decrease width of pulse applied to DATA INPUTS of Model 1607A. Observe that Model 1607A remains triggered for pulse widths greater than or equal to 25 ns.

**5-17. Setup and Hold Time.** Specification: Setup Time, 20 ns minimum; Hold Time, 0 ns minimum.

a. Connect test setup as shown in figure 5-1, and set Model 1607A controls as described in paragraph 5-9, step c.

b. Apply waveforms shown in figure 5-6A.

c. Slowly decrease delay time between leading edge (⌐¬) of clock pulse and leading edge (⌐¬) of data pulse. Observe that Model 1607A remains triggered and display is stable for delay times greater than or equal to 20 ns.

d. Adjust delay time between pulses so that trailing edge (¬⌐) of data pulse is coincident with leading edge (⌐¬) of clock pulse as shown in figure 5-6A (hold time). Observe that stable display occurs for 0 hold time.

e. Switch Model 1607A clock slope to (¬⌐). Complement pulse generator output to clock probe.

f. Apply waveform shown in figure 5-6B.

g. Slowly decrease delay time between leading edge (¬⌐) of clock pulse and leading edge (⌐¬) of data pulse. Observe that Model 1607A remains triggered and display is stable for delay times greater than or equal to 20 ns.

h. Adjust delay time between pulses so that trailing edge (¬⌐) of data pulse is coincident with leading edge (¬⌐) of clock pulse as shown in figure 5-6B (hold time). Observe stable display for 0 hold time.

i. Complement output of pulse generator to data probes, and set all Model 1607A TRIGGER WORD switches to LO.

j. Apply waveforms shown in figure 5-6C.

k. Slowly decrease delay time between leading edge (¬⌐) of clock pulse and leading edge (¬⌐) of data pulse. Observe that Model 1607A remains triggered and stable display of all zeros occurs for delay times greater than or equal to 20 ns.

l. Adjust delay time between pulses so that

trailing edge (⌐¬) of data pulse is coincident with leading edge (¬⌐) of clock pulse as shown in figure 5-6C (hold time). Observe that stable display occurs for 0 hold time.

m. Switch Model 1607A clock slope to (⌐¬) and set pulse generator clock output to normal.

n. Apply waveforms shown in figure 5-6D.

o. Slowly decrease delay time between leading edge (⌐¬) of clock pulse and leading edge (¬⌐) of data pulse. Observe that Model 1607A remains triggered and display is stable for delays greater than or equal to 20 ns.

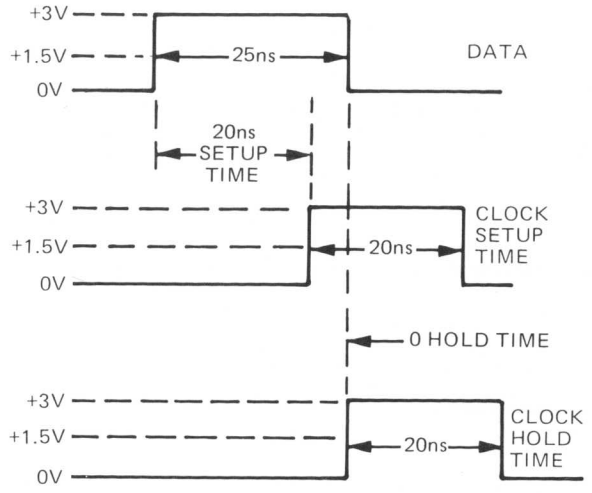
p. Adjust delay time between pulses so that trailing edge (⌐¬) of data pulse is coincident with leading edge (⌐¬) of clock pulse as shown in figure 5-6D (hold time). Observe that stable display occurs for 0 hold time.

**5-18. Trigger Arm Input.** Specification: Input Impedance, 50 ohms; Input Levels, 0 V ≤LOW <0.4 V, 2 V <HIGH <5 V; Pulse Width, 15 ns minimum at 1.5 V.

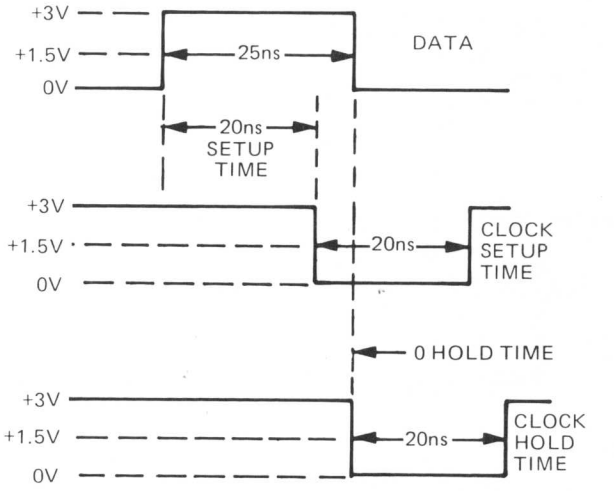
a. Remove power from the Model 1607A.

b. Using multimeter, measure input impedance of the trigger arm input. Observe that measured value is 50 (±2) ohms.

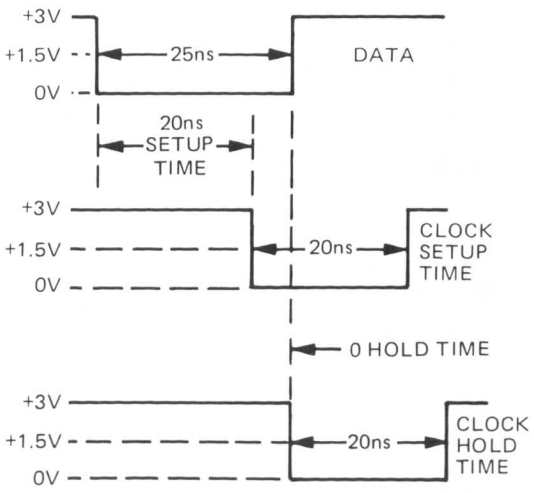
c. Reapply power to Model 1607A.



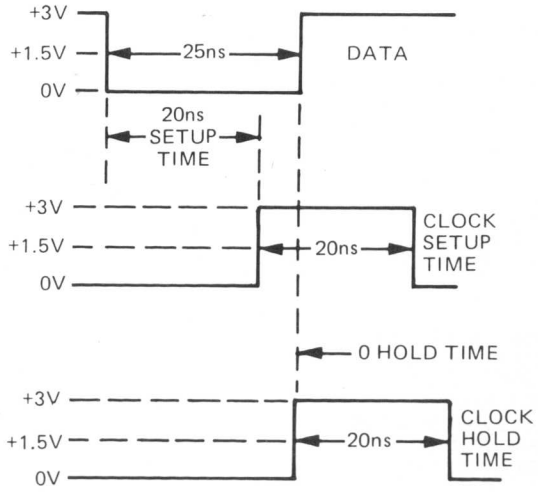

A. POSITIVE DATA/POSITIVE CLOCK SETUP AND HOLD TIMES




B. POSITIVE DATA/NEGATIVE CLOCK SETUP AND HOLD TIMES



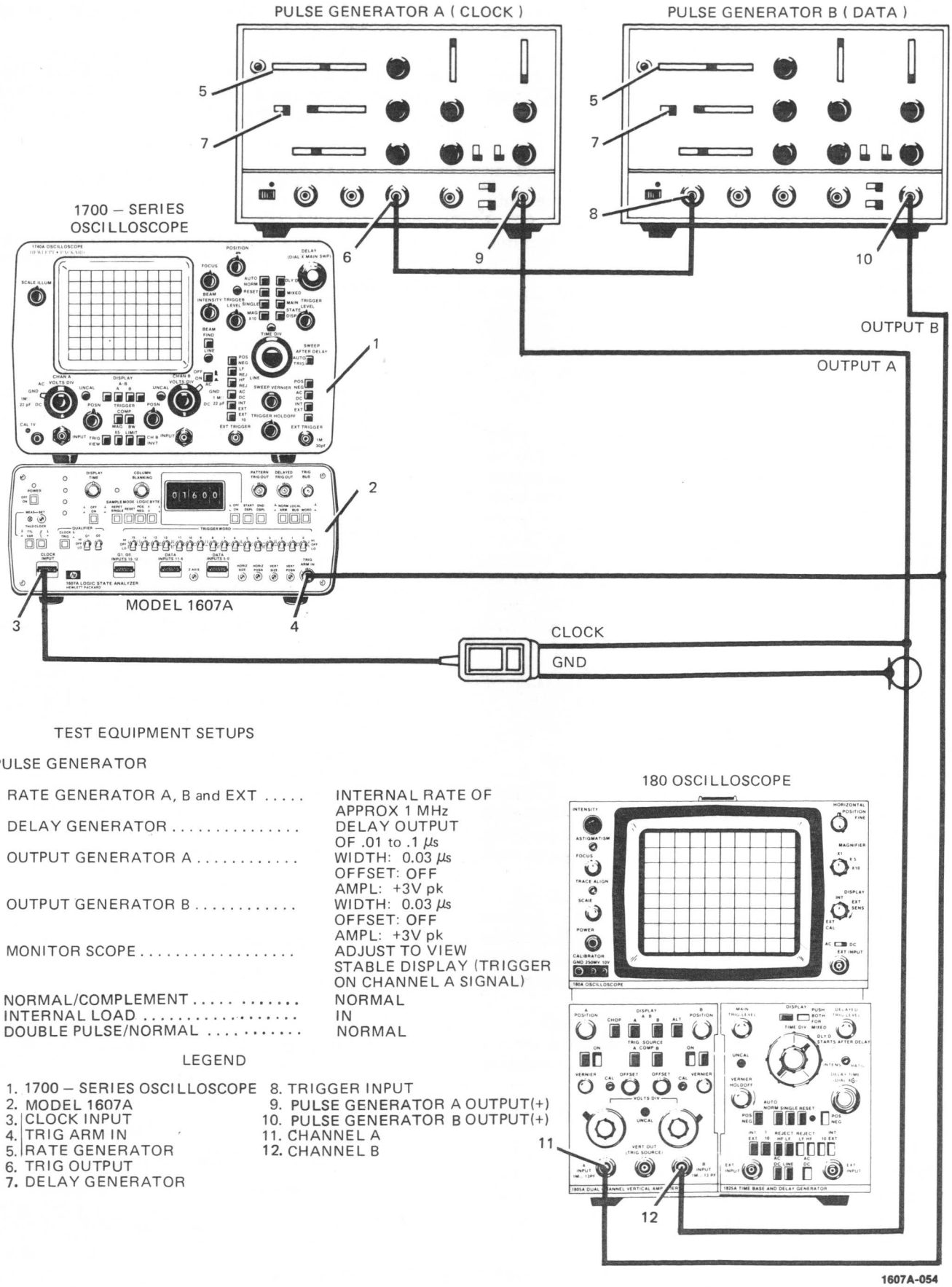

C. NEGATIVE DATA/NEGATIVE CLOCK SETUP AND HOLD TIME




D. NEGATIVE DATA/POSITIVE CLOCK SETUP AND HOLD TIME

1607A-053

*Figure 5-6. Setup and Hold Waveforms*




TEST EQUIPMENT SETUPS

PULSE GENERATOR

| | |
|---|---|
| RATE GENERATOR A, B and EXT ..... | INTERNAL RATE OF APPROX 1 MHz |
| DELAY GENERATOR ..... | DELAY OUTPUT OF .01 to .1 μs |
| OUTPUT GENERATOR A ..... | WIDTH: 0.03 μs<br>OFFSET: OFF<br>AMPL: +3V pk |
| OUTPUT GENERATOR B ..... | WIDTH: 0.03 μs<br>OFFSET: OFF<br>AMPL: +3V pk |
| MONITOR SCOPE ..... | ADJUST TO VIEW STABLE DISPLAY (TRIGGER ON CHANNEL A SIGNAL) |
| NORMAL/COMPLEMENT ..... | NORMAL |
| INTERNAL LOAD ..... | IN |
| DOUBLE PULSE/NORMAL ..... | NORMAL |

LEGEND

1. 1700 – SERIES OSCILLOSCOPE
2. MODEL 1607A
3. CLOCK INPUT
4. TRIG ARM IN
5. RATE GENERATOR
6. TRIG OUTPUT
7. DELAY GENERATOR
8. TRIGGER INPUT
9. PULSE GENERATOR A OUTPUT(+)
10. PULSE GENERATOR B OUTPUT(+)
11. CHANNEL A
12. CHANNEL B

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*Figure 5-7. Trigger Arm Test Setup*

d. Set Model 1607A controls as follows:

| | |
|---|---|
| CLOCK | ⎍ |
| THLD | TTL |
| QUALIFIERS Q0, Q1 | OFF |
| SAMPLE MODE | REPET |
| START DSPL | ON |
| TRIGGER MODE | |
| NORM/ARM | ARM |
| LOCAL/BUS | LOCAL |
| WORD | ON |
| TRIGGER WORD | all LO |

e. Connect test equipment as shown in figure 5-7, and apply waveforms shown in figure 5-8 to CLOCK INPUT and TRIG ARM input.

f. Connect PATTERN TRIG OUT from Model 1607A to channel A or oscilloscope. Trigger oscilloscope on channel A input.

g. Set oscilloscope control for sweep speed of 5 ms and pulse generator to single pulse.

h. Press pulse generator pushbutton for single pulse. Observe that a sweep occurs for every pulse input.

i. Reset test setup to settings shown in figure 5-7, and apply waveforms shown in figure 5-8.

j. Adjust pulse generator delays from 45 ns to greater than or equal to 75 ns.

k. Set oscilloscope control for sweep speed of 5 ms and pulse generator to single pulse.

l. Depress pulse generator manual (single pulse) pushbutton. Observe that triggered sweep occurs every other pulse input. This verifies the trigger arming conditions specified in table 1-1.

**5-19. Display Time.** Specification: Variable from <50 ms to >5 s.

a. Set up equipment per paragraph 5-9, steps a, b, and c.

b. Remove power from Model 1607A and remove bottom cover.

c. Set up timer counter to measure period, and connect timer counter input to A1U68, pin 10.

**CAUTION**

Use care to prevent shorting between adjacent pins.

d. Apply power and observe timer counter measurement while varying DISPLAY TIME control from full CCW to full CW positions. Measurements should vary from less than 50 ms for full CCW position of DISPLAY TIME to greater than five seconds for full CW position.

**5-20. Pattern Trigger and Delayed Trigger Outputs.** Specification: High, >2 V into 50 ohms; Low, <0.4 V into 50 ohms; Width, ≈25 ns (synchronous).

a. Set up equipment per paragraph 5-9, steps a, b, and c.

b. Connect PATTERN TRIG OUT and DELAYED TRIG OUT to channels A and B inputs respectively of oscilloscope.

c. Set delay to all 0's. Observe that output pulses meet specifications listed above.

**5-21. Horizontal Output.** Specification: <0.6 V to >6 V p-p, ±8 V maximum into >100 kΩ.

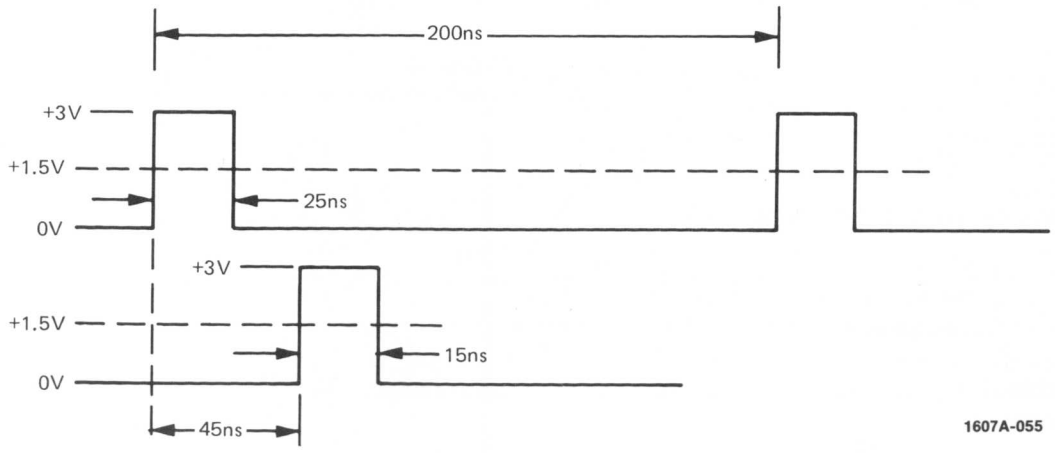



*Figure 5-8. Trigger Arm Input Test Waveforms*

a. Set Model 1607A controls as follows:

| | |
|---|---|
| POWER | ON |
| TRIGGER MODE | WORD |
| TRIGGER WORD switches | all OFF |
| SAMPLE MODE | SINGLE |
| COLUMN BLANKING | full CCW |
| QUALIFIER Q0, Q1 | OFF |
| Z-AXIS | ON |
| All Other Pushbuttons | out position |

b. Monitor HORIZ output at rear panel.

c. Set HORIZ SIZE fully CCW and adjust HORIZ POSN for approximately 0 volts. Observe that ramp is <0.6 volts p-p.

d. Set HORIZ SIZE to full CW position. Observe that ramp is >6 volts p-p.

e. Adjust HORIZ POSN from full CCW position to full cw position while observing offset.

**5-22. Vertical Output.** Specification: <0.6 V to >6 V p-p, ±8 V maximum into >100 kΩ.

a. Monitor VERT output at rear panel.

b. Set VERT SIZE to full CCW position and adjust VERT POSN for approximately 0 volts. Observe that ramp is <0.6 volts p-p.

c. Set VERT SIZE to full CW position and observe that ramp is >6 volts p-p.

d. Adjust VERT POSN from full CCW to full CW while observing offset.

**5-23. Z-axis Output.** Specification: 0 V to 10 V p-p into >1000 ohms.

a. Connect monitor oscilloscope to Z-AXIS BNC on Model 1607A rear panel.

b. Set Model 1607A Z-AXIS switch to ON position.

c. Turn front panel Z-AXIS adjustment from full CCW to full CW position while observing Z-AXIS output. Output should vary from 0 V to greater than 10 V p-p.

## 5-24. ADJUSTMENT PROCEDURES.

**WARNING**

Read the Safety Summary at the front of this manual before performing adjustment procedures.

5-25. The following adjustment procedures for the Model 1607A should be performed only if it has previously been established by the performance checks that the instrument is out of adjustment. The adjustments can be made separately following repairs to the instrument or in sequence as part of a periodic calibration procedure. The location of adjustments and test points are shown in figures accompanying the adjustment procedures.

**CAUTION**

Adjustments are performed with top and bottom covers removed. Use care to avoid shorting or damaging internal parts of the instrument.

**5-26. +5 VOLT POWER SUPPLY ADJUSTMENT. (See schematic 2 and figure 5-9.)**

a. Remove power from Model 1607A.

b. Remove top and bottom covers.

c. Apply power to Model 1607A.

d. While monitoring +5-volt power supply at test point TP1 with respect to ground (TP2), adjust A3R8 for +5 V ±0.01 V.

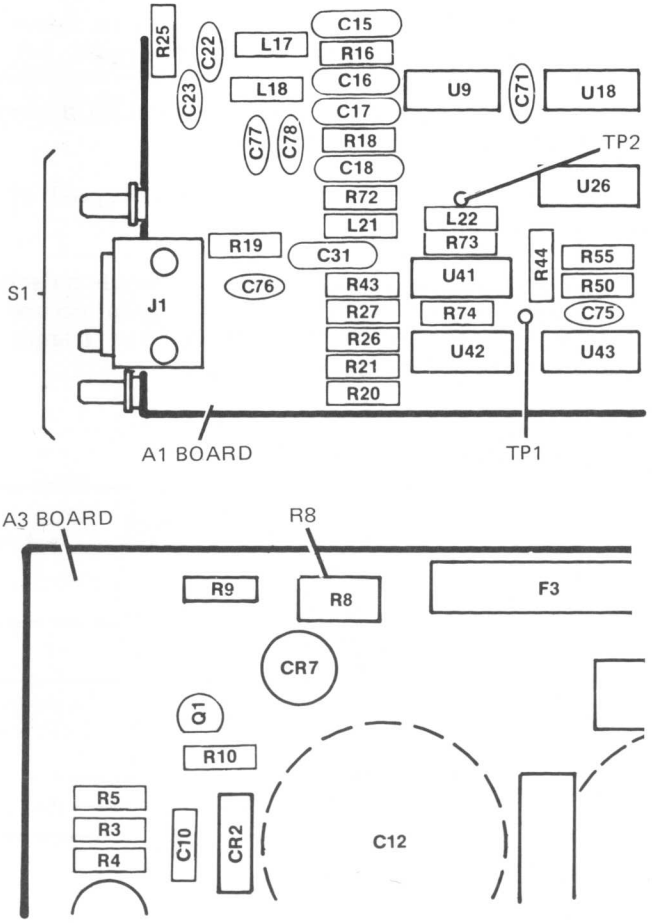



*Figure 5-9. +5 Volt Power Supply Adjustment Location*

**5-27. TIMING ADJUSTMENTS. (See schematic 9 and figures 5-10 and 5-11.)**

a. Set up equipment as shown in figure 5-1.

b. Perform steps b and c of paragraph 5-9.

c. Switch TRIGGER WORD bit 0 to LO and set Model 1607A to END DSPL mode. Verify that NO TRIG light is on.

d. Disconnect monitor oscilloscope inputs from pulse generator outputs.

e. Externally trigger monitor oscilloscope from clock pulse (OUTPUT A).

f. Set oscilloscope sweep for 5 ns/cm and oscilloscope vertical sensitivity for 1 volt with X10 probe.

g. Adjust pulse generator rate for 10 MHz.

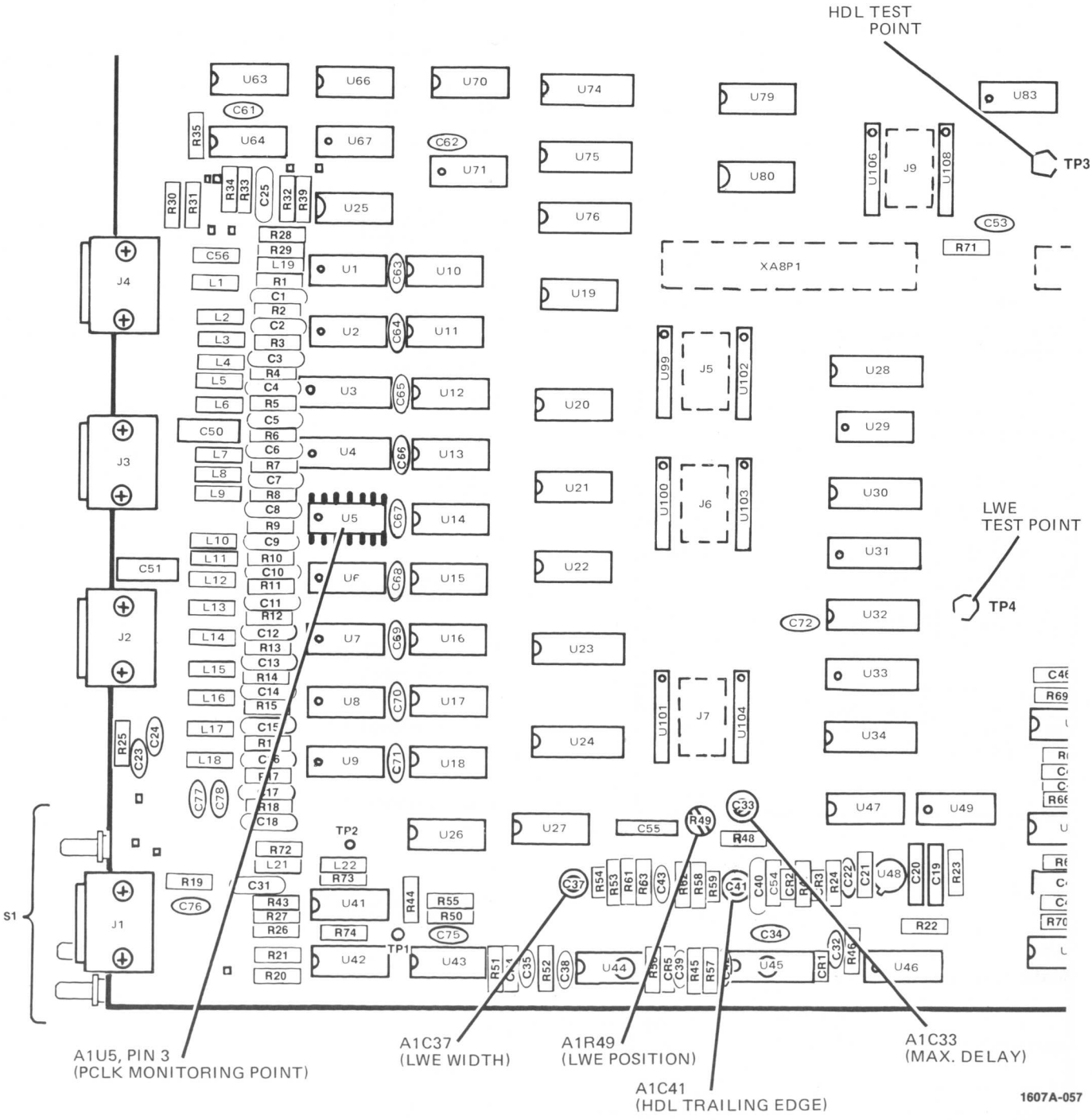



*Figure 5-10. Timing Adjustment Locations*

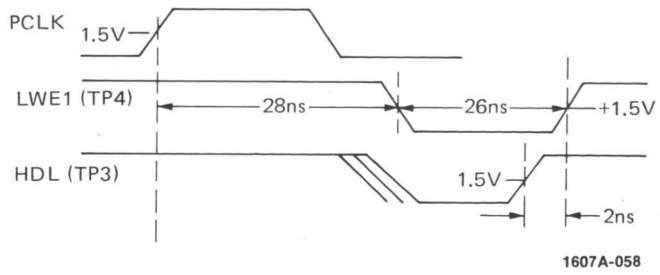



*Figure 5-11. Timing Adjustment Waveforms*

h. Monitor PCLK at A1U5, pin 3. Adjust monitor oscilloscope to position 1.5 V point on positive edge of PCLK at a reference point.

i. Monitor LWE at A1TP4. Adjust A1C33 for maximum delay between LWE and PCLK.

j. Adjust A1R49 to position LWE 28 ns from PCLK reference.

k. Adjust A1C37 to obtain 26 ns width for LWE.

l. Monitor delay clock (HDL) at A1TP3. Set trailing edge of HDL two nanoseconds in advance of trailing edge of LWE by adjusting A1C41.

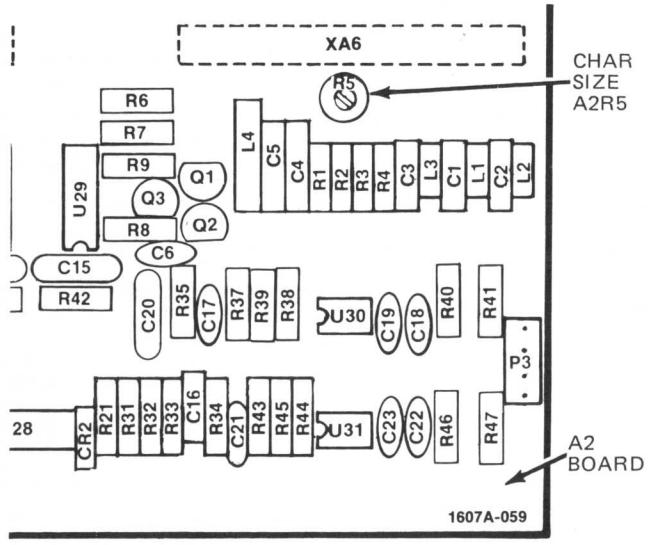



*Figure 5-12. Character Size Adjustment Location*

**5-28. CHARACTER SIZE ADJUSTMENT. (See schematic 13 and figure 5-12.)**

a. Perform paragraph 3-39, steps a thru h of the operator's checks and adjustments in Section III.

b. Adjust character size A2R5 for slight space between zeros. Displayed characters should be as large as possible without overlap.

## 5-29. CUSTOMER MODIFICATIONS.

**5-30. RESET.** as shipped from the factory, the Model 1600A RESET pushbutton controls only the Model 1600A. If it is desirable to control both the Model 1600A and the Model 1607A with the Model 1600A RESET, modify the Model 1607A Display Board Assembly A2 (see figure 5-13) as follows:

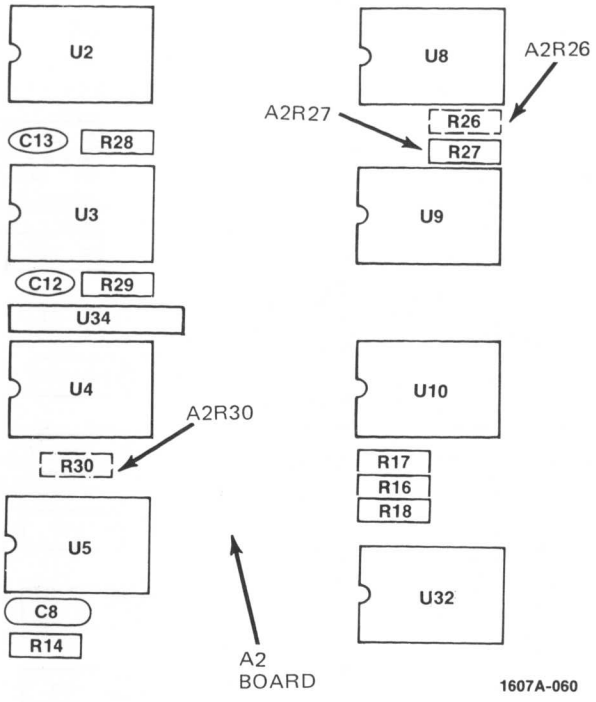



*Figure 5-13. Reset Modification Location*

a. Turn off instrument power and remove power cable from rear-panel connector.

b. Removal A2 board (refer to disassembly procedure in Section VIII).

c. Remove 10-ohm resistor A2R27 (factory installed).

d. Install 10-ohm resistors A2R26 and A2R30 (not installed at factory).

e. Reinstall A2 board.

**NOTE**

This modification affects instrument operation in the bus mode only. The Model 1607A reset circuit will function normally when used with an oscilloscope.

## PERFORMANCE CHECK RECORD

## MODEL 1607A

Instrument Serial Number _____ Date _____

| Check | Specification | Measured |
|---|---|---|
| **INITIAL OPERATIONAL CHECK DISPLAY** | 16 Bits<br>16 Words<br>all ones | |
| **REPETITION RATE** | 20 MHz<br>maximum | _____ |
| **INPUT RC** | | |
| Input Resistance | 40 kΩ ±3 kΩ | _____ |
| Shunt Capacitance | ≤14 pF | _____ |
| **INPUT BIAS CURRENT** | | |
| Clock & Probe Inputs | ≤30 μA | _____ |
| **INPUT THRESHOLD/SWING** | .5 V +5% of THLD | |
| VAR MEAS/SET Swing | ≥ +10 Vdc | _____ |
| | ≤—10 Vdc | _____ |
| 0 V Threshold | Valid Data | _____ |
| +10 V Threshold | Valid Data | _____ |
| —10 V Threshold | Valid Data | _____ |
| —15 V Peak | Valid Data | _____ |
| +15 V peak | Valid Data | _____ |
| **MINIMUM CLOCK PULSE WIDTH** | | |
| Applied pulses >20 ns | 20 ns minimum | _____ |
| **MINIMUM DATA PULSE** | | |
| Applied pulse >25 ns | 25 ns minimum | _____ |
| **SET UP and HOLD TIME** | | |
| Set up Time | 20 ns minimum | _____ |
| Hold Time | 0 ns minimum | _____ |
| **TRIGGER ARM INPUT** | | |
| Input Impedance | 50Ω ±2Ω | _____ |
| Levels | | |
| HI | >2 V, <5 V | _____ |
| LO | >0 V, <0.4 V | _____ |
| Arming Condition | <45 ns | _____ |
| | >75 ns | _____ |

## PERFORMANCE CHECK RECORD (Cont'd)

## MODEL 1607A

Instrument Serial Number _____ Date _____

| Check | Specification | Measured |
|---|---|---|
| **DISPLAY** | | |
| Display Time CCW | <50 ms | _____ |
| Display Time CW | >5 sec | _____ |
| **PATTERN TRIGGER and DELAY TRIGGER OUTPUTS** | into 50Ω | _____ |
| Pattern Trigger Output | 2 V < HI >5 V pk | _____ |
| | 0 V < LO >.4 V pk | _____ |
| Delay Trigger Output | 2 V < HI >5 V pk | _____ |
| | 0 V < LO >.4 V pk | _____ |
| WIDTH | ≈25 ns | _____ |
| | Synchronous | _____ |
| **HORIZONTAL, VERTICAL, and Z-AXIS OUTPUTS** | | |
| Horizontal Output | <0.6 V to >6 V p-p, ±8 V max into 100 kΩ | _____ |
| Vertical Output | <0.6 V to >6 V p-p, ±8 V max into 100 kΩ | _____ |
| Z-axis Output | >10 V p-p | _____ |

# SECTION VI

# REPLACEABLE PARTS

## 6-1. INTRODUCTION.

6-2. This section contains information for ordering replacement parts. The abbreviations used in the parts list are described in table 6-1. Table 6-2 lists the parts in alphanumeric order by reference designation and includes the manufacturer and manufacturer's part number. Table 6-3 contains the list of manufacturers' codes.

## 6-3. ORDERING INFORMATION.

6-4. To obtain replacement parts from Hewlett-Packard, address order or inquiry to the nearest Hewlett-Packard Sales/Service Office and supply the following information:

a. Instrument model and serial number.

b. HP part number of item(s).

c. Quantity of part(s) desired.

d. Reference designation of part(s).

6-5. To order a part not listed in the table, provide the following information:

a. Instrument model and serial number.

b. Description of the part, including function and location in the instrument.

c. Quantity desired.

Table 6-1. Abbreviations for Replaceable Parts List

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| A | AMPERE(S) | H | HENRY(IES) | NPN | NEGATIVE-POSITIVE-NEGATIVE | RWV | REVERSE WORKING VOLTAGE |
| ASSY | ASSEMBLY | HG | MERCURY | | | | |
| | | HP | HEWLETT-PACKARD | NSR | NOT SEPARATELY REPLACEABLE | S-B | SLOW-BLOW |
| BD | BOARD(S) | HZ | HERTZ | | | SCR | SILICON CONTROLLED RECTIFIER |
| BH | BINDER HEAD | | | | | | |
| BP | BANDPASS | IF | INTERMEDIATE FREQ. | | | SE | SELENIUM |
| | | IMPG | IMPREGNATED | OBD | ORDER BY DESCRIPTION | SEC | SECOND(S) |
| C | CENTI ($10^{-2}$) | INCD | INCANDESCENT | | | SECT | SECTION(S) |
| CAR | CARBON | INCL | INCLUDE(S) | OH | OVAL HEAD | SI | SILICON |
| CCW | COUNTERCLOCKWISE | INS | INSULATION(ED) | OX | OXIDE | SIL | SILVER |
| CER | CERAMIC | INT | INTERNAL | | | SL | SLIDE |
| CMO | CABINET MOUNT ONLY | | | P | PEAK | SP | SINGLE POLE |
| COAX | COAXIAL | K | KILO ($10^{3}$) | PC | PRINTED (ETCHED) CIRCUIT(S) | SPL | SPECIAL |
| COEF | COEFFICIENT | KG | KILOGRAM | | | ST | SINGLE THROW |
| COMP | COMPOSITION | | | PF | PICOFARADS | STD | STANDARD |
| CONN | CONNECTOR(S) | LB | POUND(S) | PHL | PHILLIPS | | |
| CRT | CATHODE-RAY TUBE | LH | LEFT HAND | PIV | PEAK INVERSE VOLTAGE(S) | TA | TANTALUM |
| CW | CLOCKWISE | LIN | LINEAR TAPER | | | TD | TIME DELAY |
| | | LOG | LOGARITHMIC TAPER | PNP | POSITIVE-NEGATIVE-POSITIVE | TFL | TEFLON |
| D | DECI ($10^{-1}$) | LPF | LOW-PASS FILTER(S) | | | TGL | TOGGLE |
| DEPC | DEPOSITED CARBON | LVR | LEVER | P/O | PART OF | THYR | THYRISTOR |
| DP | DOUBLE POLE | | | PORC | PORCELAIN | TI | TITANIUM |
| DT | DOUBLE THROW | M | MILLI ($10^{-3}$) | POS | POSITION(S) | TNLDIO | TUNNEL DIODE(S) |
| | | MEG | MEGA ($10^{6}$) | POT | POTENTIOMETER(S) | TOL | TOLERANCE |
| ELECT | ELECTROLYTIC | MET FILM | METAL FILM | P-P | PEAK-TO-PEAK | TRIM | TRIMMER |
| ENCAP | ENCAPSULATED | MET OX | METAL OXIDE | PRGM | PROGRAM | | |
| EXT | EXTERNAL | MFR | MANUFACTURER | PS | POLYSTYRENE | | |
| | | MINAT | MINIATURE | PWV | PEAK WORKING VOLTAGE | U | MICRO ($10^{-6}$) |
| F | FARAD(S) | MOM | MOMENTARY | | | | |
| FET | FIELD-EFFECT TRANSISTOR(S) | MTG | MOUNTING | | | V | VOLTS |
| | | MY | MYLAR | RECT | RECTIFIER(S) | VAR | VARIABLE |
| FH | FLAT HEAD | | | RF | RADIO FREQUENCY | VDCW | DC WORKING VOLT(S) |
| FIL H | FILLISTER HEAD | N | NANO ($10^{-9}$) | RFI | RADIO FREQUENCY INTERFERENCE | | |
| FXD | FIXED | N/C | NORMALLY CLOSED | | | W | WATT(S) |
| | | NE | NEON | RH | ROUND HEAD OR RIGHT HAND | W/ | WITH |
| G | GIGA ($10^{9}$) | N/O | NORMALLY OPEN | | | WIV | WORKING INVERSE VOLTAGE |
| GE | GERMANIUM | NOP | NEGATIVE POSITIVE ZERO (ZERO TEMPERATURE COEFFICIENT) | | | | |
| GL | GLASS | | | RMO | RACK MOUNT ONLY | W/O | WITHOUT |
| GRD | GROUNDED | | | RMS | ROOT MEAN SQUARE | WW | WIREWOUND |

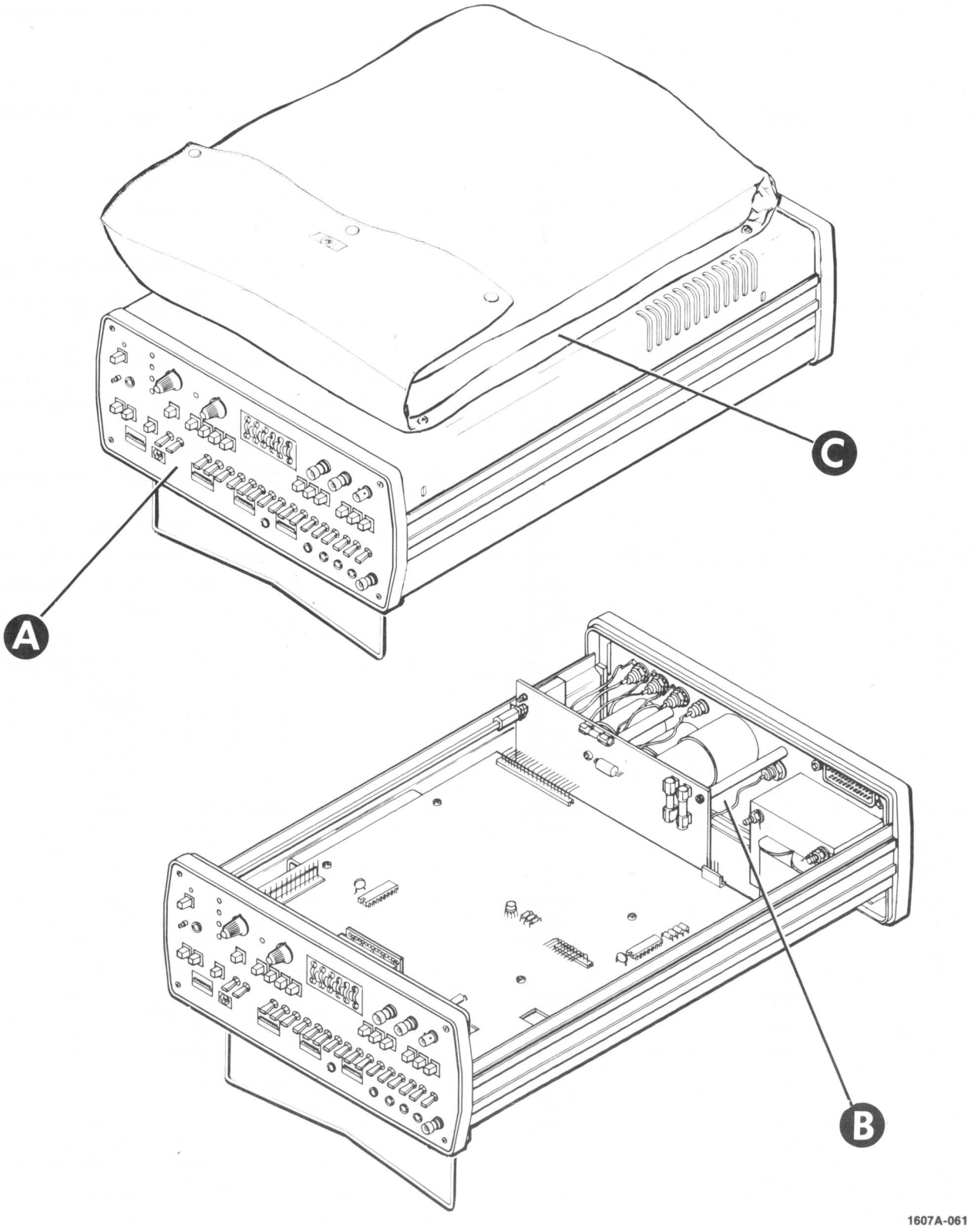



*Figure 6-1. Illustrated Parts Breakdown (Sheet 1 of 3)*

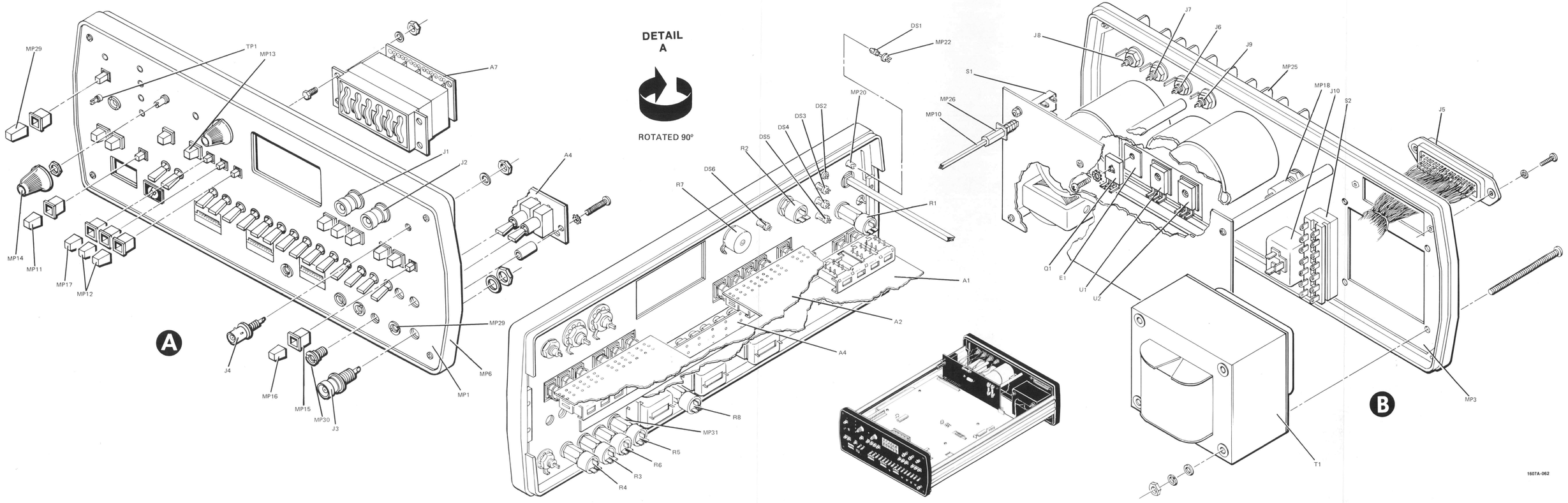



*Figure 6-1.*
*Illustrated Parts Breakdown (Sheet 2 of 3)*

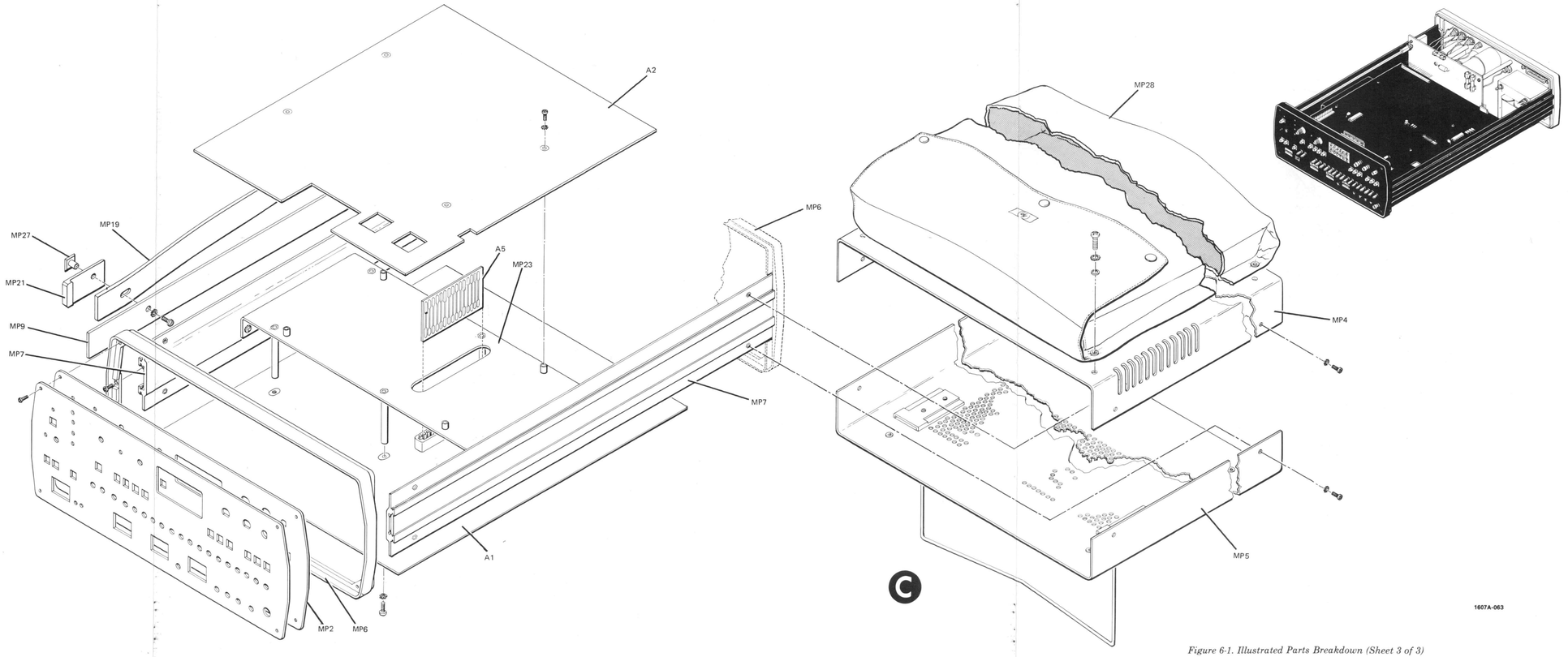



*Figure 6-1. Illustrated Parts Breakdown (Sheet 3 of 3)*

## Table 6-2. Replaceable Parts

| Reference Designation | HP Part Number | Qty | Description | Mfr Code | Mfr Part Number |
|---|---|---|---|---|---|
| A1 | 01600-66511 | | BOARD ASSY, DATA ACQUISITION | 28480 | 01600-66511 |
| A2 | 01607-66504 | | BOARD ASSY, DISPLAY | 28480 | 01607-66504 |
| A3 | 01607-66502 | | BOARD ASSY, LOW VOLTAGE P.S. | 28480 | 01607-66502 |
| A4 | 01600-66506 | | BOARD ASSY, TRIGGER SWITCH | 28480 | 01600-66506 |
| A5 | 01607-26503 | | BOARD, PRINTED CIRCUIT | 28480 | 01607-26503 |
| A6 | 01607-26503 | | BOARD, PRINTED CIRCUIT | 28480 | 01607-26503 |
| A7 | 01600-66510 | | BOARD ASSY, DIGITAL SWITCH | 28480 | 01600-66510 |
| CR1 | 1901-0511 | 1 | DIODE-PWR RECT 1N3889R 200NS 50V 12A | 12954 | 1N3889R |
| DS1 | 1990-0486 | 5 | LED-VISIBLE | 28480 | 1990-0486 |
| DS2 | 1990-0486 | | LED-VISIBLE | 28480 | 1990-0486 |
| DS3 | 1990-0486 | | LED-VISIBLE | 28480 | 1990-0486 |
| DS4 | 1990-0486 | | LED-VISIBLE | 28480 | 1990-0486 |
| DS5 | 1990-0486 | | LED-VISIBLE | 28480 | 1990-0486 |
| DS6 | 2140-0016 | 1 | LAMP, INCAND, BULB T-1, 5V | 71744 | 683 |
| E1 | 0340-0511 | 1 | INSULATOR, TRANSISTOR | 13103 | 43-77-2 |
| F1 | 2110-0007 | 1 | FUSE 1A 250V SLO-BLO 1.25X.25 | 71400 | MDL-1 |
| J1 | 1250-0083 | 7 | CONNECTOR-RF BNC FEM SGL HOLE FR | 24931 | 28JR-130-1 |
| J2 | 1250-0083 | | CONNECTOR-RF BNC FEM SGL HOLE FR | 24931 | 28JR-130-1 |
| J3 | 1250-0083 | | CONNECTOR-RF BNC FEM SGL HOLE FR | 24931 | 28JR-130-1 |
| J4 | 1250-0659 | 1 | | 28480 | 1250-0659 |
| J5 | 1251-0085 | 1 | CONNECTOR, 36-CONT, FEM, MICRO RIBBON | 71785 | 57-40360-375 |
| J6 | 1250-0083 | | CONNECTOR-RF BNC FEM SGL HOLE FR | 24931 | 28JR-130-1 |
| J7 | 1250-0083 | | CONNECTOR-RF BNC FEM SGL HOLE FR | 24931 | 28JR-130-1 |
| J8 | 1250-0083 | | CONNECTOR-RF BNC FEM SGL HOLE FR | 24931 | 28JR-130-1 |
| J9 | 1250-0083 | | CONNECTOR - RF BNC FEM SGL HOLE FR | 24931 | 28JR-130-1 |
| J10 | 1251-2357 | 1 | CONNECTOR, AC POWER HP-9 MALE FLANGE | 28480 | 1251-2357 |
| MP1 | 01607-00202 | 1 | PANEL, FRONT | 28480 | 01607-00202 |
| MP2 | 01607-00203 | 1 | PANEL, SUB | 28480 | 01607-00203 |
| MP3 | 01607-00204 | 1 | PANEL, REAR | 28480 | 01607-00204 |
| MP4 | 01607-04101 | 1 | COVER, TOP | 28480 | 01607-04101 |
| MP5 | 01607-04102 | 1 | COVER, BOTTOM | 28480 | 01607-04102 |
| MP6 | 01620-20501 | 2 | FRAME, CASTING | 28480 | 01620-20501 |
| MP7 | 01607-23701 | 2 | RAIL, SIDE | 28480 | 01607-23701 |
| MP8 | 01607-07201 | 1 | TRIM, SIDE RAIL | 28480 | 01607-07201 |
| MP9 | 01607-07202 | 1 | TRIM, SIDE RAIL | 28480 | 01607-07202 |
| MP10 | 01607-23201 | 1 | EXTENSION, SWITCH | 28480 | 01607-23201 |
| MP11 | 0370-0603 | 1 | PUSHBUTTON:SQUARE, MINT GRAY | 28480 | 0370-0603 |
| MP12 | 0370-0671 | 1 | PUSHBUTTON, LEG BLU | 28480 | 0370-0671 |
| MP13 | 0370-0684 | 1 | PUSHBUTTON, HARVEST GOLD | 28480 | 0370-0684 |
| MP14 | 0370-1005 | 2 | KNOB; BASE; PTR; .375 IN; JGK; SGI | 28480 | 0370-1005 |
| MP15 | 0370-2626 | 15 | BEZEL, PB GRAY | 28480 | 0370-2626 |
| MP16 | 0370-2630 | 1 | PUSHBUTTON, WIL GRN | 28480 | 0370-2630 |
| MP17 | 0370-2790 | 1 | PUSHBUTTON, YEL-ORN | 28480 | 0370-2790 |
| MP18 | 1400-0084 | 1 | FUSEHOLDER-EXTR POST 15A 250V UL | 28480 | 1400-0084 |
| MP19 | 1440-0103 | 1 | HANDLE; SPCL 12.5 L .12 THK | 28480 | 1440-0103 |
| MP20 | 1450-0404 | 1 | LIGHT-IND LENS CAP CLR TL LENS | 28480 | 1450-0404 |
| MP21 | 5040-7042 | 2 | CAP, PLASTIC | 28480 | 5040-7042 |
| MP22 | 00183-67701 | 1 | BASE, PILOT LIGHT | 28480 | 00183-67701 |
| MP23 | 01607-01201 | 1 | BRACKET, MOUNTING | 28480 | 01607-01201 |
| MP24 | 01607-24701 | 3 | SPACER, POWER SUPPLY | 28480 | 01607-24701 |
| MP25 | 01720-20503 | 1 | HEAT SINK | 28480 | 01720-20503 |
| MP26 | 01830-23201 | 1 | COUPLER, SWITCH EXTENSION | 28480 | 01830-23201 |
| MP27 | 03580-24706 | 1 | NUT | 28480 | 03580-24706 |
| MP28 | 1540-0292 | 1 | CASE - ACCESS PVC 10.5 - LG 1.5 - WD 13.5-DP | 28480 | 1540-0292 |
| MP29 | 0370-2826 | 1 | PUSHBUTTON, CORP WHT | 28480 | 0370-2826 |
| MP30 | 1490-0968 | 5 | BUSHING: POT | 28480 | 1490-0968 |
| MP31 | 0590-0043 | 6 | NUT; HEX, DBL CHAM | 28480 | 0590-0043 |
| Q1 | 1854-0433 | 1 | TRANSISTOR NPN SI PD = 90W FT = 2MHZ | 28480 | 1854-0433 |
| R1 | 2100-2635 | 3 | RESISTOR-VAR 50K 20% CC | 01121 | TYPE W |
| R2 | 2100-3460 | 1 | RESISTOR-VAR 500K 10% CC | 01121 | WA1N040S504AZ |
| R3 | 2100-2062 | 2 | RESISTOR-VAR 500 OHM 10% CC | 12697 | 63M |
| R4 | 2100-2635 | | RESISTOR-VAR 50K 20% CC | 01121 | TYPE W |
| R5 | 2100-2062 | | RESISTOR-VAR 500 OHM 10% CC | 12697 | 63M |
| R6 | 2100-2635 | | RESISTOR-VAR 50K 20% CC | 01121 | TYPE W |
| R7 | 2100-2492 | 2 | RESISTOR-VAR 5K 20% CC | 71450 | SERIES 300 |
| R8 | 2100-2492 | | RESISTOR-VAR 5K 20% CC | 71450 | SERIES 300 |
| S1 | 3101-7042 | 1 | SWITCH | 28480 | 3101-7042 |
| S2 | 3101-1609 | 1 | SWITCH-SL 2-DPDT-NS STD 3A 125VAC SLDR | 82389 | 11E-1036 |
| T1 | 9100-3468 | 1 | TRANSFORMER, POWER | 28480 | 9100-3468 |
| TP1 | 0360-1646 | 1 | TERMINAL-STUD SPCL PRESS MTG | 28480 | 0360-1646 |
| U1 | 1826-0147 | 1 | IC LIN REGULATOR | 07263 | 7812UC |
| U2 | 1826-0221 | 1 | IC LIN MC 7912CP REGULATOR | 04713 | MC7912CP |
| W1 | 01607-61602 | 1 | CABLE, DISPLAY TIME/LO | 28480 | 01607-61602 |
| W2 | 01607-61601 | 1 | CABLE, V SIZE AND POSITION | 28480 | 01607-61601 |
| W3 | 01607-61604 | 1 | CABLE, HORIZ/VERT OUT | 28480 | 01607-61604 |
| W4 | 01607-61609 | 1 | CABLE, LV POWER INPUT | 28480 | 01607-61609 |
| W5 | 01607-61610 | 1 | CABLE, INPUT/OUTPUT | 28480 | 01607-61610 |
| W6 | 01607-61611 | 1 | CABLE, POWER INPUT | 28480 | 01607-61611 |
| W7 | 8120-1521 | 1 | CABLE; UNSHLD 3-COND 18AWG | 28480 | 8120-1521 |
| W8 | 01607-61612 | 1 | CABLE, VOLT REG A | 28480 | 01607-61612 |
| W9 | 01607-61613 | 1 | CABLE, VOLT REG B | 28480 | 01607-61613 |
| W10 | 01607-61614 | 1 | CABLE, VOLT REG C | 28480 | 01607-61614 |

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

| Reference Designation | HP Part Number | Qty | Description | Mfr Code | Mfr Part Number |
|---|---|---|---|---|---|
| A1 | 01600-66511 | 1 | BOARD ASSY, DATA ACQUISITION | 28480 | 01600-66511 |
| A1C1 | 0140-0202 | 21 | CAPACITOR-FXD 15PF +-5% 500WVDC MICA | 72136 | DM15C150J0500WV1CR |
| A1C2 | 0140-0202 | | CAPACITOR-FXD 15PF +-5% 500WVDC MICA | 72136 | DM15C150J0500WV1CR |
| A1C3 | 0140-0202 | | CAPACITOR-FXD 15PF +-5% 500WVDC MICA | 72136 | DM15C150J0500WV1CR |
| A1C4 | 0140-0202 | | CAPACITOR-FXD 15PF +-5% 500WVDC MICA | 72136 | DM15C150J0500WV1CR |
| A1C5 | 0140-0202 | | CAPACITOR-FXD 15PF +-5% 500WVDC MICA | 72136 | DM15C150J0500WV1CR |
| A1C6 | 0140-0202 | | CAPACITOR-FXD 15PF +-5% 500WVDC MICA | 72136 | DM15C150J0500WV1CR |
| A1C7 | 0140-0202 | | CAPACITOR-FXD 15PF +-5% 500WVDC MICA | 72136 | DM15C150J0500WV1CR |
| A1C8 | 0140-0202 | | CAPACITOR-FXD 15PF +-5% 500WVDC MICA | 72136 | DM15C150J0500WV1CR |
| A1C9 | 0140-0202 | | CAPACITOR-FXD 15PF +-5% 500WVDC MICA | 72136 | DM15C150J0500WV1CR |
| A1C10 | 0140-0202 | | CAPACITOR-FXD 15PF +-5% 500WVDC MICA | 72136 | DM15C150J0500WV1CR |
| A1C11 | 0140-0202 | | CAPACITOR-FXD 15PF +-5% 500WVDC MICA | 72136 | DM15C150J0500WV1CR |
| A1C12 | 0140-0202 | | CAPACITOR-FXD 15PF +-5% 500WVDC MICA | 72136 | DM15C150J0500WV1CR |
| A1C13 | 0140-0202 | | CAPACITOR-FXD 15PF +-5% 500WVDC MICA | 72136 | DM15C150J0500WV1CR |
| A1C14 | 0140-0202 | | CAPACITOR-FXD 15PF +-5% 500WVDC MICA | 72136 | DM15C150J0500WV1CR |
| A1C15 | 0140-0202 | | CAPACITOR-FXD 15PF +-5% 500WVDC MICA | 72136 | DM15C150J0500WV1CR |
| A1C16 | 0140-0202 | | CAPACITOR-FXD 15PF +-5% 500WVDC MICA | 72136 | DM15C150J0500WV1CR |
| A1C17 | 0140-0202 | | CAPACITOR-FXD 15PF +-5% 500WVDC MICA | 72136 | DM15C150J0500WV1CR |
| A1C18 | 0140-0202 | | CAPACITOR-FXD 15PF +-5% 500WVDC MICA | 72136 | DM15C150J0500WV1CR |
| A1C19 | 0160-0174 | 5 | CAPACITOR-FXD .47UF +80-20% 25WVDC CER | 28480 | 0160-0174 |
| A1C20 | 0160-0174 | | CAPACITOR-FXD .47UF +80-20% 25WVDC CER | 28480 | 0160-0174 |
| A1C21 | 0160-0174 | | CAPACITOR-FXD .47UF +80-20% 25WVDC CER | 28480 | 0160-0174 |
| A1C22 | 0160-3448 | 1 | CAPACITOR-FXD 1000PF +-10% 1000WVDC CER | 28480 | 0160-3448 |
| A1C23 | 0160-3451 | 41 | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C24 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C25 | 0140-0190 | 2 | CAPACITOR-FXD 39PF +-5% 300WVDC MICA | 72136 | DM15E390J0300WV1CR |
| A1C26 | 0160-2207 | 1 | CAPACITOR-FXD 300PF +-5% 300WVDC MICA | 28480 | 0160-2207 |
| A1C27 | 0140-0196 | 1 | CAPACITOR-FXD 150PF +-5% 300WVDC MICA | 72136 | DM15F151J0300WV1CR |
| A1C28 | 0160-2204 | 3 | CAPACITOR-FXD 100PF +-5% 300WVDC MICA | 28480 | 0160-2204 |
| A1C29 | 0140-0202 | | CAPACITOR-FXD 15PF +-5% 500WVDC MICA | 72136 | DM15C150J0500WV1CR |
| A1C30 | 0140-0190 | | CAPACITOR-FXD 39PF +-5% 300WVDC MICA | 72136 | DM15E390J0300WV1CR |
| A1C31 | 0160-2201 | 1 | CAPACITOR-FXD 51PF +-5% 300WVDC MICA | 28480 | 0160-2201 |
| A1C32 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C33 | 0121-0046 | 3 | CAPACITOR; VAR; TRMR; CER; 9/35PF | 73899 | DV11PS350 |
| A1C34 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C35 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C36 | | | NOT ASSIGNED | | |
| A1C37 | 0121-0046 | | CAPACITOR; VAR; TRMR; CER; 9/35PF | 73899 | DV11PS350 |
| A1C38 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C39 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C40 | 0160-2198 | 4 | CAPACITOR-FXD 20PF +-5% 300WVDC MICA | 28480 | 0160-2198 |
| A1C41 | 0121-0046 | | CAPACITOR; VAR; TRMR; CER; 9/35PF | 73899 | DV11PS350 |
| A1C42 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C43 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C44 | 0180-0197 | 5 | CAPACITOR-FXD; 2.2UF+-10% 20VDC TA | 56289 | 150D225X9020A2 |
| A1C45 | 0180-0116 | 6 | CAPACITOR-FXD; 6.8UF+-10% 35VDC TA | 56289 | 150D685X9035B2 |
| A1C46 | 0180-0116 | | CAPACITOR-FXD; 6.8UF+-10% 35VDC TA | 56289 | 150D685X9035B2 |
| A1C47 | 0180-0197 | | CAPACITOR-FXD; 2.2UF+-10% 20VDC TA | 56289 | 150D225X9020A2 |
| A1C48 | 0180-0116 | | CAPACITOR-FXD; 6.8UF+-10% 35VDC TA | 56289 | 150D685X9035B2 |
| A1C49 | 0180-0116 | | CAPACITOR-FXD; 6.8UF+-10% 35VDC TA | 56289 | 150D685X9035B2 |
| A1C50 | 0180-0116 | | CAPACITOR-FXD; 6.8UF+-10% 35VDC TA | 56289 | 150D685X9035B2 |
| A1C51 | 0180-0116 | | CAPACITOR-FXD; 6.8UF+-10% 35VDC TA | 56289 | 150D685X9035B2 |
| A1C52 | 0160-2198 | | CAPACITOR-FXD 20PF +-5% 300WVDC MICA | 28480 | 0160-2198 |
| A1C53 | 0160-2198 | | CAPACITOR-FXD 20PF +-5% 300WVDC MICA | 28480 | 0160-2198 |
| A1C54 | 0160-0174 | | CAPACITOR-FXD .47UF +80-20% 25WVDC CER | 28480 | 0160-0174 |
| A1C55 | 0160-0174 | | CAPACITOR-FXD .47UF +80-20% 25WVDC CER | 28480 | 0160-0174 |
| A1C56 | 0180-0106 | 2 | CAPACITOR-FXD; 60UF+-20% 6VDC TA-SOLID | 56289 | 150D606X0006B2 |
| A1C57 | 0180-0106 | | CAPACITOR-FXD; 60UF+-20% 6VDC TA-SOLID | 56289 | 150D606X0006B2 |
| A1C58 | 0180-0228 | 7 | CAPACITOR-FXD; 22UF+-10% 15VDC TA-SOLID | 56289 | 150D226X9015B2 |
| A1C59 | 0180-0228 | | CAPACITOR-FXD; 22UF+-10% 15VDC TA-SOLID | 56289 | 150D226X9015B2 |
| A1C60 | 0160-2198 | | CAPACITOR-FXD 20PF +-5% 300WVDC MICA | 28480 | 0160-2198 |
| A1C61 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C62 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C63 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C64 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C65 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C66 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C67 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C68 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C69 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C70 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

| Reference Designation | HP Part Number | Qty | Description | Mfr Code | Mfr Part Number |
|---|---|---|---|---|---|
| A1C71 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C72 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C73 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C74 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C75 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C76 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C77 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1C78 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A1CR1 | 1901-0040 | 5 | DIODE-SWITCHING 2NS 30V 50MA | 28480 | 1901-0040 |
| A1CR2 | 1901-0535 | 2 | DIODE-SCHOTTKY | 28480 | 1901-0535 |
| A1CR3 | 1901-0535 | | DIODE-SCHOTTKY | 28480 | 1901-0535 |
| A1CR4 | 1901-0040 | | DIODE-SWITCHING 2NS 30V 50MA | 28480 | 1901-0040 |
| A1CR5 | 1901-0040 | | DIODE-SWITCHING 2NS 30V 50MA | 28480 | 1901-0040 |
| A1J1 | 1251-0699 | 4 | CONNECTOR | 28480 | 1251-0699 |
| A1J2 | 1251-0699 | | CONNECTOR | 28480 | 1251-0699 |
| A1J3 | 1251-0699 | | CONNECTOR | 28480 | 1251-0699 |
| A1J4 | 1251-0699 | | CONNECTOR | 28480 | 1251-0699 |
| A1J5 | 1200-0441 | 5 | SOCKET, ELEC, IC 14-CONT DIP SLDR TERM | 24995 | 583527-1 |
| A1J6 | 1200-0441 | | SOCKET, ELEC, IC 14-CONT DIP SLDR TERM | 24995 | 583527-1 |
| A1J7 | 1200-0441 | | SOCKET, ELEC, IC 14-CONT DIP SLDR TERM | 24995 | 583527-1 |
| A1J8 | 1200-0441 | | SOCKET, ELEC, IC 14-CONT DIP SLDR TERM | 24995 | 583527-1 |
| A1J9 | 1200-0441 | | SOCKET, ELEC, IC 14-CONT DIP SLDR TERM | 24995 | 583527-1 |
| A1L1 | 9100-2259 | 20 | COIL-FXD MOLDED RF CHOKE 1.5UH 10% | 24226 | 10/151 |
| A1L2 | 9100-2259 | | COIL-FXD MOLDED RF CHOKE 1.5UH 10% | 24226 | 10/151 |
| A1L3 | 9100-2259 | | COIL-FXD MOLDED RF CHOKE 1.5UH 10% | 24226 | 10/151 |
| A1L4 | 9100-2259 | | COIL-FXD MOLDED RF CHOKE 1.5UH 10% | 24226 | 10/151 |
| A1L5 | 9100-2259 | | COIL-FXD MOLDED RF CHOKE 1.5UH 10% | 24226 | 10/151 |
| A1L6 | 9100-2259 | | COIL-FXD MOLDED RF CHOKE 1.5UH 10% | 24226 | 10/151 |
| A1L7 | 9100-2259 | | COIL-FXD MOLDED RF CHOKE 1.5UH 10% | 24226 | 10/151 |
| A1L8 | 9100-2259 | | COIL-FXD MOLDED RF CHOKE 1.5UH 10% | 24226 | 10/151 |
| A1L9 | 9100-2259 | | COIL-FXD MOLDED RF CHOKE 1.5UH 10% | 24226 | 10/151 |
| A1L10 | 9100-2259 | | COIL-FXD MOLDED RF CHOKE 1.5UH 10% | 24226 | 10/151 |
| A1L11 | 9100-2259 | | COIL-FXD MOLDED RF CHOKE 1.5UH 10% | 24226 | 10/151 |
| A1L12 | 9100-2259 | | COIL-FXD MOLDED RF CHOKE 1.5UH 10% | 24226 | 10/151 |
| A1L13 | 9100-2259 | | COIL-FXD MOLDED RF CHOKE 1.5UH 10% | 24226 | 10/151 |
| A1L14 | 9100-2259 | | COIL-FXD MOLDED RF CHOKE 1.5UH 10% | 24226 | 10/151 |
| A1L15 | 9100-2259 | | COIL-FXD MOLDED RF CHOKE 1.5UH 10% | 24226 | 10/151 |
| A1L16 | 9100-2259 | | COIL-FXD MOLDED RF CHOKE 1.5UH 10% | 24226 | 10/151 |
| A1L17 | 9100-2259 | | COIL-FXD MOLDED RF CHOKE 1.5UH 10% | 24226 | 10/151 |
| A1L18 | 9100-2259 | | COIL-FXD MOLDED RF CHOKE 1.5UH 10% | 24226 | 10/151 |
| A1L19 | 9100-2259 | | COIL-FXD MOLDED RF CHOKE 1.5UH 10% | 24226 | 10/151 |
| A1L20 | 9100-2255 | 2 | COIL-FXD MOLDED RF CHOKE 470MH 10% | 24226 | 10/470 |
| A1L21 | 9100-2255 | | COIL-FXD MOLDED RF CHOKE 470MH 10% | 24226 | 10/470 |
| A1L22 | 9100-2259 | | COIL-FXD MOLDED RF CHOKE 1.5UH 10% | 24226 | 10/151 |
| A1MP1 | 5040-7478 | 4 | HOUSING, TOP | 28480 | 5040-7478 |
| A1MP2 | 5040-7479 | 4 | HOUSING, BOTTOM | 28480 | 5040-7479 |
| A1R1 | 0757-0420 | 18 | RESISTOR 750 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-751-F |
| A1R2 | 0757-0420 | | RESISTOR 750 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-751-F |
| A1R3 | 0757-0420 | | RESISTOR 750 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-751-F |
| A1R4 | 0757-0420 | | RESISTOR 750 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-751-F |
| A1R5 | 0757-0420 | | RESISTOR 750 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-751-F |
| A1R6 | 0757-0420 | | RESISTOR 750 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-751-F |
| A1R7 | 0757-0420 | | RESISTOR 750 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-751-F |
| A1R8 | 0757-0420 | | RESISTOR 750 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-751-F |
| A1R9 | 0757-0420 | | RESISTOR 750 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-751-F |
| A1R10 | 0757-0420 | | RESISTOR 750 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-751-F |
| A1R11 | 0757-0420 | | RESISTOR 750 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-751-F |
| A1R12 | 0757-0420 | | RESISTOR 750 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-751-F |
| A1R13 | 0757-0420 | | RESISTOR 750 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-751-F |
| A1R14 | 0757-0420 | | RESISTOR 750 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-751-F |
| A1R15 | 0757-0420 | | RESISTOR 750 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-751-F |
| A1R16 | 0757-0420 | | RESISTOR 750 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-751-F |
| A1R17 | 0757-0420 | | RESISTOR 750 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-751-F |
| A1R18 | 0757-0420 | | RESISTOR 750 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-751-F |
| A1R19 | 0684-6821 | 4 | RESISTOR 6.8K 10% .25W FC TC=-400/+700 | 01121 | CB6821 |
| A1R20 | 0698-0084 | 2 | RESISTOR 2.15K 1% .125W F TC=0+-100 | 16299 | C4-1/8-TO-2151-F |
| A1R21 | 0757-0438 | 2 | RESISTOR 5.11K 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-5111-F |
| A1R22 | 0757-0472 | 2 | RESISTOR 200K 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-2003-F |
| A1R23 | 0757-0465 | 2 | RESISTOR 100K 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-1003-F |
| A1R24 | 0757-0463 | 1 | RESISTOR 82.5K 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-8252-F |
| A1R25 | 0683-0275 | 1 | RESISTOR 2.7 5% .25W FC TC=-400/+500 | 01121 | CB2705 |
| A1R26 | 0684-6821 | | RESISTOR 6.8K 10% .25W FC TC=-400/+700 | 01121 | CB6821 |
| A1R27 | 0684-6821 | | RESISTOR 6.8K 10% .25W FC TC=-400/+700 | 01121 | CB6821 |
| A1R28 | 0757-0407 | 4 | RESISTOR 200 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-201-F |
| A1R29 | 0757-0401 | 3 | RESISTOR 100 1% .125W F TC=0+-100 | 24546 | C4-1/8-TO-101-F |
| A1R30 | 0684-3911 | + | RESISTOR 390 10% .25W FC TC=-400/+600 | 01121 | CB3911 |

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

| Reference Designation | HP Part Number | Qty | Description | Mfr Code | Mfr Part Number |
|---|---|---|---|---|---|
| A1R31 | 0684-3911 | | RESISTOR 390 10% .25W FC TC=-400/+600 | 01121 | CB3911 |
| A1R32 | 0684-3911 | | RESISTOR 390 10% .25W FC TC=-400/+600 | 01121 | CB3911 |
| A1R33 | 0757-0280 | 10 | RESISTOR 1K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1001-F |
| A1R34 | 0757-0280 | | RESISTOR 1K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1001-F |
| A1R35 | 0684-3911 | | RESISTOR 390 10% .25W FC TC=-400/+600 | 01121 | CB3911 |
| A1R36 | 0757-0288 | 3 | RESISTOR 9.09K 1% .125W F TC=0+-100 | 19701 | MF4C1/8-T0-9091-F |
| A1R37 | 0757-0288 | | RESISTOR 9.09K 1% .125W F TC=0+-100 | 19701 | MF4C1/8-T0-9091-F |
| A1R38 | 0757-0288 | | RESISTOR 9.09K 1% .125W F TC=0+-100 | 19701 | MF4C1/8-T0-9091-F |
| A1R39 | 0683-5105 | 1 | RESISTOR 51 5% .25W FC TC=-400/+500 | 01121 | CB5105 |
| A1R40 | 0757-0280 | | RESISTOR 1K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1001-F |
| A1R41 | 0698-3447 | 1 | RESISTOR 422 1% .125W F TC=0+-100 | 16299 | C4-1/8-T0-422R-F |
| A1R42 | 0757-0418 | 1 | RESISTOR 619 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-619R-F |
| A1R43 | 0757-0416 | 3 | RESISTOR 511 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-511R-F |
| A1R44 | 0698-3150 | 1 | RESISTOR 2.37K 1% .125W F TC=0+-100 | 16299 | C4-1/8-T0-2371-F |
| A1R45 | 0698-3122 | 1 | RESISTOR 412 1% .125W F TC=0+-100 | 03888 | PME55-1/8-T0-4120-F |
| A1R46 | 0757-0416 | | RESISTOR 511 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-511R-F |
| A1R47 | 0757-0442 | 3 | RESISTOR 10K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1002-F |
| A1R48 | 0757-0416 | | RESISTOR 511 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-511R-F |
| A1R49 | 2100-1738 | 1 | RESISTOR-VAR TRMR 500 OHM 10% C TOP ADJ | 84048 | 170-501 |
| A1R50 | 0698-3444 | 2 | RESISTOR 316 1% .125W F TC=0+-100 | 16299 | C4-1/8-T0-316R-F |
| A1R51 | 0757-0280 | | RESISTOR 1K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1001-F |
| A1R52 | 0757-0442 | | RESISTOR 10K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1002-F |
| A1R53 | 0757-0280 | | RESISTOR 1K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1001-F |
| A1R54 | 0698-4130 | 1 | RESISTOR 39 5% .125W CC TC=0+588 | 01121 | BB3905 |
| A1R55 | 0698-3444 | | RESISTOR 316 1% .125W F TC=0+-100 | 16299 | C4-1/8-T0-316R-F |
| A1R56 | 0757-0280 | | RESISTOR 1K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1001-F |
| A1R57 | 0757-0442 | | RESISTOR 10K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1002-F |
| A1R58 | 0757-0280 | | RESISTOR 1K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1001-F |
| A1R59 | 0698-3379 | 1 | RESISTOR 68 5% .125W CC TC=0+588 | 01121 | BB6805 |
| A1R60 | 0684-2201 | 2 | RESISTOR 22 10% .25W FC TC=-400/+500 | 01121 | CB2201 |
| A1R61 | 0684-4721 | 1 | RESISTOR 4.7K 10% .25W FC TC=-400/+700 | 01121 | CB4721 |
| A1R62 | 0757-0434 | 1 | RESISTOR 3.65K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-3651-F |
| A1R63 | 0757-0426 | 1 | RESISTOR 1.3K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1301-F |
| A1R64 | 0757-0280 | | RESISTOR 1K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1001-F |
| A1R65 | | 3 | NOT ASSIGNED | | |
| A1R66 | 0757-0457 | 7 | RESISTOR 47.5K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-4752-F |
| A1R67 | 0757-0457 | | RESISTOR 47.5K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-4752-F |
| A1R68 | 0757-0457 | | RESISTOR 47.5K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-4752-F |
| A1R69 | 0757-0457 | | RESISTOR 47.5K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-4752-F |
| A1R70 | 0757-0457 | | RESISTOR 47.5K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-4752-F |
| A1R71 | 0684-2201 | | RESISTOR 22 10% .25W FC TC=-400/+500 | 01121 | CB2201 |
| A1R72 | 0684-6821 | | RESISTOR 6.8K 10% .25W FC TC=-400/+700 | 01121 | CB6821 |
| A1R73 | 0757-0407 | | RESISTOR 200 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-201-F |
| A1R74 | 0757-0401 | | RESISTOR 100 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-101-F |
| A1R75 | 0698-0084 | | RESISTOR 2.15K 1% .125W F TC=0+-100 | 16299 | C4-1/8-T0-2151-F |
| A1R76 | 0698-3151 | 1 | RESISTOR 2.87K 1% .125W F TC=0+-100 | 16299 | C4-1/8-T0-2871-F |
| A1R77 | 0757-0457 | | RESISTOR 47.5K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-4752-F |
| A1S1 | 3101-1946 | 1 | SWITCH | 28480 | 3101-1946 |
| A1TP1 | 0360-0535 | 2 | TERMINAL, TEST POINT | 4G819 | OBD |
| A1TP2 | 0360-0535 | | TERMINAL, TEST POINT | 4G819 | OBD |
| A1TP3 | 1251-2229 | 2 | CONNECTOR; 1-CONT SKT .033 DIA | 00779 | 1-331677-3 |
| A1TP4 | 1251-2229 | | CONNECTOR; 1-CONT SKT .033 DIA | 00779 | 1-331677-3 |
| A1U1 | 1820-0693 | 9 | IC SN74S 74 N | 01295 | SN74S74N |
| A1U2 | 1820-0693 | | IC SN74S 74 N | 01295 | SN74S74N |
| A1U3 | 1820-0693 | | IC SN74S 74 N | 01295 | SN74S74N |
| A1U4 | 1820-0693 | | IC SN74S 74 N | 01295 | SN74S74N |
| A1U5 | 1820-0693 | | IC SN74S 74 N | 01295 | SN74S74N |
| A1U6 | 1820-0693 | | IC SN74S 74 N | 01295 | SN74S74N |
| A1U7 | 1820-0693 | | IC SN74S 74 N | 01295 | SN74S74N |
| A1U8 | 1820-0693 | | IC SN74S 74 N | 01295 | SN74S74N |
| A1U9 | 1820-0693 | | IC SN74S 74 N | 01295 | SN74S74N |
| A1U10 | 1820-0692 | 8 | IC SN74S 65 N | 01295 | SN74S65N |
| A1U11 | 1820-0692 | | IC SN74S 65 N | 01295 | SN74S65N |
| A1U12 | 1820-0692 | | IC SN74S 65 N | 01295 | SN74S65N |
| A1U13 | 1820-0692 | | IC SN74S65N | 01295 | SN74S65N |
| A1U14 | 1820-0692 | | IC SN74S 65 N | 01295 | SN74S65N |
| A1U15 | 1820-0692 | | IC SN74S 65 N | 01295 | SN74S65N |
| A1U16 | 1820-0692 | | IC SN74S 65 N | 01295 | SN74S65N |
| A1U17 | 1820-0692 | | IC SN74S 65 N | 01295 | SN74S65N |
| A1U18 | 1820-0692 | | IC SN74S 65 N | 01295 | SN74S65N |
| A1U19 | 1820-1146 | 7 | IC CD4050AE | 02735 | CD4050AE |
| A1U20 | 1820-1146 | | IC CD4050AE | 02735 | CD4050AE |
| A1U21 | 1820-1146 | | IC CD4050AE | 02735 | CD4050AE |
| A1U22 | 1820-1146 | | IC CD4050AE | 02735 | CD4050AE |
| A1U23 | 1820-1146 | | IC CD4050AE | 02735 | CD4050AE |
| A1U24 | 1820-1146 | | IC CD4050AE | 02735 | CD4050AE |
| A1U25 | 1820-0687 | 1 | IC SN74S 15 N | 01295 | SN74S15N |

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

| Reference Designation | HP Part Number | Qty | Description | Mfr Code | Mfr Part Number |
|---|---|---|---|---|---|
| A1U26 | 1820-0691 | 11 | IC SN74S 64 N | 01295 | SN74S64N |
| A1U27 | 1820-1201 | 1 | IC SN74LS 08 N | 01295 | SN74LS08N |
| A1U28 | 1820-1106 | 4 | IC MEMORY | 34649 | 3101A |
| A1U29 | 1820-1139 | 3 | IC:TTL, HEX INVERTER | 28480 | 1820-1139 |
| A1U30 | 1820-1106 | | IC MEMORY | 34649 | 3101A |
| A1U31 | 1820-1139 | | IC:TTL, HEX INVERTER | 28480 | 1820-1139 |
| A1U32 | 1820-1106 | | IC MEMORY | 34649 | 3101A |
| A1U33 | 1820-1139 | | IC:TTL, HEX INVERTER | 28480 | 1820-1139 |
| A1U34 | 1820-1106 | | IC MEMORY | 34649 | 3101A |
| A1U35 | | | NOT ASSIGNED | | |
| A1U36 | | | NOT ASSIGNED | | |
| A1U37 | | | NOT ASSIGNED | | |
| A1U38 | | | NOT ASSIGNED | | |
| A1U39 | 1820-0640 | 1 | IC SN74 150 N | 01295 | SN74150N |
| A1U40 | | | NOT ASSIGNED | | |
| A1U41 | 1820-0681 | 3 | IC SN74S 00 N | 01295 | SN74S00N |
| A1U42 | 1820-1158 | 1 | IC SN74S 51 N | 01295 | SN74S51N |
| A1U43 | 1820-0629 | 5 | IC SN74S 112 N | 01295 | SN74S112N |
| A1U44 | 1821-0002 | 2 | IC CA3045 | 02735 | CA3045 |
| A1U45 | 1821-0002 | | IC CA3045 | 02735 | CA3045 |
| A1U46 | 1820-0629 | | IC SN74S 112 N | 01295 | SN74S112N |
| A1U47 | 1820-0661 | 1 | IC SN74 32 N | 01295 | SN7432N |
| A1U48 | 1820-0203 | 1 | IC AMPLIFIER | 28480 | 1820-0203 |
| A1U49 | 1820-0584 | 1 | IC DM74L 02N | 27014 | DM74L02N |
| A1U50 | 1810-0183 | 19 | NETWORK-RES 9-PIN SIP .1-PIN-SPCG | 28480 | 1810-0183 |
| A1U51 | 1820-0515 | 5 | IC MULTIVIBRATOR | 07263 | 9602DC |
| A1U52 | 1820-0515 | | IC MULTIVIBRATOR | 07263 | 9602DC |
| A1U53 | 1820-0515 | | IC MULTIVIBRATOR | 07263 | 9602DC |
| A1U54 | 1820-0691 | | IC SN74S 64 N | 01295 | SN74S64N |
| A1U55 | 1820-0691 | | IC SN74S 64 N | 01295 | SN74S64N |
| A1U56 | 1820-0691 | | IC SN74S 64 N | 01295 | SN74S64N |
| A1U57 | 1820-0691 | | IC SN74S 64 N | 01295 | SN74S64N |
| A1U58 | 1820-0910 | 3 | IC SN74LS 83 N | 01295 | SN74LS83N |
| A1U59 | 1820-0910 | | IC SN74LS 83 N | 01295 | SN74LS83N |
| A1U60 | 1820-1475 | 2 | IC COUNTER | 07263 | 93S16DC |
| A1U61 | 1820-0515 | | IC MULTIVIBRATOR | 07263 | 9602DC |
| A1U62 | 1820-0697 | 2 | IC SN74S 140 N | 01295 | SN74S140N |
| A1U63 | 1820-0681 | | IC SN74S 00 N | 01295 | SN74S00N |
| A1U64 | 1820-0691 | | IC SN74S 64 N | 01295 | SN74S64N |
| A1U65 | 1820-0691 | | IC SN74S 64 N | 01295 | SN74S64N |
| A1U66 | 1820-0069 | 1 | IC SN74 20 N | 01295 | SN7420N |
| A1U67 | 1820-1372 | 3 | IC FLIP-FLOP | 07263 | 9S109DC |
| A1U68 | 1820-0515 | | IC MULTIVIBRATOR | 07263 | 9602DC |
| A1U69 | 1820-0685 | 1 | IC SN74S 10 N | 01295 | SN74S10N |
| A1U70 | 1820-1373 | 1 | IC COUNTER | 07263 | 93S10DC |
| A1U71 | 1820-1372 | | IC FLIP-FLOP | 07263 | 9S109DC |
| A1U72 | 1820-0063 | 1 | IC SN74 51 N | 01295 | SN7451N |
| A1U73 | 1820-0669 | 4 | IC COUNTER | 07263 | 93L10DC |
| A1U74 | 1820-0669 | | IC COUNTER | 07263 | 93L10DC |
| A1U75 | 1820-0669 | | IC COUNTER | 07263 | 93L10DC |
| A1U76 | 1820-0669 | | IC COUNTER | 07263 | 93L10DC |
| A1U77 | 1820-0691 | | IC SN74S 64 N | 01295 | SN74S64N |
| A1U78 | 1820-0070 | 1 | IC SN74 30 N | 01295 | SN7430N |
| A1U79 | 1820-0910 | | IC SN74LS 83 N | 01295 | SN74LS83N |
| A1U80 | 1820-0589 | 1 | IC DM74L 30N | 27014 | DM74L30N |
| A1U81 | 1820-0382 | 2 | IC SN74H 55 N | 01295 | SN74H55N |
| A1U82 | 1820-0538 | 1 | IC DM74L 20N | 27014 | DM74L20N |
| A1U83 | 1820-0710 | 2 | IC MULTIPLEXER | 07263 | 93L22DC |
| A1U84 | 1820-1372 | | IC FLIP-FLOP | 07263 | 9S109DC |
| A1U85 | 1820-0583 | 1 | IC DM74L 00N | 27014 | DM74L00N |
| A1U86 | 1820-0904 | 2 | IC COMPARATOR | 07263 | 93L24DC |
| A1U87 | 1820-0382 | | IC SN74H 55 N | 01295 | SN74H55N |
| A1U88 | 1820-0681 | | IC SN74S 00 N | 01295 | SN74S00N |
| A1U89 | 1820-0629 | | IC SN74S 112 N | 01295 | SN74S112N |
| A1U90 | 1820-0697 | | IC SN74S 140 N | 01295 | SN74S140N |
| A1U91 | 1820-0691 | | IC SN74S 64 N | 01295 | SN74S64N |
| A1U92 | 1820-0691 | | IC SN74S 64 N | 01295 | SN74S64N |
| A1U93 | 1820-0629 | | IC SN74S 112 N | 01295 | SN74S112N |
| A1U94 | 1820-0629 | | IC SN74S 112 N | 01295 | SN74S112N |
| A1U95 | 1820-1475 | | IC COUNTER | 07263 | 93S16DC |
| A1U96 | 1820-0686 | 1 | IC SN74S 11 N | 01295 | SN74S11N |
| A1U97 | 1820-0904 | | IC COMPARATOR | 07263 | 93L24DC |
| A1U98 | 1820-0683 | 1 | IC SN74S 04 N | 01295 | SN74S04N |
| A1U99 | 1810-0183 | | NETWORK-RES 9-PIN SIP .1-PIN-SPCG | 28480 | 1810-0183 |
| A1U100 | 1810-0183 | | NETWORK-RES 9-PIN SIP .1-PIN-SPCG | 28480 | 1810-0183 |

Table 6-2. Replaceable Parts (Cont'd)

| Reference Designation | HP Part Number | Qty | Description | Mfr Code | Mfr Part Number |
|---|---|---|---|---|---|
| A1U101 | 1810-0183 | | NETWORK-RES 9-PIN SIP .1-PIN-SPCG | 28480 | 1810-0183 |
| A1U102 | 1810-0183 | | NETWORK-RES 9-PIN SIP .1-PIN-SPCG | 28480 | 1810-0183 |
| A1U103 | 1810-0183 | | NETWORK-RES 9-PIN SIP .1-PIN-SPCG | 28480 | 1810-0183 |
| A1U104 | 1810-0183 | | NETWORK-RES 9-PIN SIP .1-PIN-SPCG | 28480 | 1810-0183 |
| A1U105 | 1810-0183 | | NETWORK-RES 9-PIN SIP .1-PIN-SPCG | 28480 | 1810-0183 |
| A1U106 | 1810-0183 | | NETWORK-RES 9-PIN SIP .1-PIN-SPCG | 28480 | 1810-0183 |
| A1U107 | 1810-0183 | | NETWORK-RES 9-PIN SIP .1-PIN-SPCG | 28480 | 1810-0183 |
| A1U108 | 1810-0183 | | NETWORK-RES 9-PIN SIP .1-PIN-SPCG | 28480 | 1810-0183 |
| A1U109 | 1810-0183 | | NETWORK-RES 9-PIN SIP .1-PIN-SPCG | 28480 | 1810-0183 |
| A1U110 | 1810-0183 | | NETWORK-RES 9-PIN SIP .1-PIN-SPCG | 28480 | 1810-0183 |
| A1XA5 | 1251-2035 | 4 | CONNECTOR; PC EDGE; 15-CONT; DIP SOLDER | 71785 | 252-15-30-300 |
| A1XA6 | 1251-2035 | | CONNECTOR; PC EDGE; 15-CONT; DIP SOLDER | 71785 | 252-15-30-300 |
| A2 | 01607-66504 | 1 | BOARD ASSY, DISPLAY | 28480 | 01607-66504 |
| A2C1 | 0180-0228 | | CAPACITOR-FXD; 22UF+-10% 15VDC TA-SOLID | 56289 | 150D226X9015B2 |
| A2C2 | 0180-0228 | | CAPACITOR-FXD; 22UF+-10% 15VDC TA-SOLID | 56289 | 150D226X9015B2 |
| A2C3 | 0180-0228 | | CAPACITOR-FXD; 22UF+-10% 15VDC TA-SOLID | 56289 | 150D226X9015B2 |
| A2C4 | 0160-0153 | 1 | CAPACITOR-FXD 1000PF +-10% 200WVDC POLYE | 56289 | 292P10292 |
| A2C5 | 0160-0161 | 1 | CAPACITOR-FXD .01UF +-10% 200WVDC POLYE | 56289 | 292P10392 |
| A2C6 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A2C7 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A2C8 | 0180-0228 | | CAPACITOR-FXD; 22UF+-10% 15VDC TA-SOLID | 56289 | 150D226X9015B2 |
| A2C9 | 0180-0228 | | CAPACITOR-FXD; 22UF+-10% 15VDC TA-SOLID | 56289 | 150D226X9015B2 |
| A2C10 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A2C11 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A2C12 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A2C13 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A2C14 | 0160-2204 | | CAPACITOR-FXD 100PF +-5% 300WVDC MICA | 28480 | 0160-2204 |
| A2C15 | 0160-2204 | | CAPACITOR-FXD 100PF +-5% 300WVDC MICA | 28480 | 0160-2204 |
| A2C16 | 0180-0197 | | CAPACITOR-FXD; 2.2UF+-10% 20VDC TA | 56289 | 150D225X9020A2 |
| A2C17 | 0160-3466 | 2 | CAPACITOR-FXD 100PF +-10% 1000WVDC CER | 28480 | 0160-3466 |
| A2C18 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A2C19 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A2C20 | 0160-2204 | | CAPACITOR-FXD 100PF +-5% 300WVDC MICA | 28480 | 0160-2204 |
| A2C21 | 0160-3466 | | CAPACITOR-FXD 100PF +-10% 1000WVDC CER | 28480 | 0160-3466 |
| A2C22 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A2C23 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A2C24 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A2C25 | 0180-0309 | | CAPACITOR-FXD 4.7UF +-20% 10VDC TA | 56289 | 150D475X00102A |
| A2C26 | 0180-0197 | | CAPACITOR-FXD; 2.2UF+-10% 20VDC TA | 56289 | 150D225X9020A2 |
| A2C27 | 0160-3448 | | CAPACITOR-FXD 1000PF +-10% 1000WVDC CER | 28480 | 0160-3448 |
| A2C28 | 0160-3448 | | CAPACITOR-FXD 1000PF +-10% 1000WVDC CER | 28480 | 0160-3448 |
| A2CR1 | 1901-0040 | | DIODE-SWITCHING 2NS 30V 50MA | 28480 | 1901-0040 |
| A2CR2 | 1901-0040 | | DIODE-SWITCHING 2NS 30V 50MA | 28480 | 1901-0040 |
| A2CR3 | 1910-0016 | | DIODE-SWITCHING 1US 60V 60MA | 28480 | 1901-0016 |
| A2L1 | 9100-2276 | 3 | COIL-FXD MOLDED RF CHOKE 100UH 10% | 24226 | 10/103 |
| A2L2 | 9100-2276 | | COIL-FXD MOLDED RF CHOKE 100UH 10% | 24226 | 10/103 |
| A2L3 | 9100-2276 | | COIL-FXD MOLDED RF CHOKE 100UH 10% | 24226 | 10/103 |
| A2L4 | 9100-1663 | 1 | COIL-FXD MOLDED RF CHOKE 2.7MH 5% | 06560 | 22-1312-29J |
| A2P1 | 1251-0674 | 2 | CONNECTOR; 10-CONT; MALE; POST TYPE | 27264 | 09-66-1101 |
| A2P2 | 1251-0674 | | CONNECTOR; 10-CONT; MALE; POST TYPE | 27264 | 09-66-1101 |
| A2P3 | 1251-3195 | 2 | CONNECTOR 4-PIN M POST TYPE | 27264 | 09-60-1041(2403-04A) |
| A2P4 | 1251-3197 | 1 | CONNECTOR 12-PIN M POST TYPE | 27264 | 09-60-1121(2403-12A) |
| A2Q1 | 1853-0036 | 3 | TRANSISTOR PNP SI PD=310MW FT=250MHZ | 28480 | 1853-0036 |
| A2Q2 | 1853-0036 | | TRANSISTOR PNP SI PD=310MW FT=250MHZ | 28480 | 1853-0036 |
| A2Q3 | 1854-0071 | 2 | TRANSISTOR NPN SI PD=300MW FT=200MHZ | 28480 | 1854-0071 |
| A2Q4 | 1854-0071 | | TRANSISTOR NPN SI PD=300MW FT=200MHZ | 28480 | 1854-0071 |
| A2Q5 | 1853-0036 | | TRANSISTOR PNP SI PD=310MW FT=250MHZ | 28480 | 1853-0036 |
| A2Q6 | 1854-0071 | | TRANSISTOR NPN SI PD = 300MW FT = 200MHZ | 28480 | 1850-0071 |
| A2R1 | 0684-1031 | 7 | RESISTOR 10K 10% .25W FC TC=-400/+700 | 01121 | CB1031 |
| A2R2 | 0757-0407 | | RESISTOR 200 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-201-F |
| A2R3 | 0757-0407 | | RESISTOR 200 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-201-F |
| A2R4 | 0684-5621 | 9 | RESISTOR 5.6K 10% .25W FC TC=-400/+700 | 01121 | CB5621 |
| A2R5 | 2100-1738 | 1 | RESISTOR-VAR TRMR 10KOHM 10% C TOP ADJ | 19701 | ET50W103 |
| A2R6 | 0757-0200 | 4 | RESISTOR 5.62K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-5621-F |
| A2R7 | 0698-3152 | 1 | RESISTOR 3.48K 1% .125W F TC=0+-100 | 16299 | C4-1/8-T0-3481-F |
| A2R8 | 0684-1031 | | RESISTOR 10K 10% .25W FC TC=-400/+700 | 01121 | CB1031 |
| A2R9 | 0684-5621 | | RESISTOR 5.6K 10% .25W FC TC=-400/+700 | 01121 | CB5621 |
| A2R10 | 0757-0443 | 2 | RESISTOR 11K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1102-F |
| A2R11 | 0757-0421 | 1 | RESISTOR 825 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-8252-F |
| A2R12 | 0757-0443 | | RESISTOR 11K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1102-F |
| A2R13 | 0684-3311 | 1 | RESISTOR 330 10% .25W FC TC=-400/+600 | 01121 | CB3311 |
| A2R14 | 0684-4731 | 1 | RESISTOR 47K 10% .25W FC TC=-400/+800 | 01121 | CB4731 |
| A2R15 | 0684-2211 | 8 | RESISTOR 220 10% .25W FC TC=-400/+600 | 01121 | CB2211 |
| A2R16 | 0684-2211 | | RESISTOR 220 10% .25W FC TC=-400/+600 | 01121 | CB2211 |
| A2R17 | 0684-2211 | | RESISTOR 220 10% .25W FC TC=-400/+600 | 01121 | CB2211 |
| A2R18 | 0684-2211 | | RESISTOR 220 10% .25W FC TC=-400/+600 | 01121 | CB2211 |
| A2R19 | 0684-2211 | | RESISTOR 220 10% .25W FC TC=-400/+600 | 01121 | CB2211 |
| A2R20 | 0684-2701 | 1 | RESISTOR 27 10% .25W FC TC=-400/+500 | 01121 | CB2701 |

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

| Reference Designation | HP Part Number | Qty | Description | Mfr Code | Mfr Part Number |
|---|---|---|---|---|---|
| A2R21 | 0684-5621 | | RESISTOR 5.6K 10% .25W FC TC=-400/+700 | 01121 | CB5621 |
| A2R22 | 0757-0317 | 2 | RESISTOR 1.33K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1331-F |
| A2R23 | 0757-0462 | 1 | RESISTOR 75K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-7502-F |
| A2R24 | 0684-1031 | | RESISTOR 10K 10% .25W FC TC=-400/+700 | 01121 | CB1031 |
| A2R25 | 0684-5621 | | RESISTOR 5.6K 10% .25W FC TC=-400/+700 | 01121 | CB5621 |
| A2R26 | 0698-7096 | 2 | RESISTOR 10 10% .125W CC TC=0+588 (NOT INSTALLED ON BOARD AT FACTORY) | 01121 | BB1001 |
| A2R27 | 0684-1001 | 3 | RESISTOR 10 10% .25W FC TC=-400/+500 | 01121 | CB1001 |
| A2R28 | 0684-1831 | 2 | RESISTOR 18K 10% .25W FC TC=-400/+800 | 01121 | CB1831 |
| A2R29 | 0684-1831 | | RESISTOR 18K 10% .25W FC TC=-400/+800 | 01121 | CB1831 |
| A2R30 | 0698-7096 | | RESISTOR 10 10% .125W CC TC=0+588 (NOT INSTALLED ON BOARD AT FACTORY) | 01121 | BB1001 |
| A2R31 | 0757-0280 | | RESISTOR 1K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1001-F |
| A2R32 | 0757-0273 | 4 | RESISTOR 3.01K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-3011-F |
| A2R33 | 0757-0273 | | RESISTOR 3.01K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-3011-F |
| A2R34 | 0757-0290 | 2 | RESISTOR 6.19K 1% .125W F TC=0+-100 | 19701 | MF4C1/8-T0-6191-F |
| A2R35 | 0757-0290 | | RESISTOR 6.19K 1% .125W F TC=0+-100 | 19701 | MF4C1/8-T0-6191-F |
| A2R36 | 0757-0273 | | RESISTOR 3.01K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-3011-F |
| A2R37 | 0757-0415 | 2 | RESISTOR 475 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-475R-F |
| A2R38 | 0684-5621 | | RESISTOR 5.6K 10% .25W FC TC=-400/+700 | 01121 | CB5621 |
| A2R39 | 0684-5621 | | RESISTOR 5.6K 10% .25W FC TC=-400/+700 | 01121 | CB5621 |
| A2R40 | 0757-0200 | | RESISTOR 5.62K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-5621-F |
| A2R41 | 0684-2211 | | RESISTOR 220 10% .25W FC TC=-400/+600 | 01121 | CB2211 |
| A2R42 | 0757-0273 | | RESISTOR 3.01K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-3011-F |
| A2R43 | 0757-0415 | | RESISTOR 475 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-475R-F |
| A2R44 | 0684-5621 | | RESISTOR 5.6K 10% .25W FC TC=-400/+700 | 01121 | CB5621 |
| A2R45 | 0684-5621 | | RESISTOR 5.6K 10% .25W FC TC=-400/+700 | 01121 | CB5621 |
| A2R46 | 0757-0200 | | RESISTOR 5.62K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-5621-F |
| A2R47 | 0684-2211 | | RESISTOR 220 10% .25W FC TC=-400/+600 | 01121 | CB2211 |
| A2R48 | 0684-1021 | 4 | RESISTOR 1K 10% .25W FC TC=-400/+600 | 01121 | CB1021 |
| A2R49 | 0684-1021 | | RESISTOR 1K 10% .25W FC TC=-400/+600 | 01121 | CB1021 |
| A2R50 | 0684-1021 | | RESISTOR 1K 10% .25W FC TC=-400/+600 | 01121 | CB1021 |
| A2R51 | 0684-1021 | | RESISTOR 1K 10% .25W FC TC=-400/+600 | 01121 | CB1021 |
| A2R52 | 0757-0450 | 1 | RESISTOR 22.1K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-2212-F |
| A2R53 | 0757-0457 | | RESISTOR 47.5K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-4752-F |
| A2R54 | 0757-0465 | | RESISTOR 100K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1003-F |
| A2R55 | 0757-0472 | | RESISTOR 200K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-2003-F |
| A2R56 | 0757-0452 | 1 | RESISTOR 27.4K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-2742-F |
| A2R57 | 0684-1031 | | RESISTOR 10K 10% .25W FC TC=-400/+700 | 01121 | CB1031 |
| A2R58 | 0757-0401 | | RESISTOR 100 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-101-F |
| A2R59 | 0757-0317 | | RESISTOR 1.33K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1331-F |
| A2R60 | 0757-0200 | | RESISTOR 5.62K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-5621-F |
| A2R61 | 0757-0454 | 1 | RESISTOR 33.2K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-3322-F |
| A2R62 | 0684-4731 | | RESISTOR 47K 10% .25W CC TUBULAR | 01121 | CB4731 |
| A2S1 | 3101-1947 | 1 | SWITCH | 28480 | 3101-1947 |
| A2S2 | 3101-1942 | 1 | SWITCH | 28480 | 3101-1942 |
| A2U1 | 1820-0946 | 2 | IC CD4001AE | 02735 | CD4001AE |
| A2U2 | 1820-1330 | 1 | IC MC14507CP | 04713 | MC14507CP |
| A2U3 | 1820-0730 | 2 | IC MULTIVIBRATOR | 34335 | 96L02DC |
| A2U4 | 1820-1197 | 1 | IC SN74LS 00 N | 01295 | SN74LS00N |
| A2U5 | 1820-0730 | | IC MULTIVIBRATOR | 34335 | 96L02DC |
| A2U6 | 1820-0949 | 2 | IC CD4011AE | 02735 | CD4011AE |
| A2U7 | 1820-1356 | 1 | IC MC14528CP | 04713 | MC14528CP |
| A2U8 | 1820-0944 | 1 | IC CD4025AE | 02735 | CD4025AE |
| A2U9 | 1820-0691 | | IC SN74S 64 N | 01295 | SN74S64N |
| A2U10 | 1820-0071 | 1 | IC SN74 40 N | 01295 | SN7440N |
| A2U11 | 1826-0119 | 1 | IC NE 555T | 18324 | NE555T |
| A2U12 | 1820-0939 | 2 | IC CD4013AE | 02735 | CD4013AE |
| A2U13 | 1820-1150 | 1 | IC MC14520CP | 04713 | MC14520CP |
| A2U14 | 1820-0949 | | IC CD4011AE | 02735 | CD4011AE |
| A2U15 | 1820-0577 | 1 | IC SN74 16 N | 01295 | SN7416N |
| A2U16 | 1820-0321 | 2 | IC COMPARATOR (ANALOG) | 07263 | 710HC |
| A2U17 | 1820-0321 | | IC COMPARATOR (ANALOG) | 07263 | 710HC |
| A2U18 | 1820-0939 | | IC CD4013AE | 02735 | CD4013AE |
| A2U19 | 1820-1145 | 1 | IC CD4049AE | 02735 | CD4049AE |
| A2U20 | 1820-1194 | 2 | IC SN74LS193N | 01295 | SN74LS193N |
| A2U21 | 1820-0710 | | IC MULTIPLEXER | 07263 | 93L22DC |
| A2U22 | 1820-0946 | | IC CD4001AE | 02735 | CD4001AE |
| A2U23 | 1820-1146 | | IC CD4050AE | 02735 | CD4050AE |
| A2U24 | 1820-1339 | 1 | IC MC14002CP | 04713 | MC14002CP |
| A2U25 | 1820-1194 | | IC SN74LS193N | 01295 | SN74LS193N |
| A2U26 | 1816-0352 | 1 | IC MEMORY | 28480 | 1816-0352 |
| A2U27 | 1826-0138 | 2 | IC MC 1408L-8 | 04713 | MC1408L-8 |
| A2U28 | 1820-0978 | 1 | IC CD4007AE | 02735 | CD4007AE |
| A2U29 | 1826-0138 | | IC MC 1408L-8 | 04713 | MC1408L-8 |
| A2U30 | 1826-0254 | 2 | IC MC 1741SCP1 | 04713 | MC1741SCP1 |

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

| Reference Designation | HP Part Number | Qty | Description | Mfr Code | Mfr Part Number |
|---|---|---|---|---|---|
| A2U31 | 1826-0254 | | IC MC 1741SCP1 | 04713 | MC1741SCP1 |
| A2U32 | 1820-0054 | 1 | IC DIGITAL SN 74 00 N GATE | 01295 | SN7400N |
| A2U33 | 1810-0183 | | NETWORK-RES 9-PIN SIP .1-PIN-SPCG | 28480 | 1810-0183 |
| A2U34 | 1810-0183 | | NETWORK-RES 9-PIN SIP .1-PIN-SPCG | 28480 | 1810-0183 |
| A2U35 | 1810-0183 | | NETWORK-RES 9-PIN SIP .1-PIN-SPCG | 28480 | 1810-0183 |
| A2U36 | 1810-0183 | | NETWORK-RES 9-PIN SIP .1-PIN-SPCG | 28480 | 1810-0183 |
| A2U37 | 1810-0183 | | NETWORK-RES 9-PIN SIP .1-PIN-SPCG | 28480 | 1810-0183 |
| A2U38 | 1810-0183 | | NETWORK-RES 9-PIN SIP .1-PIN-SPCG | 28480 | 1810-0183 |
| A2VR1 | 1902-0049 | 1 | DIODE-ZNR 6.19V 5% DO-7 PD=.4W TC=+.022% | 04713 | SZ 10939-122 |
| A2XA5 | 1251-2035 | | CONNECTOR; PC EDGE; 15-CONT; DIP SOLDER | 71785 | 252-15-30-300 |
| A2XA6 | 1251-2035 | | CONNECTOR; PC EDGE; 15-CONT; DIP SOLDER | 71785 | 252-15-30-300 |
| A3 | 01607-66502 | 1 | BOARD ASSY, POWER SUPPLY | 28480 | 01607-66502 |
| A3C1 | 0180-0484 | 3 | CAPACITOR-FXD; 4500UF+75-10% 25VDC AL (NOT SUPPLIED WITH A3, ORDER SEPARATELY) | 56289 | 36D452G025AA-2B-DQB |
| A3C2 | 0180-0484 | 5 | CAPACITOR-FXD; 4500UF+75-10% 25VDC AL (NOT SUPPLIED WITH A3, ORDER SEPARATELY) | 56289 | 36D452G025AA-2B-DQB |
| A3C3 | 0180-0291 | | CAPACITOR-FXD; 1UF+-10% 35VDC TA-SOLID | 56289 | 150D105X9035A2 |
| A3C4 | 0180-0291 | | CAPACITOR-FXD; 1UF+-10% 35VDC TA-SOLID | 56289 | 150D105X9035A2 |
| A3C5 | 0180-0291 | | CAPACITOR-FXD; 1UF+-10% 35VDC TA-SOLID | 56289 | 150D105X9035A2 |
| A3C6 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A3C7 | 0160-3451 | | CAPACITOR-FXD .01UF +80-20% 100WVDC CER | 28480 | 0160-3451 |
| A3C8 | 0180-0291 | | CAPACITOR-FXD; 1UF+-10% 35VDC TA-SOLID | 56289 | 150D105X9035A2 |
| A3C9 | 0160-2204 | | CAPACITOR-FXD 100PF +-5% 300WVDC MICA | 28480 | 0160-2204 |
| A3C10 | 0180-0291 | | CAPACITOR-FXD; 1UF+-10% 35VDC TA-SOLID | 56289 | 150D105X9035A2 |
| A3C11 | 0180-0137 | 2 | CAPACITOR-FXD; 100UF+-20% 10VDC TA | 56289 | 150D107X0010B2 |
| A3C12 | 0180-0484 | | CAPACITOR-FXD; 4500UF+75-10% 25VDC AL (NOT SUPPLIED WITH A3, ORDER SEPARATELY) | 56289 | 36D452G025AA-2B-DQB |
| A3C13 | 0180-0137 | | CAPACITOR-FXD; 100UF+-20% 10VDC TA | 56289 | 150D107X0010B2 |
| A3C14 | 0180-0091 | 1 | CAPACITOR-FXD; 10UF+50-10% 100VDC AL | 56289 | 30D106F100DC2 |
| A3CR1 | | | | | |
| A3CR2 | 1884-0082 | 1 | THYRISTOR-SCR JEDEC 2N4441 | 04713 | 2N4441 |
| A3CR3 | 1901-0662 | 4 | DIODE-PWR RECT 100V 6A | 28480 | 1901-0662 |
| A3CR4 | 1901-0662 | | DIODE-PWR RECT 100V 6A | 28480 | 1901-0662 |
| A3CR5 | 1901-0662 | | DIODE-PWR RECT 100V 6A | 28480 | 1901-0662 |
| A3CR6 | 1901-0662 | | DIODE-PWR RECT 100V 6A | 28480 | 1901-0662 |
| A3CR7 | 1901-0049 | 1 | DIODE-PWR RECT 50V 750MA | 28480 | 1901-0049 |
| A3F1 | 2110-0033 | 2 | FUSE .75A 250V NORM-BLO 1.25X.25 | 75915 | F02A250V3/4A |
| A3F2 | 2110-0001 | | FUSE; 1A 250V | 71400 | AGC-1 |
| A3F3 | 2110-0006 | 1 | FUSE 2A 125V SLO-BLO 1.25X.25 | 75915 | 313002. |
| A3F4 | 2110-0004 | 1 | FUSE .25A 250V 1.25X.25 IEC | 71400 | AGC-1/4 |
| A3L1 | 9100-3465 | 1 | COIL-FXD RF CHOKE 1 MH | 28480 | 9100-3465 |
| A3L2 | 9100-3829 | 1 | COIL-FXD RF CHOKE 10UH | 28480 | 9100-3829 |
| A3MP1 | 2110-0269 | 1 | FUSEHOLDER-CLIP TYPE .25FUSE | 28480 | 2110-0269 |
| A3P1 | 1251-3195 | | CONNECTOR 4-PIN M POST TYPE | 27264 | 09-60-1041(2403-04A) |
| A3Q1 | 1853-0062 | 1 | TRANSISTOR PNP SI PD=300MW FT=200MHZ | 28480 | 1853-0062 |
| A3R1 | 0684-1031 | | RESISTOR 10K 10% .25W FC TC=-400/+700 | 01121 | CB1031 |
| A3R2 | 0684-1031 | | RESISTOR 10K 10% .25W FC TC=-400/+700 | 01121 | CB1031 |
| A3R3 | 0684-6811 | 1 | RESISTOR 680 10% .25W FC TC=-400/+600 | 01121 | CB6811 |
| A3R4 | 0684-3311 | | RESISTOR 330 10% .25W FC | 01121 | CB3311 |
| A3R5 | 0684-2201 | 1 | RESISTOR 22 10% .25W FC | 01121 | CB2201 |
| A3R6 | 0757-0488 | 1 | RESISTOR 909K 1% .125W F TC=0+-100 | 24546 | NA4 |
| A3R7 | 0757-0280 | | RESISTOR 1K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1001-F |
| A3R8 | 2100-3352 | 1 | RESISTOR-VAR TRMR 1KOHM 10% C SIDE ADJ | 73138 | 72XR1K |
| A3R9 | 0757-0274 | 1 | RESISTOR 1.21K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1213-F |
| A3R10 | 0757-0438 | | RESISTOR 5.11K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-5111-F |
| A3R11 | 0684-5621 | | RESISTOR 5.6K 10% .25W FC TC=-400/+700 | 01121 | CB5621 |
| A3R12 | 0684-5601 | 2 | RESISTOR 56 10% .25W FC TC=-400/+500 | 01121 | CB5601 |
| A3R13 | 0811-1758 | 2 | RESISTOR .24 5% 2W PW TC=0+-800 | 75042 | BWH2-24/100-J |
| A3R14 | 0811-1758 | | RESISTOR .24 5% 2W PW TC=0+-800 | 75042 | BWH2-24/100-J |
| A3R15 | 0684-5601 | | RESISTOR 56 10% .25W FC TC=-400/+500 | 01121 | CB5601 |
| A3R16 | 0684-1001 | | RESISTOR 10 10% .25W FC TC=-400/+500 | 01121 | CB1001 |
| A3R17 | 0684-1031 | | RESISTOR 10K 10% .25W FC TC=-400/+700 | 01121 | CB1031 |
| A3R18 | 0684-1001 | | RESISTOR 10 10% .25W FC TC=-400/+500 | 01121 | CB1001 |
| A3U1 | 1906-0023 | 1 | DIODE-MULT FULL WAVE BRIDGE RECTIFIER | 04713 | MDA922-4 |
| A3U2 | 1820-0082 | 1 | IC COUNTER | 28480 | 1820-0082 |
| A3VR1 | 1902-3104 | 1 | DIODE-ZNR 5.62V 5% DO-7 PD=.4W TC=+.016% | 04713 | SZ 10939-110 |
| A3XU2 | 1200-0493 | 1 | SOCKET,I.C. FOR 10-PIN TO-5 CASE | 4H713 | 133-99-92-054 |
| A4 | 01600-66506 | 1 | BOARD ASSY, TRIGGER SWITCH | 28480 | 01600-66506 |

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

| Reference Designation | HP Part Number | Qty | Description | Mfr Code | Mfr Part Number |
|---|---|---|---|---|---|
| A4S0 | 3101-0576 | 18 | SWITCH-TGL SUBMIN SPDT NS 2A 250VAC | 28480 | 3101-0576 |
| A4S1 | 3101-0576 | | SWITCH-TGL SUBMIN SPDT NS 2A 250VAC | 28480 | 3101-0576 |
| A4S2 | 3101-0576 | | SWITCH-TGL SUBMIN SPDT NS 2A 250VAC | 28480 | 3101-0576 |
| A4S3 | 3101-0576 | | SWITCH-TGL SUBMIN SPDT NS 2A 250VAC | 28480 | 3101-0576 |
| A4S4 | 3101-0576 | | SWITCH-TGL SUBMIN SPDT NS 2A 250VAC | 28480 | 3101-0576 |
| A4S5 | 3101-0576 | | SWITCH-TGL SUBMIN SPDT NS 2A 250VAC | 28480 | 3101-0576 |
| A4S6 | 3101-0576 | | SWITCH-TGL SUBMIN SPDT NS 2A 250VAC | 28480 | 3101-0576 |
| A4S7 | 3101-0576 | | SWITCH-TGL SUBMIN SPDT NS 2A 250VAC | 28480 | 3101-0576 |
| A4S8 | 3101-0576 | | SWITCH-TGL SUBMIN SPDT NS 2A 250VAC | 28480 | 3101-0576 |
| A4S9 | 3101-0576 | | SWITCH-TGL SUBMIN SPDT NS 2A 250VAC | 28480 | 3101-0576 |
| A4S10 | 3101-0576 | | SWITCH-TGL SUBMIN SPDT NS 2A 250VAC | 28480 | 3101-0576 |
| A4S11 | 3101-0576 | | SWITCH-TGL SUBMIN SPDT NS 2A 250VAC | 28480 | 3101-0576 |
| A4S12 | 3101-0576 | | SWITCH-TGL SUBMIN SPDT NS 2A 250VAC | 28480 | 3101-0576 |
| A4S13 | 3101-0576 | | SWITCH-TGL SUBMIN SPDT NS 2A 250VAC | 28480 | 3101-0576 |
| A4S14 | 3101-0576 | | SWITCH-TGL SUBMIN SPDT NS 2A 250VAC | 28480 | 3101-0576 |
| A4S15 | 3101-0576 | | SWITCH-TGL SUBMIN SPDT NS 2A 250VAC | 28480 | 3101-0576 |
| A4S16 | 3101-0576 | | SWITCH-TGL SUBMIN SPDT NS 2A 250VAC | 28480 | 3101-0576 |
| A4S17 | 3101-0576 | | SWITCH-TGL SUBMIN SPDT NS 2A 250VAC | 28480 | 3101-0576 |
| A4W1 | 8120-0621 | 5 | CABLE CA ASSY 14-COND 26AWG | 28480 | 8120-0621 |
| A4W2 | 8120-0621 | | CABLE CA ASSY 14-COND 26AWG | 28480 | 8120-0621 |
| A4W3 | 8120-0621 | | CABLE CA ASSY 14-COND 26AWG | 28480 | 8120-0621 |
| A7 | 01600-66510 | 1 | BOARD ASSY, DIGITAL SWITCH | 28480 | 01600-66510 |
| A7S1 | 3100-3238 | 1 | SWITCH, ROTARY | 28480 | 3100-3238 |
| A7W1 | 8120-0621 | | CABLE CA ASSY 14-COND 26AWG | 28480 | 8120-0621 |
| A7W2 | 8120-0621 | | CABLE CA ASSY 14-COND 26AWG | 28480 | 8120-0621 |

See introduction to this section for ordering information

Table 6-3. List of Manufacturers' Codes

| MFR NO. | MANUFACTURER NAME | ADDRESS | ZIP CODE |
|---|---|---|---|
| 01121 | ALLEN BRADLEY CO | MILWAUKEE WI | 53212 |
| 01295 | TEXAS INSTR INC SEMICOND CMPNT DIV | DALLAS TX | 75231 |
| 02735 | RCA CORP SOLID STATE DIV | SOMERVILLE NJ | 08876 |
| 03888 | PYROFILM CORP | WHIPPANY NJ | 07981 |
| 04713 | MOTOROLA SEMICONDUCTOR PRODUCTS | PHOENIX AZ | 85008 |
| 06666 | AIRCO SPEER ELEC DIV AIR RDCN CO | NOGALES AZ | 85621 |
| 07263 | FAIRCHILD SEMICONDUCTOR DIV | MOUNTAIN VIEW CA | 94040 |
| 12697 | CLAROSTAT MFG CO INC | DOVER NH | 03820 |
| 12954 | DICKSON ELECTRONICS CORP | SCOTTSDALE AZ | 85252 |
| 13103 | THERMALLOY CO | DALLAS TX | 75247 |
| 16299 | CORNING GLASS WKS ELEC CMPNT DIV | RALEIGH NC | 27604 |
| 18324 | SIGNETICS CORP | SUNNYVALE CA | 94086 |
| 19701 | MEPCO/ELECTRA CORP | MINERAL WELLS TX | 76067 |
| 24226 | GOWANDA ELECTRONICS CORP | GOWANDA NY | 14070 |
| 24546 | CORNING GLASS WORKS (BRADFORD) | BRADFORD PA | 16701 |
| 24931 | SPECIALTY CONNECTOR CO INC | INDIANAPOLIS IN | 46227 |
| 24995 | ENVIRONMENTAL CONTAINER SYSTEMS INC | PALO ALTO CA | 94304 |
| 27014 | NATIONAL SEMICONDUCTOR CORP | SANTA CLARA CA | 95051 |
| 27264 | MOLEX PRODUCTS CO | DOWNERS GROVE IL | 60515 |
| 28480 | HEWLETT-PACKARD CO CORPORATE HQ | PALO ALTO CA | 94304 |
| 34335 | ADVANCED MICRO DEVICES INC | SUNNYVALE CA | 94086 |
| 34649 | INTEL CORP | MOUNTAIN VIEW CA | 94040 |
| 46619 | OVERLAND PRODUCTS CO | FREMONT NE | 68025 |
| 47613 | CINCH MFG CO | SHELBYVILLE IN | 46176 |
| 56289 | SPRAGUE ELECTRIC CO | NORTH ADAMS MA | 01247 |
| 71400 | BUSSMAN MFG DIV OF MCGRAW-EDISON CO | ST LOUIS MO | 63017 |
| 71450 | CTS CORP | ELKHART IN | 46514 |
| 71744 | CHICAGO MINIATURE LAMP WORKS | CHICAGO IL | 60640 |
| 71785 | TRW ELEK COMPONENTS CINCH DIV | ELK GROVE VILLAGE IL | 60007 |
| 72136 | ELECTRO MOTIVE MFG CO INC | WILLIMANTIC CT | 06226 |
| 73138 | BECKMAN INSTRUMENTS INC HELIPOT DIV | FULLERTON CA | 92634 |
| 73899 | J F D ELECTRONICS CORP | BROOKLYN NY | 11219 |
| 75042 | TRW INC PHILADELPHIA DIV | PHILADELPHIA PA | 19108 |
| 75915 | LITTELFUSE INC | DES PLAINES IL | 60016 |
| 82389 | SWITCHCRAFT INC | CHICAGO IL | 60630 |
| 84048 | TRW INC ST PETERSBURG DIV | ST PETERSBURG FL | 33702 |

# SECTION VII

# MANUAL CHANGES AND OPTIONS

## 7-1. INTRODUCTION.

7-2. This section contains information required to backdate or update this manual for a specific instrument. Description of special options and standard options are also in this section.

## 7-3. MANUAL CHANGES.

7-4. This manual applies directly to the instrument having the same serial prefix shown on the manual title page. If the serial prefix of the instrument is not the same as the one on the title page, find your serial prefix in table 7-1 and make the changes to the manual that are listed for that serial prefix. When making changes listed in table 7-1, make the change with the highest number first. Example: if backdating changes 1, 2, and 3 are required for your serial prefix, do change 3 first, then change 2, and finally change 1. If the serial prefix of the instrument is not listed either in the title page or in table 7-1, refer to an enclosed MANUAL CHANGES sheet for updating information. Also, if a MANUAL CHANGES sheet is supplied, make all indicated ERRATA corrections.

*Table 7-1. Manual Changes*

| Serial Prefix | Make Changes |
|---|---|
| 1510A | 1 |

## 7-5. SPECIAL OPTIONS.

7-6. Most customer special application requirements and/or specifications can be met by factory modification of a standard instrument. A standard instrument modified in this way will carry a special option number, such as Model 0000A/Option C01.

7-7. An operating and service manual and a manual insert are provided with each special option instrument. The operating and service manual contains information about the standard instrument. The manual insert for the special option describes the factory modifications required to produce the special option instrument. Amend the operating and service manual by changing it to include all manual insert information (and MANUAL CHANGES sheet information, if applicable). When these changes are made, the operating and service manual will apply to the special option instrument.

7-8. If you have ordered a special option instrument and the manual insert is missing, notify the nearest Hewlett-Packard Sales/Service Office. Be sure to give a full description of the instrument, including the complete serial number and special option number.

## 7-9. STANDARD OPTIONS.

7-10. Standard options are modifications installed on HP instruments at the factory and are available on request. Contact the nearest Hewlett-Packard Sales/Service Office for information concerning standard options.

## 7-11. MANUAL CHANGES LISTING.

### CHANGE 1

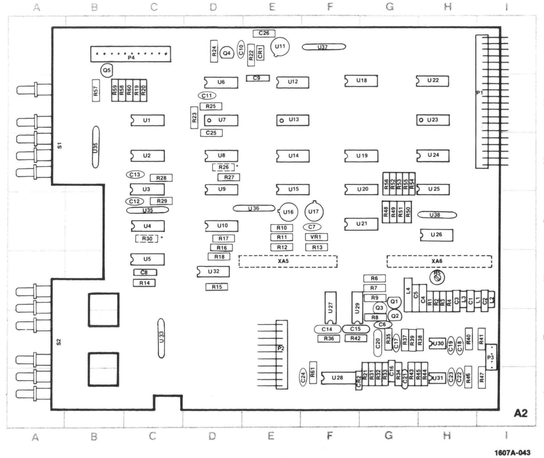
Table 6-2,

A2: Change to HP Part No. 01607-66501; description unchanged.
Q1: Change to HP Part No. 1854-0320; TRANSISTOR NPN SI PD = 83.5W FT = 4 MHz; Mfr Code 28480; Mfr Part No. 1854-0320.
A2C14: Change to HP Part No. 0140-0202; CAPACITOR-FXD 15 PF +—5% 500 WVDC MICA 0+; Mfr Code 72136; Mfr Part No. DM15C150J0500-WV1CR.
A2C15: Change to HP Part No. 0140-0202; CAPACITOR-FXD, 15 PF +—5% 500 WVDC MICA 0+; Mfr Code 72136; Mfr Part No. DM15C150J-0500WV1CR.
A2C25: Change to HP Part No. 0180-0197; CAPACITOR-FXD, 2.2 UF +—10% 20VDC TA; Mfr Code 56289; Mfr Part No. 150D225X9020A2.
A2CR3: Delete.
A2Q6: Delete.
A2R62: Delete.
A2U32: Change to HP Part No. 1820-0068; IC DGTL SN74 10 N GATE, Mfr Code 01295; Mfr Part No. SN7410N.

Figure 8-14,
Replace A2 component locator with figure 7-1.
Replace schematic 10 with figure 7-2.

Figure 8-16,
Replace schematic 12 with figure 7-3.

Figure 8-18,
Delete CR3 on schematic 14 per figure 7-4.




| REF DESIG | GRID LOC | REF DESIG | GRID LOC | REF DESIG | GRID LOC | REF DESIG | GRID LOC | REF DESIG | GRID LOC |
|---|---|---|---|---|---|---|---|---|---|
| C1 | H-5 | L2 | I-5 | R18 | D-5 | R47 | I-7 | U13 | E-2 |
| C2 | I-5 | L3 | H-5 | R19 | C-2 | R48 | G-4 | U14 | E-3 |
| C3 | H-5 | L4 | G-5 | R20 | C-2 | R49 | G-4 | U15 | E-3 |
| C4 | H-5 | P1 | G-7 | R21 | G-7 | R50 | G-4 | U16 | E-4 |
| C5 | G-5 | P2 | E-6 | R22 | E-1 | R51 | G-4 | U17 | F-4 |
| C6 | G-6 | P3 | I-6 | R23 | D-2 | R52 | G-3 | U18 | G-2 |
| C7 | F-4 | P4 | C-1 | R24 | D-1 | R53 | C-3 | U19 | G-3 |
| C8 | C-5 | Q1 | G-5 | R25 | D-2 | R54 | G-3 | U20 | G-3 |
| C9 | E-2 | Q2 | G-6 | R26 * | D-3 | R55 | G-3 | U21 | G-4 |
| C10 | D-1 | Q3 | G-5 | R27 | D-3 | R56 | G-3 | U22 | H-2 |
| C11 | D-2 | Q4 | D-1 | R28 | C-3 | R57 | B-2 | U23 | H-2 |
| C12 | C-4 | Q5 | B-1 | R29 | C-4 | R58 | B-2 | U24 | H-3 |
| C13 | C-3 | R1 | H-5 | R30 * | C-4 | R59 | B-2 | U25 | H-3 |
| C14 | F-6 | R2 | H-5 | R31 | G-7 | R60 | C-2 | U26 | H-4 |
| C15 | F-6 | R3 | H-5 | R32 | G-7 | R61 | F-7 | U27 | F-5 |
| C16 | G-7 | R4 | H-5 | R33 | G-7 | S1 | A-3 | U28 | F-7 |
| C17 | G-6 | R5 | H-5 | R34 | G-7 | S2 | A-6 | U29 | F-5 |
| C18 | H-6 | R6 | G-5 | R35 | G-6 | U1 | C-2 | U30 | H-6 |
| C19 | H-6 | R7 | G-5 | R36 | F-6 | U2 | C-3 | U31 | H-7 |
| C20 | G-6 | R8 | G-6 | R37 | G-6 | U3 | C-3 | U32 | D-5 |
| C21 | G-7 | R9 | G-5 | R38 | H-6 | U4 | C-4 | U33 | C-6 |
| C22 | H-7 | R10 | E-4 | R39 | G-6 | U5 | C-5 | U34 | C-4 |
| C23 | H-7 | R11 | E-4 | R40 | H-6 | U6 | D-2 | U35 | B-3 |
| C24 | F-7 | R12 | E-4 | R41 | I-6 | U7 | D-2 | U36 | E-4 |
| C25 | D-3 | R13 | F-4 | R42 | F-6 | U8 | D-3 | U37 | F-1 |
| C26 | E-1 | R14 | C-5 | R43 | G-7 | U9 | D-3 | U38 | H-4 |
| CR1 | E-1 | R15 | D-5 | R44 | H-7 | U10 | D-4 | VR1 | F-4 |
| CR2 | F-7 | R16 | D-4 | R45 | G-7 | U11 | E-1 | XA5 | E-5 |
| L1 | H-5 | R17 | D-4 | R46 | H-7 | U12 | E-2 | XA6 | H-5 |

* NOT LOADED AT FACTORY

*Figure 7-1. Figure 3-14 Replacement*

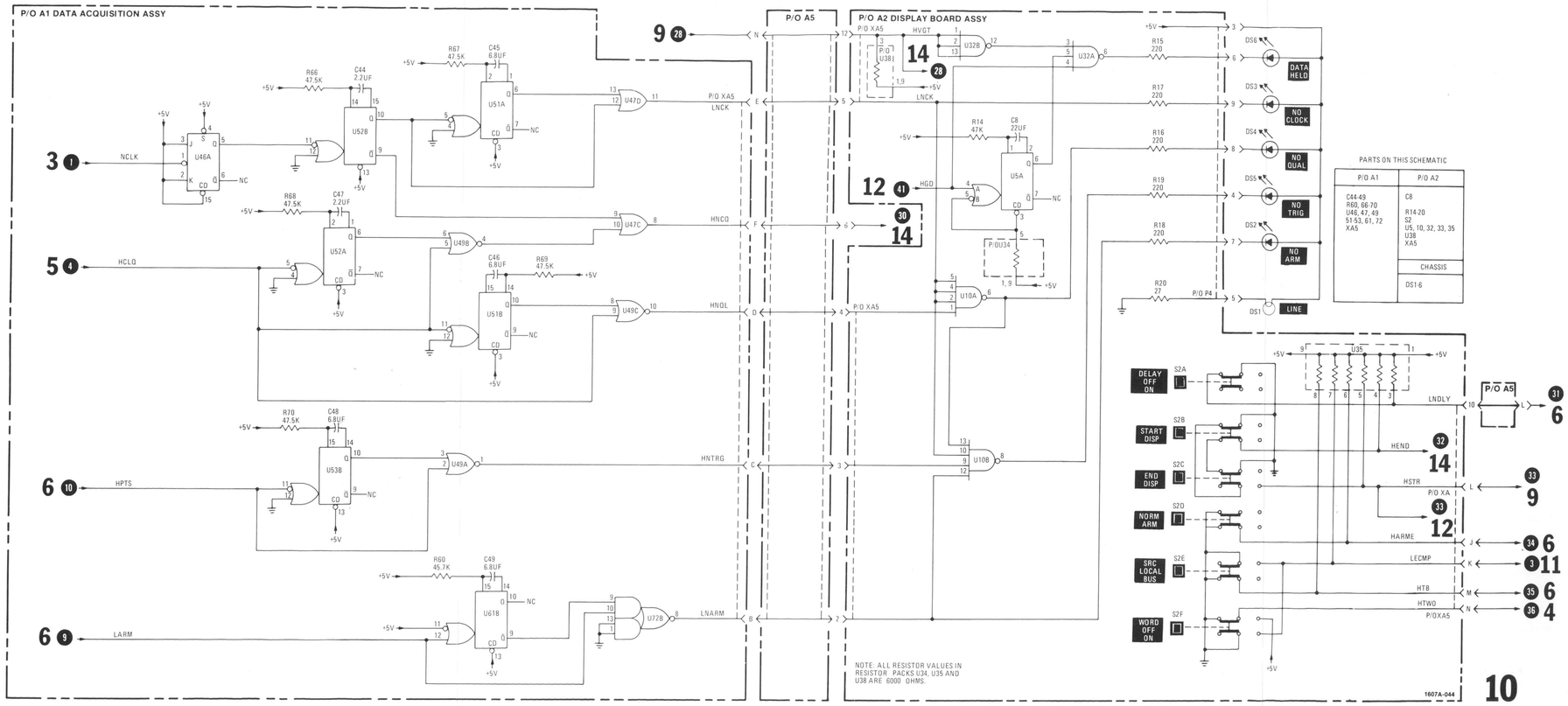



*Figure 7-2. Schematic 10 Replacement*

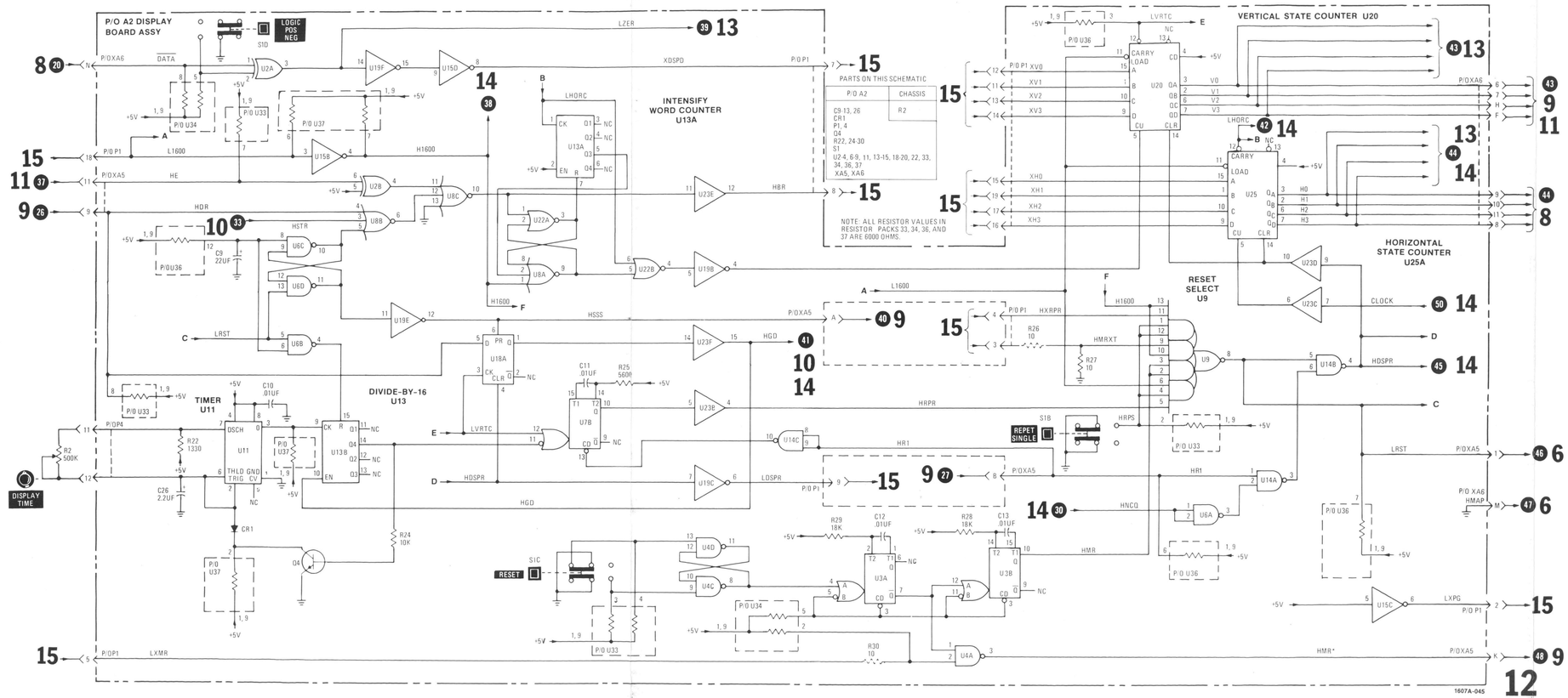



*Figure 7-3. Schematic 12 Replacement*

Figure 7-3. Schematic 12 Replacement Under Fold

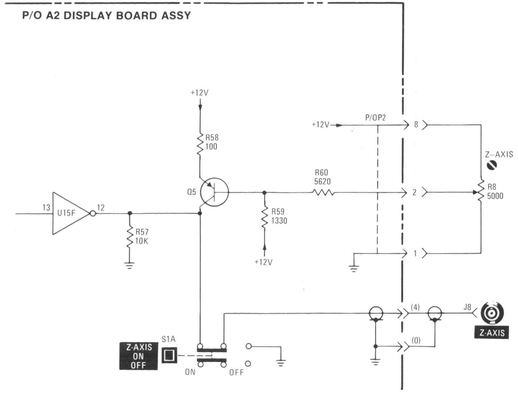



*Figure 7-4. Schematic 14 Changes*

# SECTION VIII

# SCHEMATICS AND TROUBLESHOOTING

## 8-1. INTRODUCTION.

8-2. This section contains schematics, repair and replacement information, component-identification illustrations, waveforms, test conditions, troubleshooting charts, timing diagrams, and truth tables.

## 8-3. SCHEMATICS.

8-4. The schematics indicate electronic functions of the Model 1607A circuitry. Any one schematic may include all or part of several different physical assemblies. Tables 8-1 and 8-2 define symbols and conventions used in the schematics. Figure 8-1 provides terminal identification drawings for semiconductors used in the Model 1607A. Figure 8-20 provides power, ground, and logic connections for integrated circuits (IC's) used in the Model 1607A.

8-5. The schematics are numbered in sequence with a bold number at the lower right-hand corner of each page. At each circuit breaking point, a notation is made of the signal name and two numbers. The white number on a black background is the number assigned to that signal and is used to cross reference signal connections between schematics. The number in bold type is the number of the schematic which shows the source or destination of the signal. To find the source or destination of any point on a given schematic, turn to the schematic referred to by number and find the number and name of the signal in question. Refer to table 4-1 for a list of logic term definitions and origins. Letters are used to cross reference circuit breaking points when both the signal source and signal destination are contained on the same schematic.

8-6. Square-pin connections are identified by the color code of the connecting wire. Ribbon-connector pins and sockets are identified by a number (see figure 8-2).

8-7. A table on each schematic lists all components shown on the schematic by reference designation. Component reference designators which have been deleted from the schematic are listed below the table.

## 8-8. REFERENCE DESIGNATIONS.

8-9. The unit system of reference designations used in this manual is in accordance with the provisions of American National Standard Y32.16, Reference Designations for Electrical and Electronics Parts and Equipments. Minor variations from the standard, due to design and manufacturing practices, may be noted.

8-10. Each electrical component is assigned a class letter and a number. This letter-number combination is the basic reference designation. Components which are not part of an assembly have only the basic reference designation. Components which are part of an assembly have, in addition to the basic designation, a prefix designation indicating the assembly of which the component is a part (resistor R23 on assembly A1 is called A1R23).

8-11. Assemblies are numbered consecutively. If an assembly reference designation is assigned and later deleted, that number is not reused.

## 8-12. COMPONENT LOCATIONS.

8-13. Locations of components on assemblies and subassemblies are shown in illustrations adjacent to the schematics. Since the schematics indicate electronic function, portions of a particular assembly may appear on several different schematics. The component-location illustration is printed next to the schematic that shows most of the circuitry on the assembly. Exploded-view drawings showing mechanical (and some electrical) parts are located in Section VI.

## 8-14. REPAIR AND REPLACEMENT.

**WARNING**

Read the safety summary at the front of this manual before troubleshooting the instrument.

8-15. The following paragraphs provide procedures for removal and replacement of assemblies, subassemblies, and components in the Model 1607A. Special servicing instructions for circuit boards and integrated circuits are covered, and Section VI provides a detailed parts list for use in ordering replacement parts.

### 8-16. MECHANICAL DISASSEMBLY AND BOARD REMOVAL.

**NOTE**

See illustrations in Section VI for locations of mechanical parts (MP reference designations).

*Table 8-1. Schematic Notes*

**REFER TO ANSI Y 32.2 AND Y32.14 FOR SCHEMATIC SYMBOLS NOT LISTED IN THIS TABLE.**


ETCHED CIRCUIT BOARD


ASSEMBLY

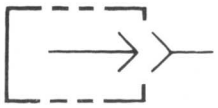

ETCHED CIRCUIT BOARD ON ASSEMBLY


FRONT- AND REAR-PANEL MARKING

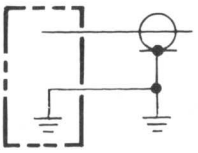

MAIN SIGNAL PATH

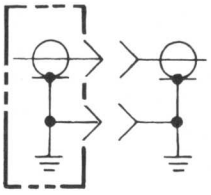

PRIMARY FEEDBACK PATH


SECONDARY FEEDBACK PATH


SINGLE-PIN CONNECTOR ON BOARD

PIN OF A PLUG-IN BOARD (WITH LETTER OR NUMBER)


COAXIAL CABLE CONNECTED DIRECTLY TO BOARD


COAXIAL CABLE CONNECTED TO SNAP-ON JACK


FRONT-PANEL CONTROL

TEST POINT (TP WITH NUMBER)


SCREWDRIVER ADJUSTMENT

WAVEFORM TEST POINT (WITH NUMBER)

COMMON ELECTRICAL POINT (WITH LETTER); NOT NECESSARILY GROUND

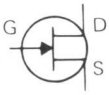
SIGNAL REFERENCE

SCHEMATIC REFERENCE


BREAKDOWN DIODE (VOLTAGE REGULATOR)


LIGHT EMITTING DIODE (LED)


TUNNEL DIODE



FIELD-EFFECT TRANSISTOR (N-TYPE BASE)


CIRCUITS OR COMPONENTS DRAWN WITH DASHED LINES (PHANTOM) SHOW FUNCTION ONLY AND ARE NOT INTENDED TO BE COMPLETE. THE CIRCUIT OR COMPONENT IS SHOWN IN DETAIL ON ANOTHER SCHEMATIC.

(925) WIRE COLORS ARE GIVEN BY NUMBERS IN PARENTHESIS USING THE RESISTOR COLOR CODE

[ (925) IS WHT-RED-GRN ]

| | |
|---|---|
| 0 - BLACK | 5 - GREEN |
| 1 - BROWN | 6 - BLUE |
| 2 - RED | 7 - VIOLET |
| 3 - ORANGE | 8 - GRAY |
| 4 - YELLOW | 9 - WHITE |

* OPTIMUM VALUE SELECTED AT FACTORY, TYPICAL VALUE SHOWN; PART MAY HAVE BEEN OMITTED.

UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS, CAPACITANCE IN PICOFARADS AND INDUCTANCE IN MICROHENRIES

| | |
|---|---|
| CW | CLOCKWISE END OF VARIABLE RESISTOR |
| NC | NO CONNECTION |
| P/O | PART OF |

VF (A)

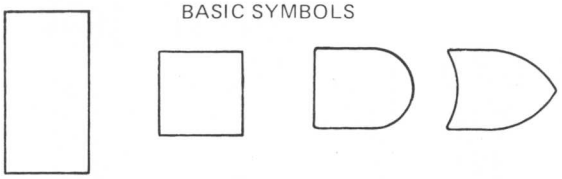
V - VOLTAGE
F - FILTERED
(A) - FILTER SOURCE

*Table 8-2. Logic Symbols*

Refer to American National Standard Y32.14 for Logic Symbols not listed in this table.

## GENERAL ELEMENT SYMBOLS

BASIC SYMBOLS

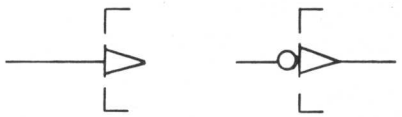


CONTIGUOUS BLOCK

## INDICATOR SYMBOLS

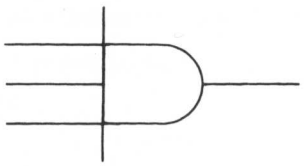
NEGATION INDICATOR

DYNAMIC INDICATOR

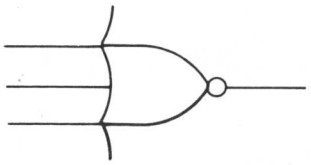


## COMBINATIONAL LOGIC SYMBOLS

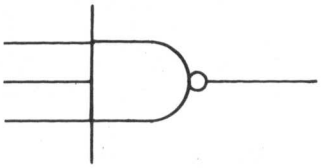
AND FUNCTION



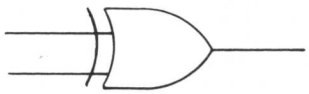
NOR FUNCTION



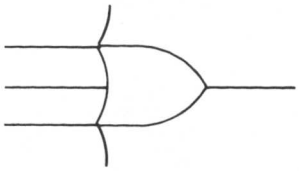
NAND FUNCTION



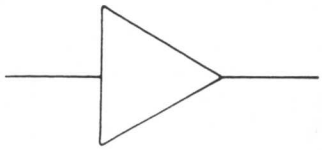
EXCLUSIVE OR FUNCTION



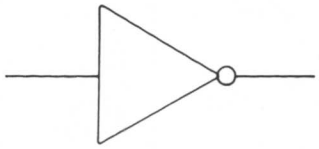
OR FUNCTION



NON-INVERTING AMPLIFIER



INVERTING AMPLIFIER



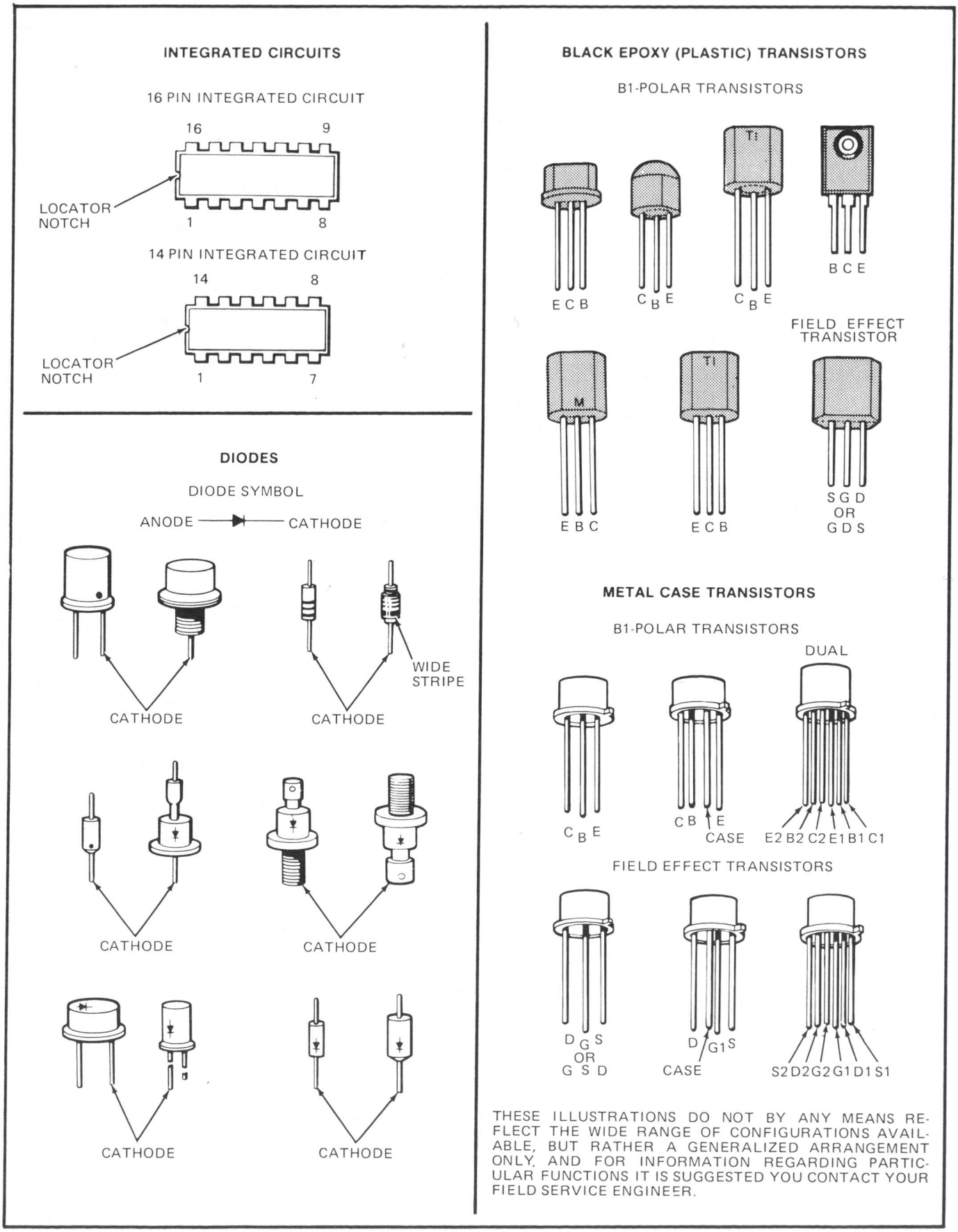



*Figure 8-1. Semiconductor Terminal Identification*

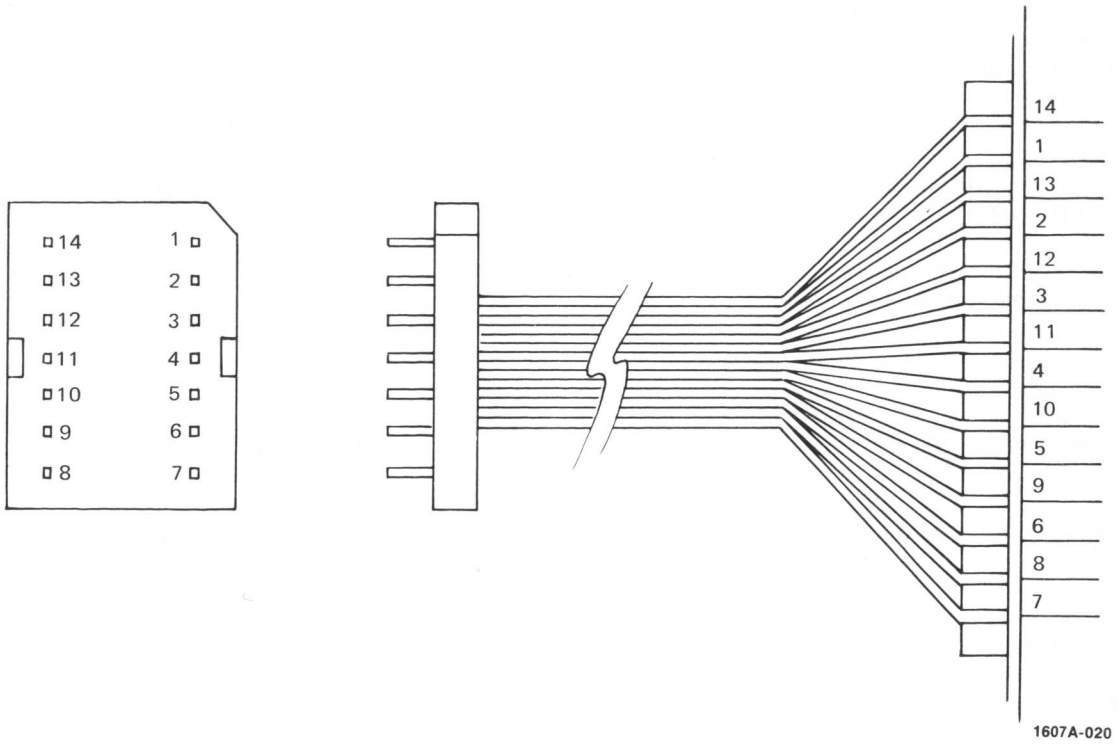



*Figure 8-2. Ribbon Connector Pin Identification*

**8-17. Rear-panel Power Supply Assembly Removal.**

a. Disconnect main power cable, and remove top and bottom covers (MP4 and MP5).

b. Disconnect all cable connectors and square-pin connectors between rear-panel assembly and display board A2.

c. Unscrew coupler MP26 on power switch extender MP10 from switch on power supply board A3.

d. Remove 4 corner screws holding rear panel MP3 to rear frame casting MP6.

e. Carefully pull rear-panel/power supply assembly to the rear, and remove it from the instrument.

**8-18. Data Acquisition Board A1 Removal.**

a. Disconnect main power cable, and remove top and bottom covers (MP4 and MP5).

b. Disconnect square-pin connections from circuit side of A1 board.

c. Remove four screws attaching A1 board to bracket MP2.

d. Lift back of A1 board, and disconnect A1XA5 and A1XA6 connectors from extender boards A5 and A6.

e. Slide A1 board back from front panel until switches and connectors are disengaged, then tilt rear of A1 board up.

f. Disconnect ribbon connectors J5 through J9 from circuit side of A1 board.

**8-19. Display Board A2 Removal.**

a. Disconnect main power cable, and remove top and bottom covers (MP4 and MP5).

b. Disconnect all cable and square-pin connectors from A2 board.

c. Disconnect cable connector W4J1 (soldered to A2 board) from power supply board A3.

d. Disconnect square-pin connectors from trigger output BNC's through A2 board to data acquisition board A1. Square pins are located on circuit side of A1 board.

e. Remove 4 screws securing A2 board to bracket MP23.

f. Lift back of A2 board until A2XA5 and A2XA6 are disconnected from extender boards A5 and A6.

g. Slide A2 board back from front panel until switches and connectors are disengaged, then left A2 board out of instrument.

**8-20. Front-panel Assembly Removal.**

a. Remove boards A1 and A2 as described in paragraphs 8-18 and 8-19.

b. Remove 4 corner screws holding front-panel assembly to frame casting MP6.

c. Pull front-panel assembly forward out of chassis.

**8-21. Delay Board A7/Trigger Switch Board A4 Removal.**

a. Remove front-panel assembly as described in paragraph 8-20.

b. Remove screws holding A4 and A7 boards to front-panel assembly.

**8-22. SERVICING CIRCUIT BOARDS.** This instrument uses circuit boards with plated-through component holes. This allows components to be removed or replaced by unsoldering or soldering from either side of the board. When removing large components, such as potentiometers, rotate the soldering iron tip from lead to lead while applying pressure to the part to lift it from the board. HP Service Note M-20E contains additional information on the repair of circuit boards.

**8-23. SEMICONDUCTOR REPLACEMENT.** Figure 8-1 is included to help identify the leads in the common shapes and sizes of semiconductor devices. When removing a semiconductor, use long-nosed pliers as a heat sink between the device and the soldering iron. When replacing a semiconductor, ensure sufficient lead length to dissipate the soldering heat by using the same length of exposed lead as was used for the original part.

**8-24. INTEGRATED CIRCUIT HANDLING.** Many of the integrated circuits in the Model 1607A are in the CMOS family of digital devices. CMOS devices can be damaged by static voltages in the service environment. To protect CMOS devices during handling, the following procedures are suggested:

a. Ground all test equipment.

b. Use grounded-tip soldering irons.

c. Disconnect all low-impedance test equipment (such as pulse generators) from device inputs before removing dc power supplies.

d. Store unused CMOS devices in conductive rails or conductive foam, or short all device leads together.

**8-25. INTEGRATED CIRCUIT REPLACEMENT.** Soldered IC units may be removed with soldering irons which simultaneously heat all connections (available from various manufacturers). Soldering irons with built-in desoldering tools facilitate quick removal.

**CAUTION**

Unless an IC has definitely failed, becareful to prevent damage when removing or replacing it.

8-26. To remove an IC with a standard soldering iron, proceed as follows:

a. Heat IC lead solder joint. Use soldering iron with small pencil tip (such as Weller No. PT-H7).

b. When solder is fluid, remove it with desoldering aid (such as Soldapullt manufactured by Edsyn Company of California).

c. Repeat steps a and b for each IC lead until all leads are free.

d. Grasp each lead with long-nosed pliers and check that it is mechanically free from circuit board.

e. When all leads are free, carefully remove IC. Dual in-line type may be removed by gently gripping top and bottom with long-nosed pliers and rolling IC out.

f. Use desoldering tool or toothpick to remove all remaining solder from circuit board holes.

**CAUTION**

Use care to prevent IC damage with heat from the soldering iron. Word quickly.

g. Insert replacement IC into circuit board and solder it in place.

8-27. When replacing an IC, note the mark or notch used for orientation. The component identification illustrations and the IC pin-location diagrams in figure 8-1 show IC orientation.

## 8-28. TROUBLESHOOTING.

8-29. The most important prerequisites for successful troubleshooting are an understanding of the instrument functional operation and the correct use of front-panel controls. Suspected malfunctions may be caused by improper control settings. Before performing the test and/or troubleshooting procedures, refer to Section III for an explanation of controls, connectors, and general operating considerations. Refer to Section IV for an explanation of circuit functional operation.

8-30. If trouble is suspected, visually inspect the instrument. Look for loose or burned components that might suggest a source of trouble. Check to see that all circuit board connections are making good contact and are not shorting to an adjacent circuit. If no obvious trouble is found, check the instrument supply voltages, and the external power sources.

**8-31. DC VOLTAGES.** On some schematics, dc voltages are indicated at certain points in the circuit. Test equipment and control setups for making voltage measurements are provided in Section V. Check these setup conditions before making any measurements.

**8-32. WAVEFORMS.** Waveforms are placed on the schematics along main signal paths. Test equipment and control setups for making these measurements are listed in Section V. Check these setup conditions before making any measurements.

**8-33. TEST POINTS.** Test points are shown on the schematics with this symbol (⊙). Test points usually correspond to pins protruding from circuit boards and do not necessarily correspond to waveform measurement points.

**8-34. FAULT ISOLATION.** Figure 8-3 provides a fault isolation procedure in flow-chart form. Malfunctions can be isolated to a specific circuit or component by following the step-by-step instructions. Refer to table 4-1 for a list of mnemonic definitions and origins. Refer to Section IV for flow charts, block diagrams, and simplified schematics showing the operation of circuits contained in the Model 1607A.

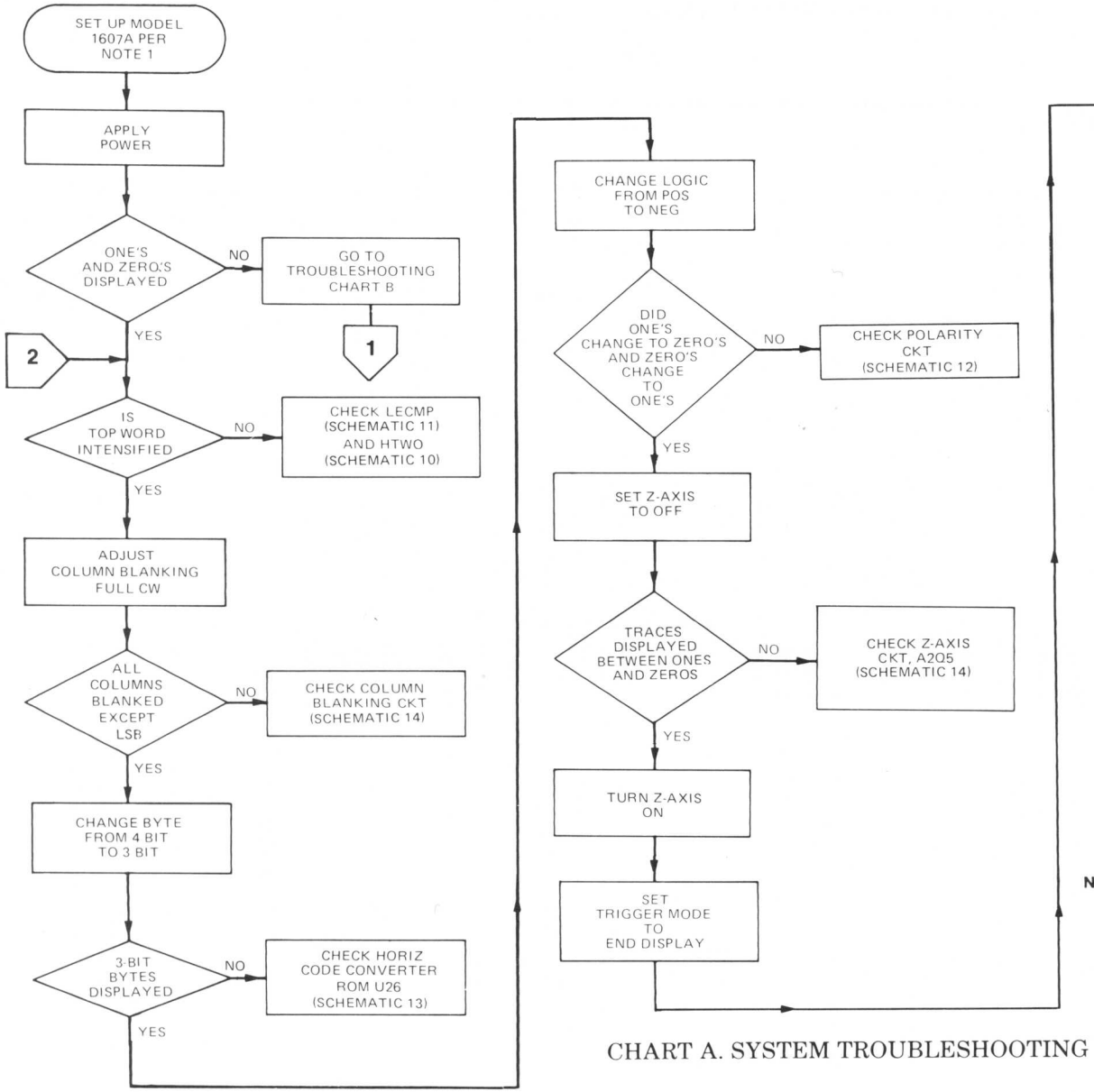



CHART A. SYSTEM TROUBLESHOOTING

**NOTE 1:** A. CONNECT MODEL 1607A TO DISPLAY MONITOR PER PARAGRAPH 3-39, STEPS A THROUGH C.

B. MODEL 1607A FRONT PANEL TROUBLESHOOTING SETUP:

| | |
|---|---|
| SAMPLE MODE | SINGLE |
| TRIGGER MODE | START DSPL |
| WORD | ON |
| DELAY | OFF |
| THUMBWHEELS | ALL 0's |
| COLUMN BLANKING | FULL CCW |
| LOGIC | POS |
| BYTE | 4 BIT |

1607A-026

*Figure 8-3. Troubleshooting Charts (Sheet 1 of 3)*

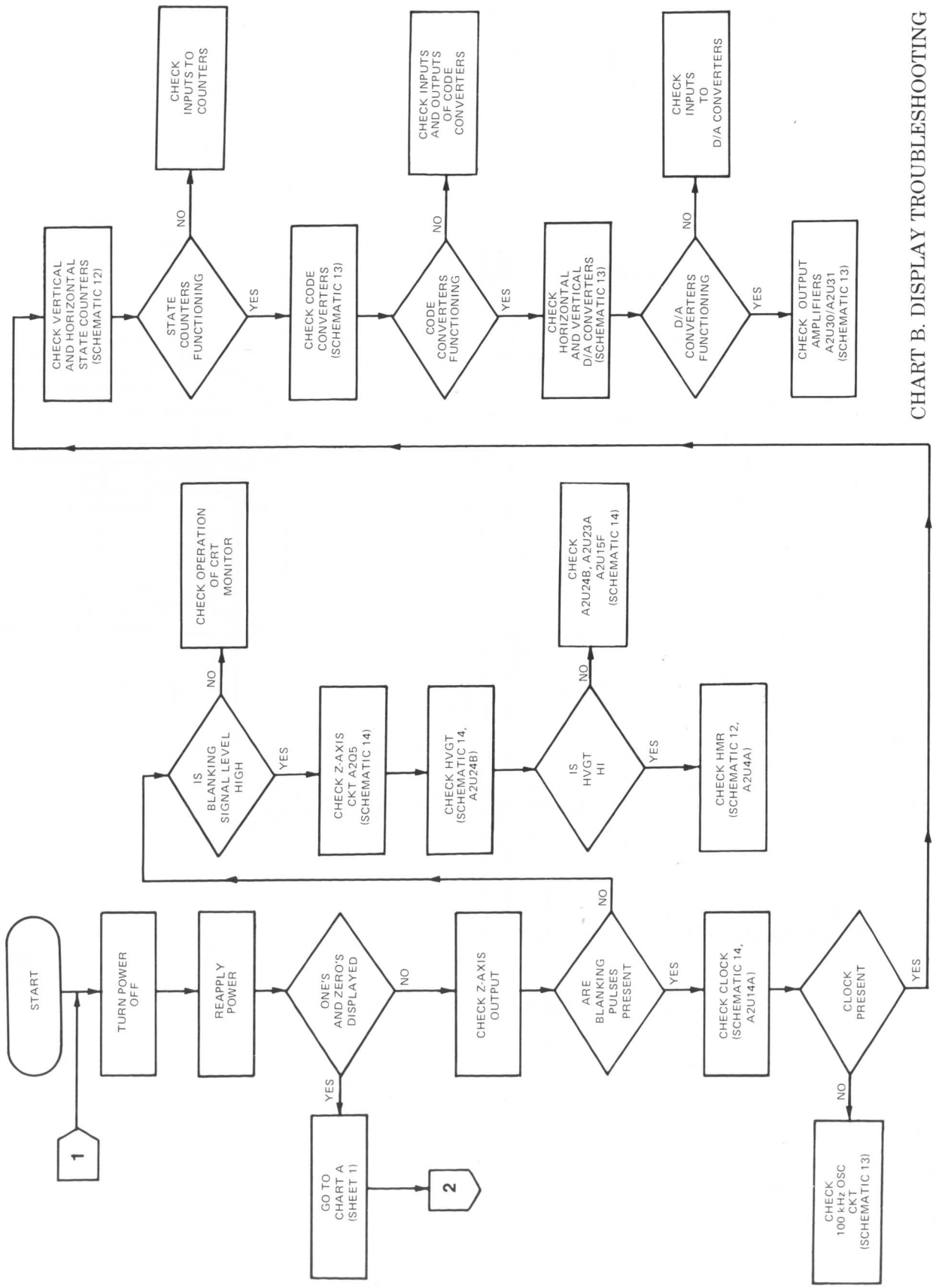



*Figure 8-3. Troubleshooting Charts (Sheet 2 of 3)*

**NOTE 2:** INSTRUMENT SETUP FOR CHART C.

A. CONNECT TEST EQUIPMENT AS SHOWN IN FIGURE 5-1.

B. SET MODEL 1607A CONTROLS AS FOLLOWS:

| | |
|---|---|
| CLOCK | ⌐¯ |
| THLD | TTL |
| QUALIFIER | |
| Q0, Q1 | HI |
| DSPL/TRIG | TRIG |
| SAMPLE MODE | REPET |
| TRIGGER MODE | |
| START DSPL | ON |
| NORM/ARM | NORM |
| LOCAL/BUS | LOCAL |
| WORD | ON |
| TRIGGER WORD | ALL HI |

C. APPLY WAVEFORMS SHOWN IN FIGURE 5-2 to CLOCK AND DATA INPUTS.

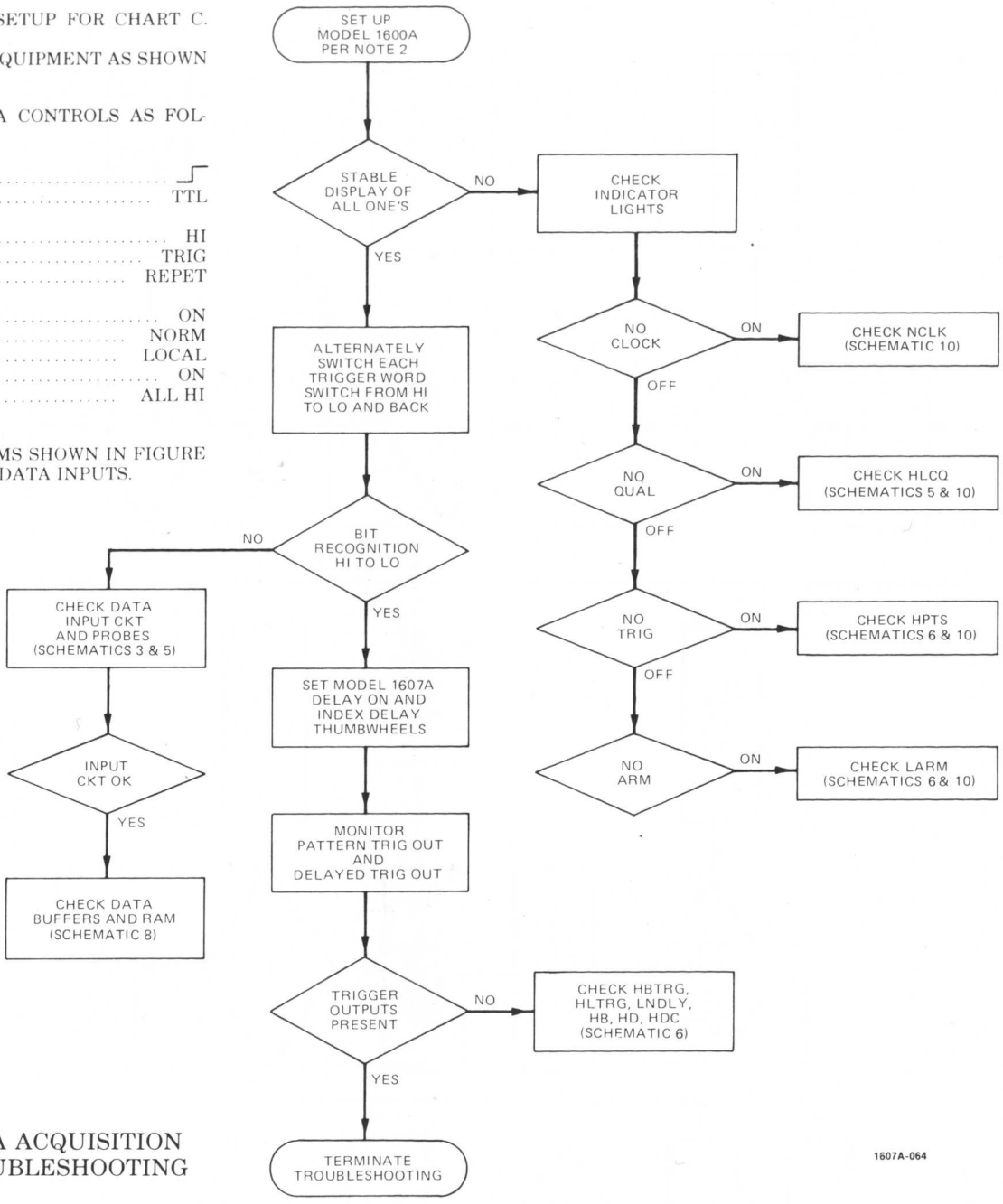



CHART C. DATA ACQUISITION TROUBLESHOOTING

*Figure 8-3. Troubleshooting Charts (Sheet 3 of 3)*

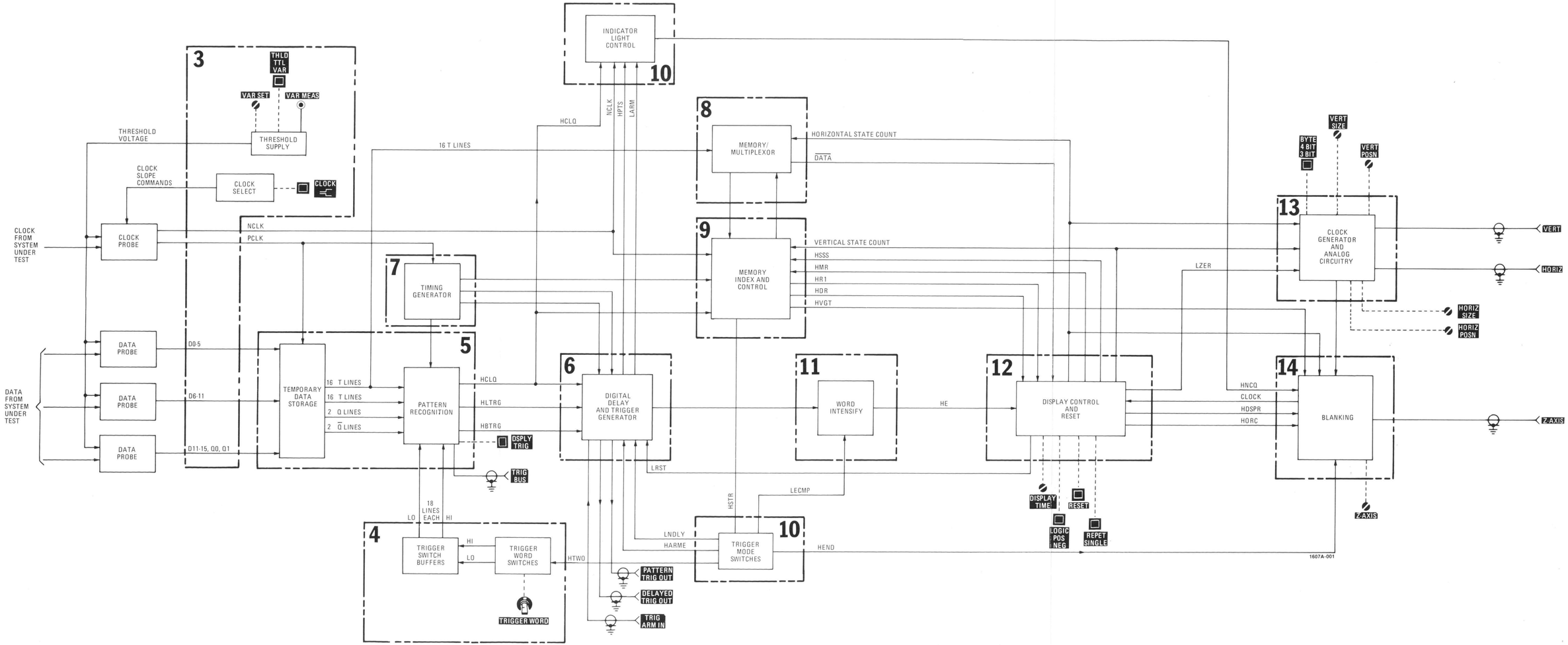



*Figure 8-4.*
*Model 1607A Block Diagram*
8-11/(8-12 blank)

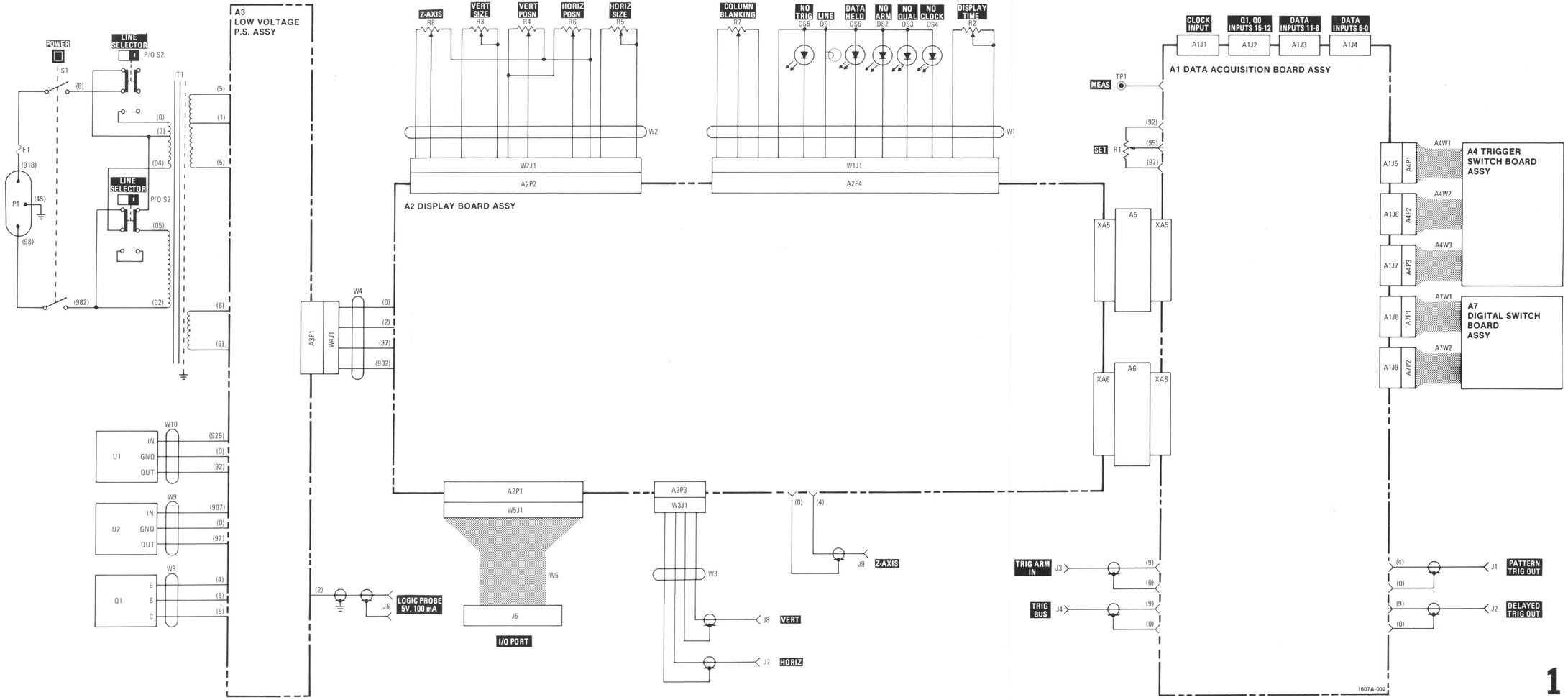
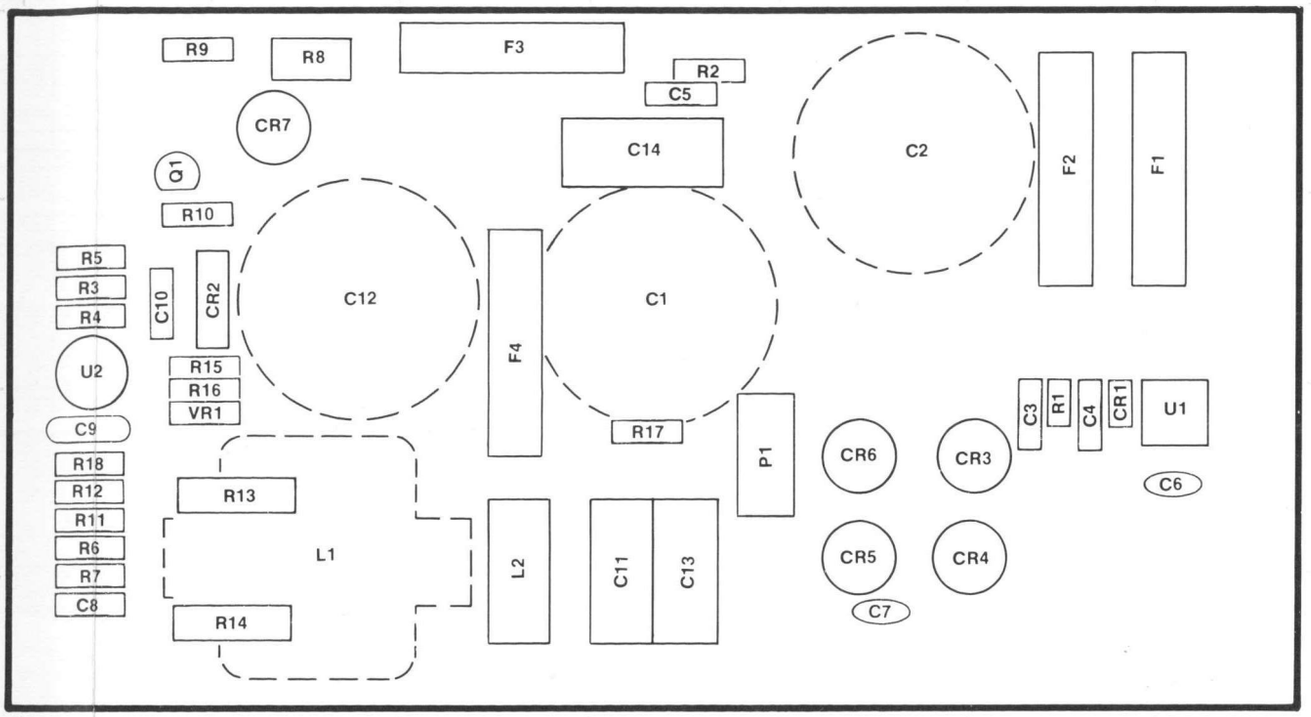



*Figure 8-5.*
*Schematic 1, Model 1607A Interconnection Diagram*




| REF DESIG | GRID LOC | REF DESIG | GRID LOC | REF DESIG | GRID LOC | REF DESIG | GRID LOC | REF DESIG | GRID LOC |
|---|---|---|---|---|---|---|---|---|---|
| C1 | E-3 | C11 | D-4 | CR7 | C-2 | R2 | E-2 | R12 | B-4 |
| C2 | F-2 | C12 | C-3 | F1 | G-2 | R3 | B-3 | R13 | B-4 |
| C3 | G-3 | C13 | E-4 | F2 | G-2 | R4 | B-3 | R14 | B-4 |
| C4 | G-3 | C14 | E-2 | F3 | D-1 | R5 | B-2 | R15 | B-3 |
| C5 | E-2 | CR1 | G-3 | F4 | D-3 | R6 | B-4 | R16 | B-3 |
| C6 | G-4 | CR2 | B-3 | L1 | C-4 | R7 | B-4 | R17 | E-3 |
| C7 | F-4 | CR3 | F-4 | L2 | D-4 | R8 | C-1 | R18 | B-4 |
| C8 | B-4 | CR4 | F-4 | P1 | E-4 | R9 | B-1 | U1 | G-3 |
| C9 | B-3 | CR5 | F-4 | Q1 | B-2 | R10 | B-2 | U2 | B-3 |
| C10 | B-3 | CR6 | F-4 | R1 | G-3 | R11 | B-4 | VR1 | B-3 |

*Figure 8-6. Schematic 2, Low Voltage Power Distribution, Assembly A3 (Sheet 1 of 3)*

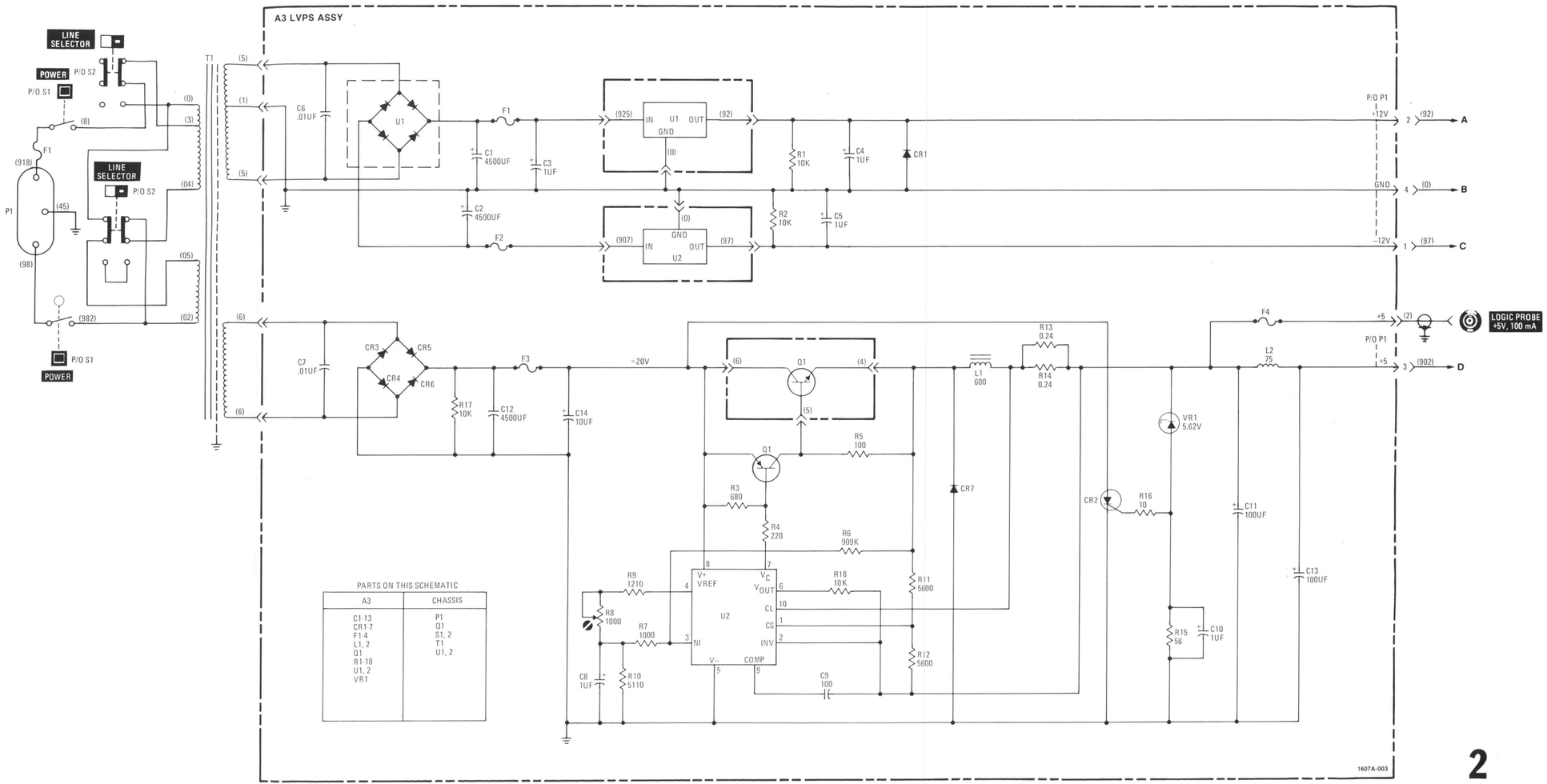



*Figure 8-6.*
*Schematic 2, Low Voltage Power Distribution, Assembly A3 (Sheet 2 of 3)*

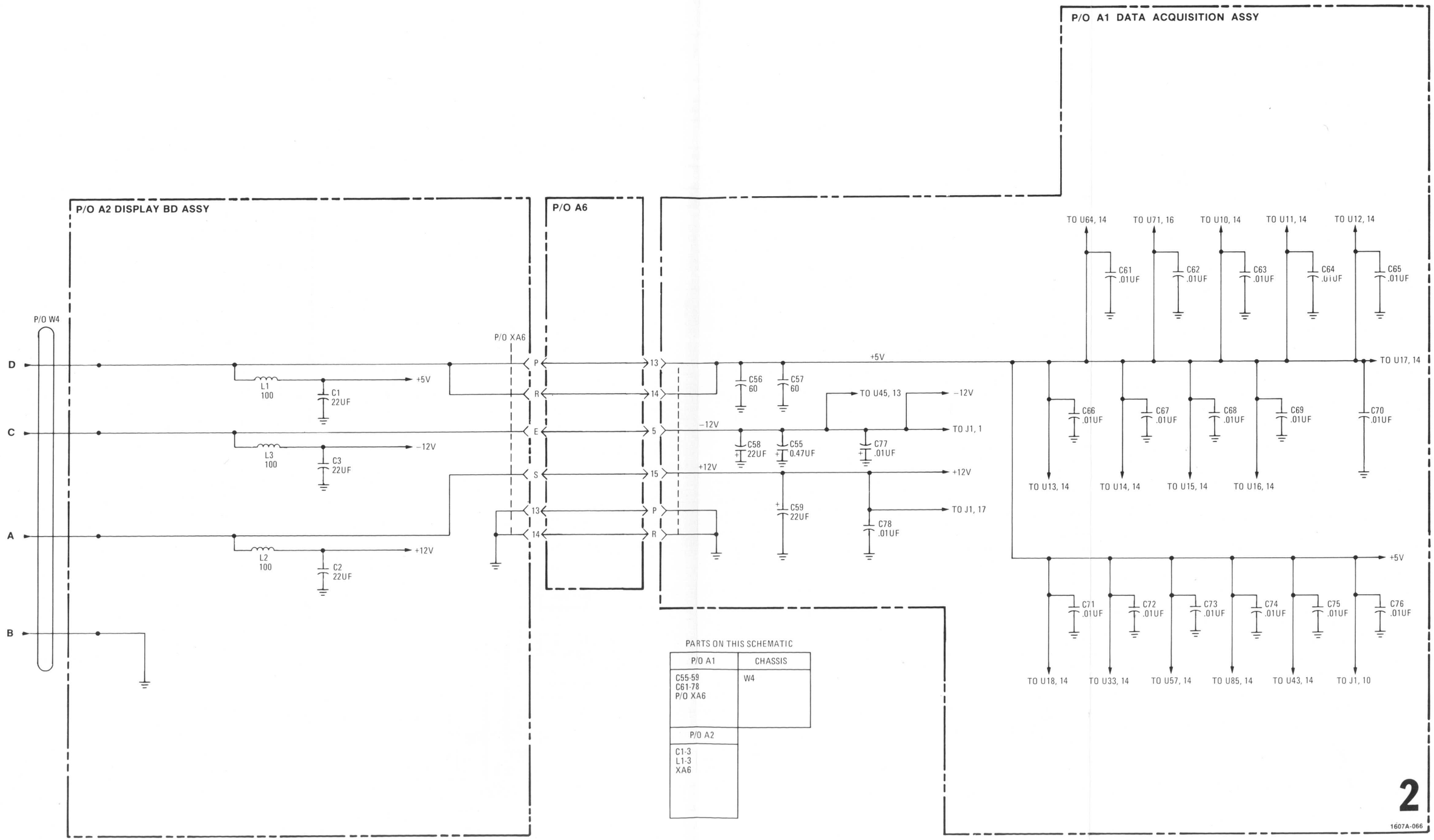
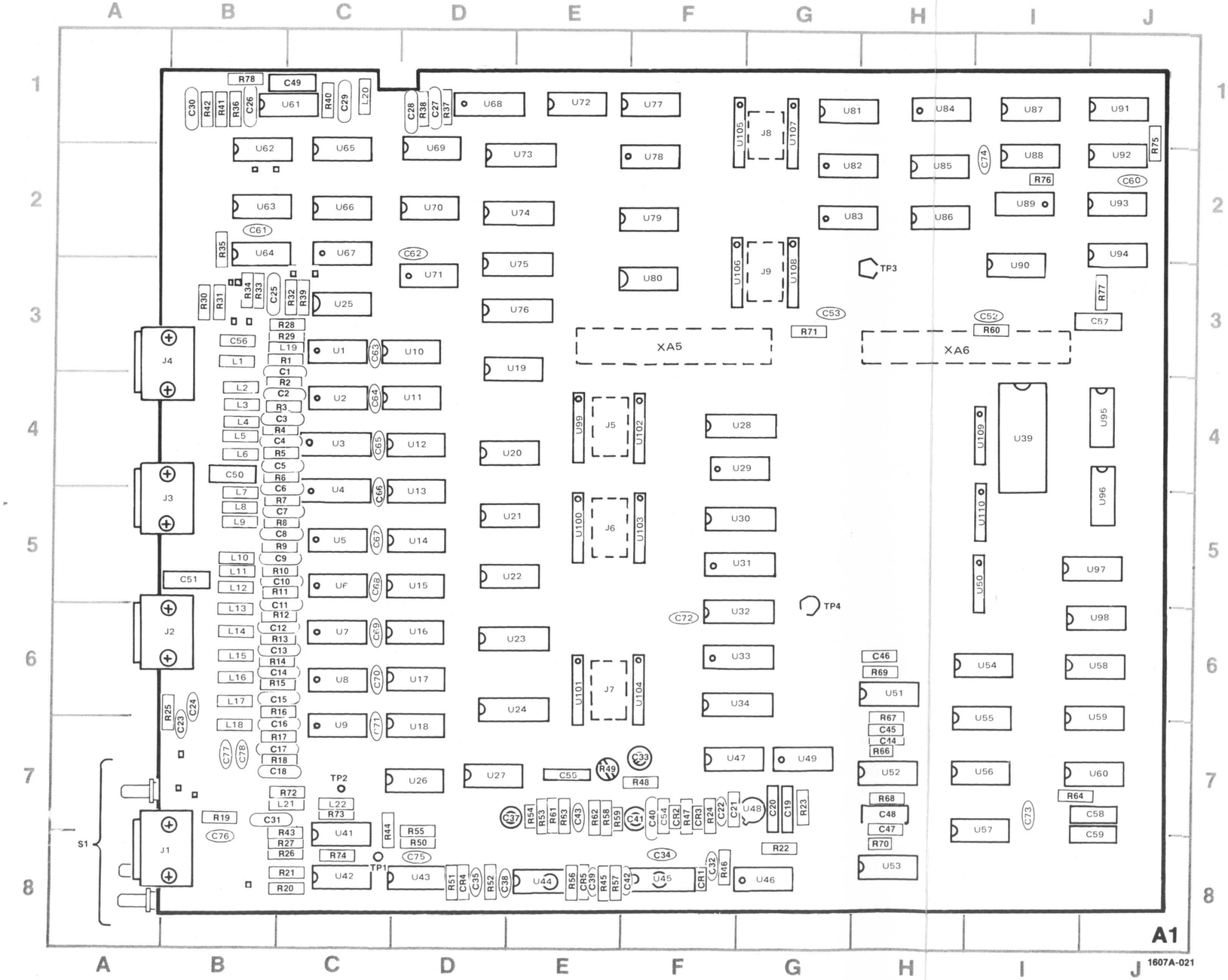



*Figure 8-6.*
*Schematic 2, Low Voltage Power Distribution, Assembly A3 (Sheet 3 of 3)*




| REF DESIG | GRID LOC | REF DESIG | GRID LOC | REF DESIG | GRID LOC | REF DESIG | GRID LOC | REF DESIG | GRID LOC |
|---|---|---|---|---|---|---|---|---|---|
| C1 | B-3 | C63 | C-3 | R10 | B-5 | R72 | C-7 | U55 | I-6 |
| C2 | B-4 | C64 | C-4 | R11 | B-5 | R73 | C-7 | U56 | I-7 |
| C3 | B-4 | C65 | C-4 | R12 | B-6 | R74 | C-8 | U57 | I-7 |
| C4 | B-4 | C66 | C-4 | R13 | B-6 | R75 | J-1 | U58 | J-6 |
| C5 | B-4 | C67 | C-5 | R14 | B-6 | R76 | I-2 | U59 | J-6 |
| C6 | B-4 | C68 | C-5 | R15 | B-6 | R77 | J-3 | U60 | J-7 |
| C7 | B-5 | C69 | C-6 | R16 | B-6 | R78 | B-1 | U61 | B-1 |
| C8 | B-5 | C70 | C-6 | R17 | B-7 | S1 | A-8 | U62 | B-1 |
| C9 | B-5 | C71 | C-6 | R18 | B-7 | TP1 | C-8 | U63 | B-2 |
| C10 | B-5 | C72 | F-6 | R19 | B-7 | TP2 | C-7 | U64 | B-2 |
| C11 | B-5 | C73 | I-7 | R20 | C-8 | TP3 | H-2 | U65 | C-1 |
| C12 | B-6 | C74 | I-1 | R21 | C-8 | TP4 | G-5 | U66 | C-2 |
| C13 | B-6 | C75 | D-8 | R22 | G-8 | U1 | C-3 | U67 | C-2 |
| C14 | B-6 | C76 | B-7 | R23 | G-7 | U2 | C-4 | U68 | D-1 |
| C15 | B-6 | C77 | B-7 | R24 | F-7 | U3 | C-4 | U69 | D-1 |
| C16 | B-6 | C78 | B-7 | R25 | A-6 | U4 | C-4 | U70 | D-2 |
| C17 | B-7 | CR1 | F-8 | R26 | C-8 | U5 | C-5 | U71 | D-3 |
| C18 | B-7 | CR2 | F-7 | R27 | C-8 | U6 | C-5 | U72 | E-1 |
| C19 | G-7 | CR3 | F-7 | R28 | B-3 | U7 | C-6 | U73 | E-1 |
| C20 | G-7 | CR4 | D-8 | R29 | B-3 | U8 | C-6 | U74 | E-2 |
| C21 | F-7 | CR5 | E-8 | R30 | B-3 | U9 | C-6 | U75 | E-2 |
| C22 | F-7 | J1 | A-8 | R31 | B-3 | U10 | D-3 | U76 | E-3 |
| C23 | B-6 | J2 | A-6 | R32 | C-3 | U11 | D-4 | U77 | F-1 |
| C24 | B-6 | J3 | A-5 | R33 | B-3 | U12 | D-4 | U78 | F-1 |
| C25 | B-3 | J4 | A-3 | R34 | B-3 | U13 | D-4 | U79 | F-2 |
| C26 | B-1 | J5 | E-4 | R35 | B-2 | U14 | D-5 | U80 | F-3 |
| C27 | D-1 | J6 | E-5 | R36 | B-1 | U15 | D-5 | U81 | G-1 |
| C28 | D-1 | J7 | E-6 | R37 | D-1 | U16 | D-6 | U82 | G-2 |
| C29 | C-1 | J8 | G-1 | R38 | D-1 | U17 | D-6 | U83 | G-2 |
| C30 | B-1 | J9 | G-3 | R39 | C-3 | U18 | D-7 | U84 | H-1 |
| C31 | B-7 | L1 | B-3 | R40 | C-1 | U19 | E-3 | U85 | H-2 |
| C32 | F-8 | L2 | B-4 | R41 | B-1 | U20 | E-4 | U86 | H-2 |
| C33 | F-7 | L3 | B-4 | R42 | B-1 | U21 | E-5 | U87 | I-1 |
| C34 | F-8 | L4 | B-4 | R43 | C-7 | U22 | E-5 | U88 | I-1 |
| C35 | D-8 | L5 | B-4 | R44 | C-7 | U23 | E-6 | U89 | I-2 |
| C37 | E-7 | L6 | B-4 | R45 | E-8 | U24 | E-6 | U90 | I-2 |
| C38 | D-8 | L7 | B-4 | R46 | F-8 | U25 | C-3 | U91 | J-1 |
| C39 | E-8 | L8 | B-5 | R47 | F-7 | U26 | D-7 | U92 | J-1 |
| C40 | F-7 | L9 | B-5 | R48 | F-7 | U27 | D-7 | U93 | J-2 |
| C41 | F-7 | L10 | B-5 | R49 | E-7 | U28 | G-4 | U94 | J-2 |
| C42 | F-8 | L11 | B-5 | R50 | D-8 | U29 | G-4 | U95 | J-4 |
| C43 | E-7 | L12 | B-5 | R51 | D-8 | U30 | G-5 | U96 | J-4 |
| C44 | H-7 | L13 | B-5 | R52 | D-8 | U31 | G-5 | U97 | J-5 |
| C45 | H-7 | L14 | B-6 | R53 | E-7 | U32 | G-6 | U98 | J-6 |
| C46 | H-6 | L15 | B-6 | R54 | E-7 | U33 | G-6 | U99 | E-4 |
| C47 | H-7 | L16 | B-6 | R55 | D-7 | U34 | G-6 | U100 | E-5 |
| C48 | H-7 | L17 | B-6 | R56 | E-8 | U39 | I-4 | U101 | E-6 |
| C49 | B-1 | L18 | B-6 | R57 | E-8 | U41 | C-7 | U102 | F-4 |
| C50 | B-4 | L19 | B-3 | R58 | E-7 | U42 | C-8 | U103 | F-5 |
| C51 | B-5 | L20 | C-1 | R59 | E-7 | U43 | D-8 | U104 | F-6 |
| C52 | I-3 | L21 | B-7 | R60 | I-3 | U44 | E-8 | U105 | F-1 |
| C53 | G-3 | L22 | C-7 | R61 | E-7 | U45 | F-8 | U106 | F-3 |
| C54 | F-7 | R1 | B-3 | R62 | E-7 | U46 | G-8 | U107 | G-1 |
| C55 | E-7 | R2 | B-4 | R63 | E-7 | U47 | F-7 | U108 | G-3 |
| C56 | B-3 | R3 | B-4 | R64 | J-7 | U48 | G-7 | U109 | I-4 |
| C57 | J-3 | R4 | B-4 | R66 | H-7 | U49 | G-7 | U110 | I-5 |
| C58 | J-7 | R5 | B-4 | R67 | H-6 | U50 | I-5 | XA5 | F-3 |
| C59 | J-7 | R6 | B-4 | R68 | H-7 | U51 | H-6 | XA6 | H-3 |
| C60 | J-2 | R7 | B-5 | R69 | H-6 | U52 | H-7 | | |
| C61 | B-2 | R8 | B-5 | R70 | H-8 | U53 | H-8 | | |
| C62 | D-2 | R9 | B-5 | R71 | G-3 | U54 | I-6 | | |

*Figure 8-7. Schematic 3, Data Input and Threshold, P/O Assembly A1 (Sheet 1 of 2)*

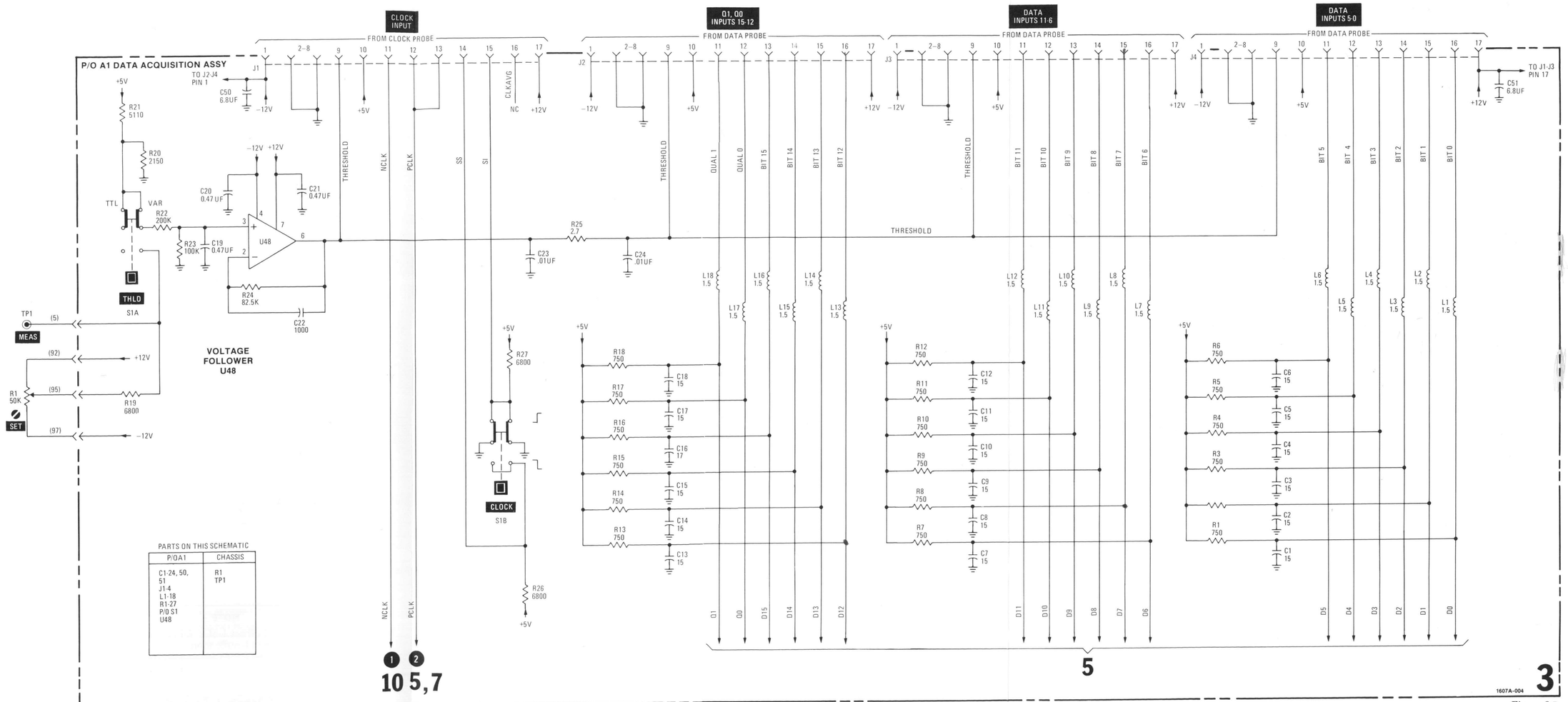
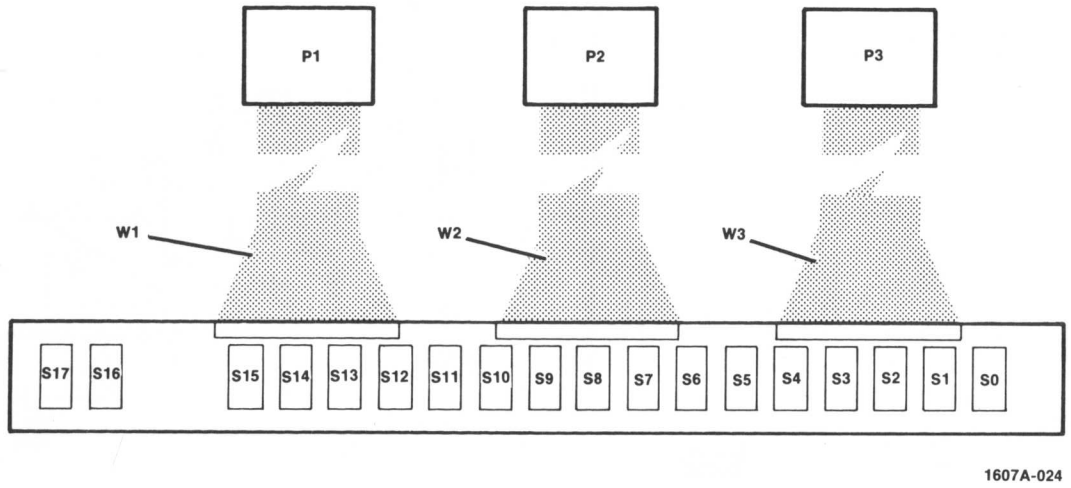



*Figure 8-7.*
*Schematic 3, Data Input and Threshold, P/O Assembly A1 (Sheet 2 of 2)*




**NOTE**

See figure 8-7 (Sheet 1 of 2) for Assembly A1 Component Identification.

**CAUTION**

A1U19 through A1U24 are CMOS devices which can be easily damaged if contacted by static voltage.

*Figure 8-8. Schematic 4, Trigger Word Select, P/O Assembly A1 and Assembly A4 (Sheet 1 of 2)*

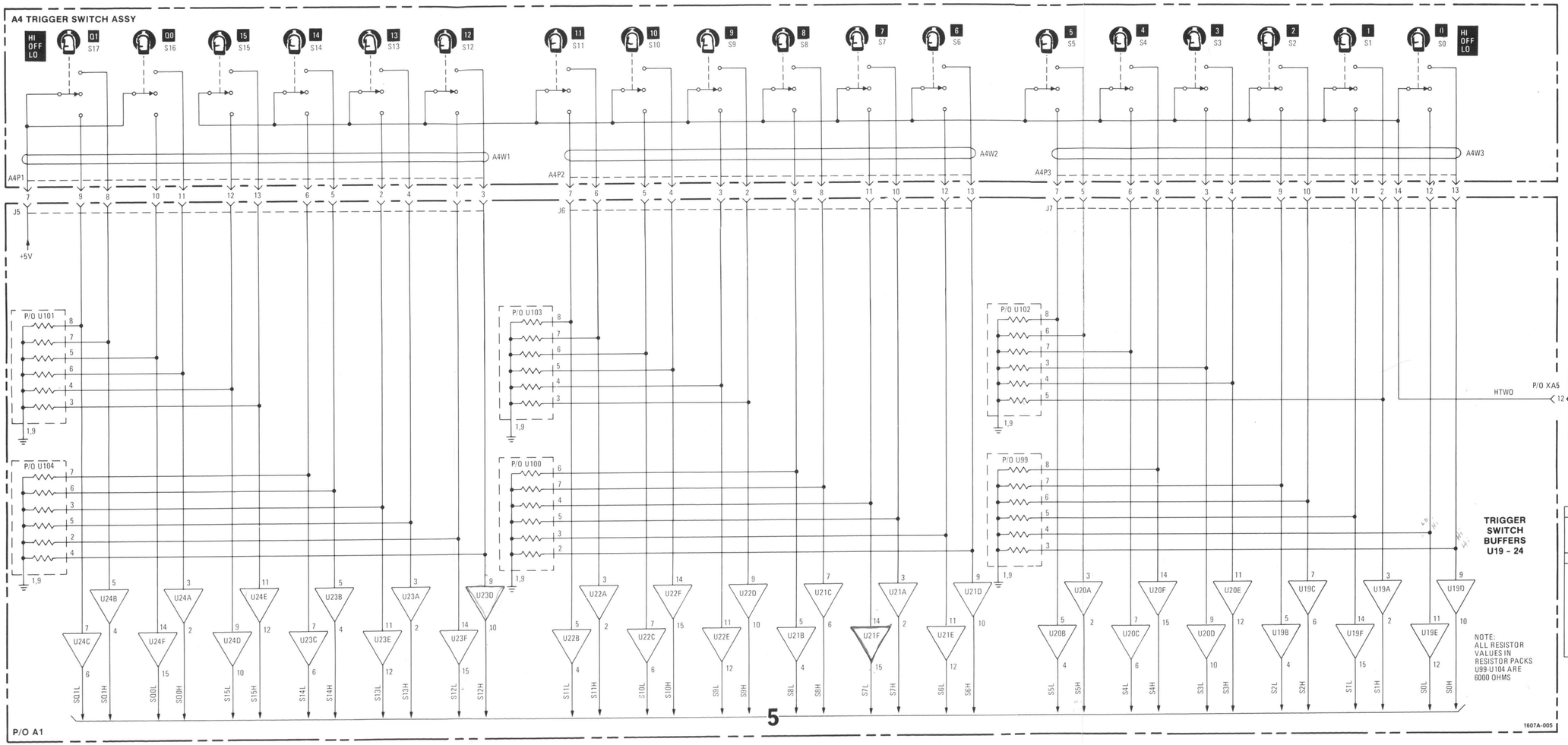



*Figure 8-8.*
*Schematic 4, Trigger Word Select, P/O Assembly A1 and Assembly A4 (Sheet 2 of 2)*

**NOTE**

See figure 8-7 (Sheet 1 of 2) for Assembly A1 Component Identification.

*Figure 8-9. Schematic 5, Temporary Storage and Pattern Recognition, P/O Assembly A1 (Sheet 1 of 2)*

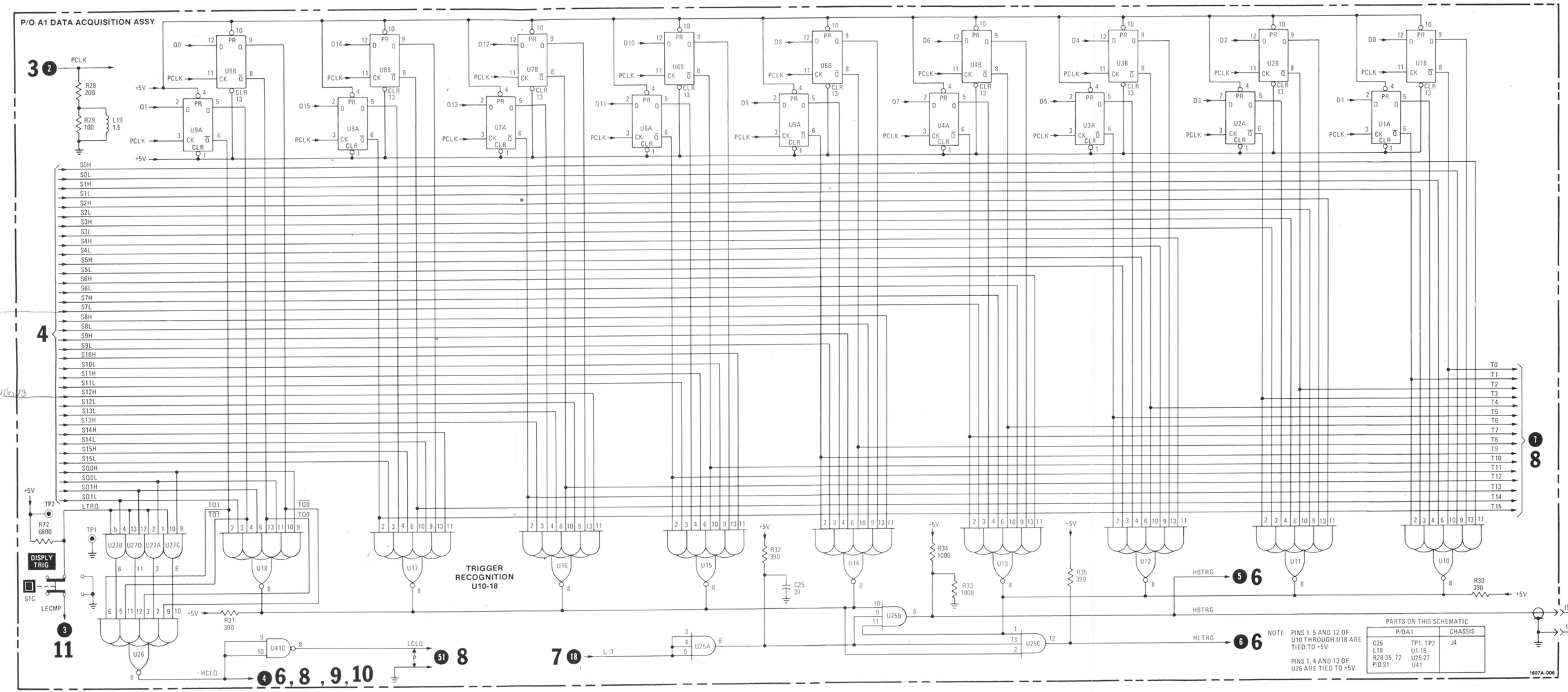
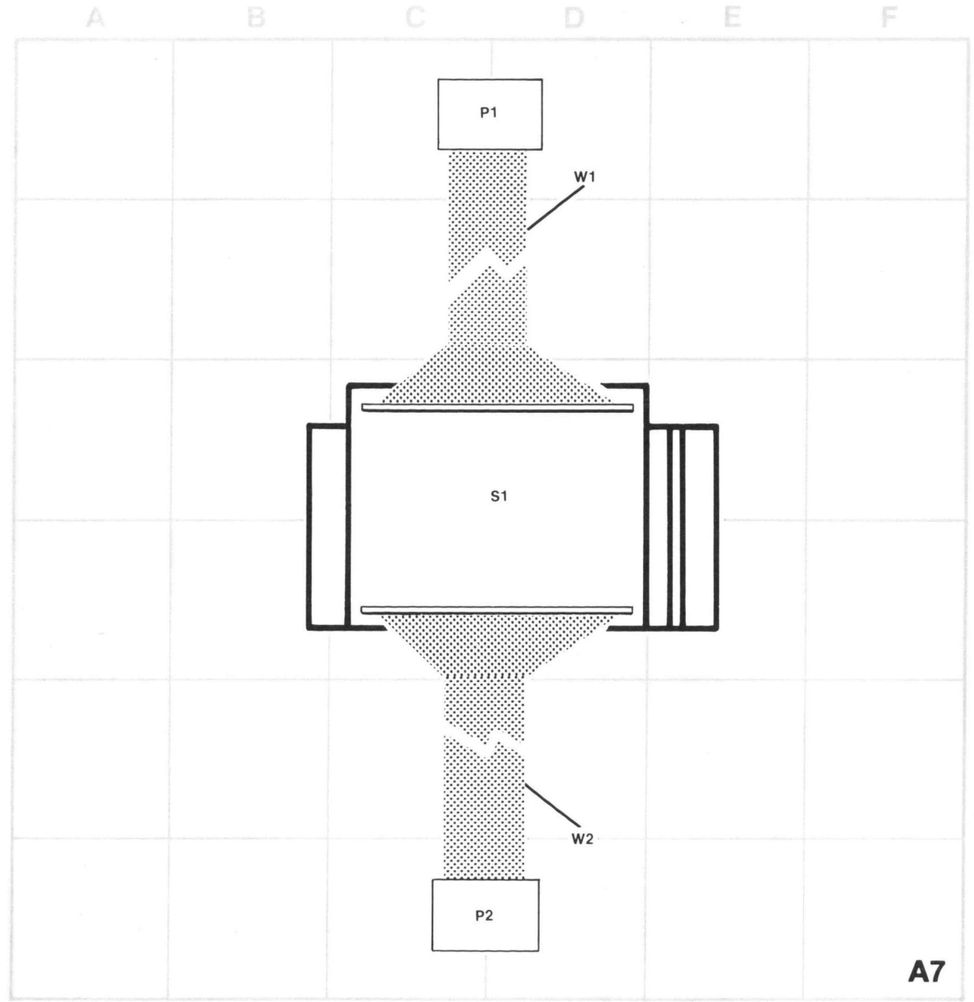



*Figure 8-9.*
*Schematic 5, Tempory Storage and Pattern Recognition, P/O Assembly A1 (Sheet 2 of 2)*

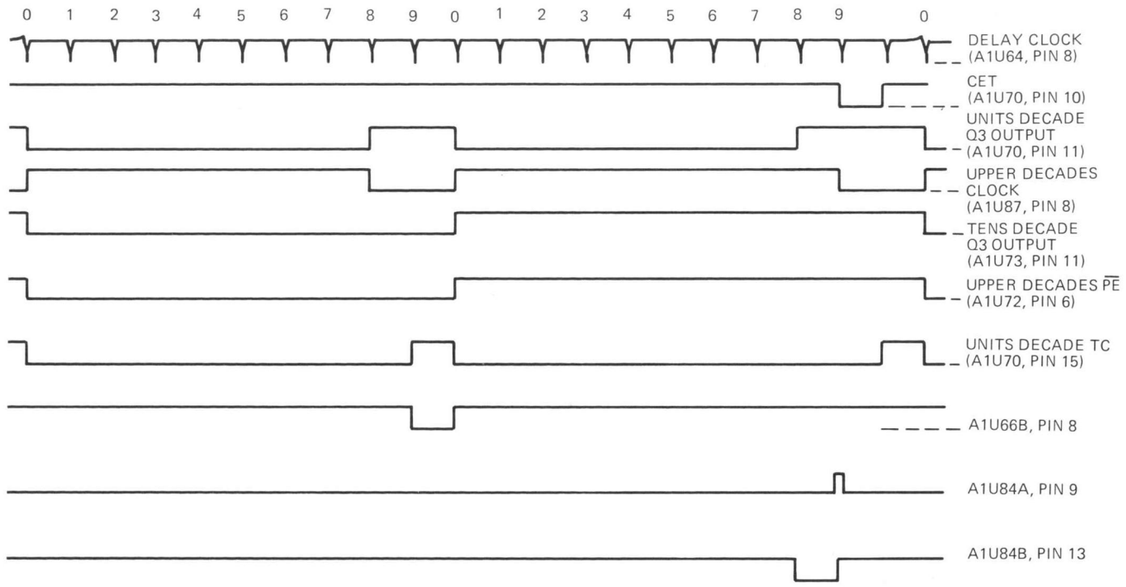



**NOTE**

See figure 8-7 (Sheet 1 of 2) for Assembly A1 Component Identification.



**DIGITAL DELAY TIMING DIAGRAM**
**SCHEMATIC 6**

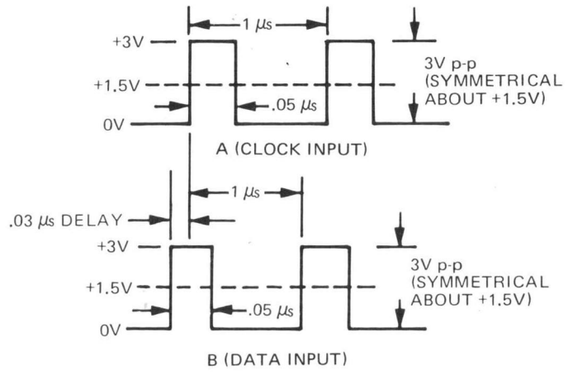



1. Connect test equipment as shown for Operational Check Test Setup in Section V.

2. Set Model 1607A controls as follows:

| | |
|---|---|
| CLOCK | ⌐ |
| THLD | TTL |
| QUALIFIER Q1, Q0 | OFF |
| SAMPLE MODE | REPET |
| START DSPL | ON |
| TRIGGER MODE | |
| NORM/ARM | NORM |
| LOCAL/BUS | LOCAL |
| WORD | ON |
| TRIGGER WORD | All Switches HI |
| DELAY ON/OFF | ON |
| DELAY Thumbwheels | 00020 |

3. Apply waveforms shown below to clock and data inputs.




**NOTE**

1. Unused logic not shown for A1U64, U65, U77, U81, and U87.

U67B/U84A and B* TRUTH TABLE

| J | $\overline{K}$ | Q | $\overline{Q}$ |
|---|---|---|---|
| L | H | NO | CHANGE |
| L | L | L | H |
| H | L | H | L |

* U67A and U71A/B are wired D Flip-Flops

*Figure 8-10. Schematic 6, Digital Delay and Trigger Generator, P/O Assembly A1 and Assembly A7 (Sheet 1 of 2)*

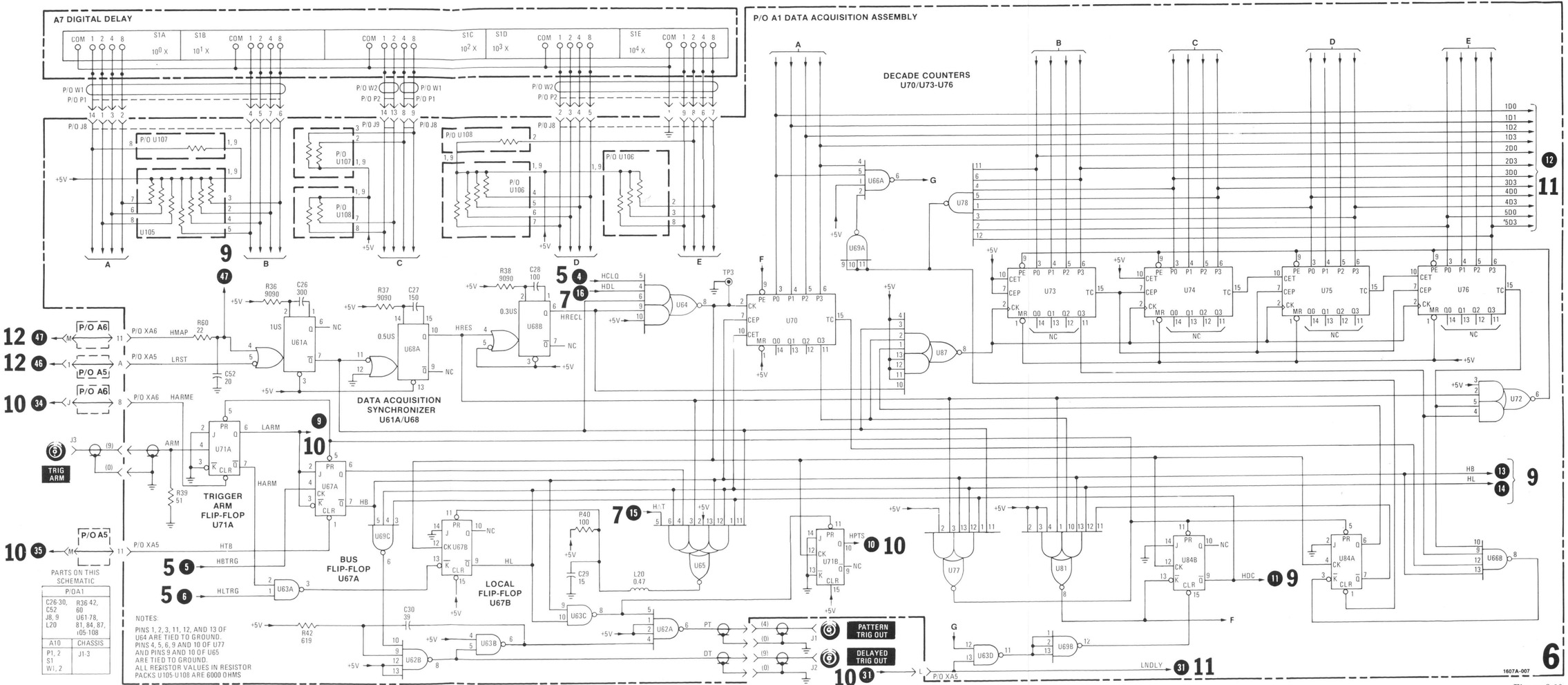


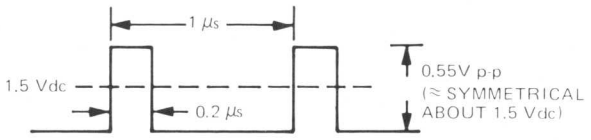

*Figure 8-10.*
*Schematic 6, Digital Delay and Trigger Generator, P/O Assembly A1 and Assembly A7 (Sheet 2 of 2)*

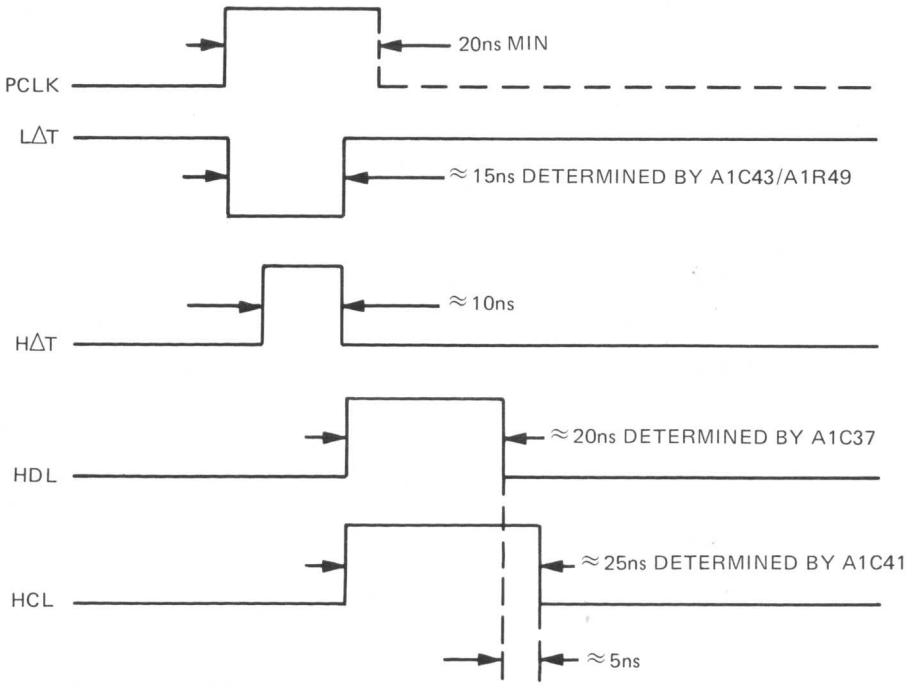
## TIMING GENERATOR TIMING DIAGRAM
## SCHEMATIC 7

1. Set Model 1607A controls as follows.

| | |
|---|---|
| CLOCK | ⌐ |
| THLD | TTL |
| START DSPL | ON |
| WORD | ON |
| QUALIFIER | |
| DSPLY/TRIG | TRIG |
| Q1, Q0 | OFF |
| TRIGGER WORD | Bits 0-15 OFF |

2. Connect HP Model 8013B Pulse Generator OUTPUT (+) connector to CLOCK probe and apply waveform below.



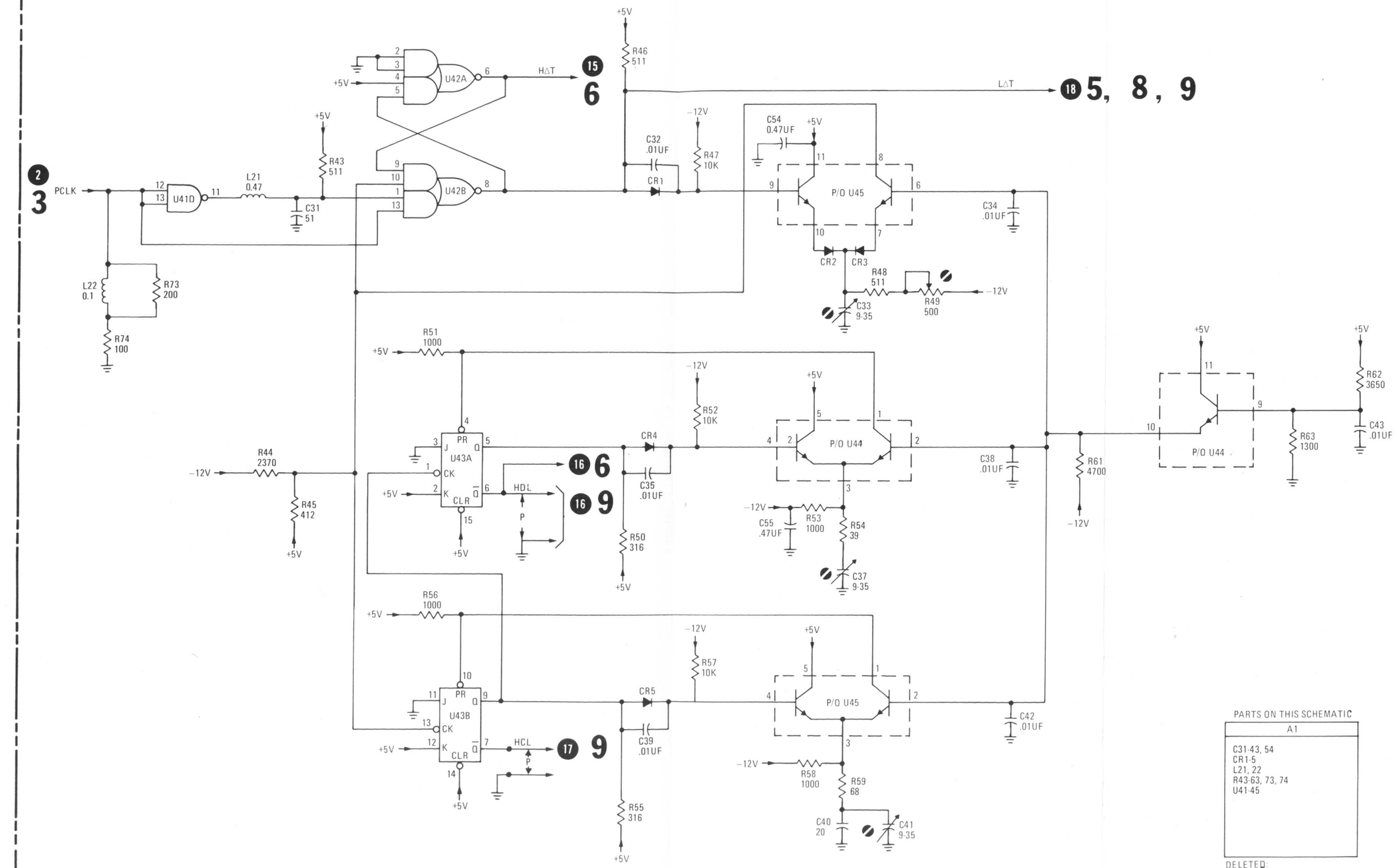




**NOTE**

See figure 8-7 (Sheet 1 of 2) for Assembly A1 Component Identification.

*Figure 8-11. Schematic 7, Timing Generator, P/O Assembly A1 (Sheet 1 of 2)*

P/O A1 DATA ACQUISITION ASSY




PARTS ON THIS SCHEMATIC

| A1 |
|---|
| C31-43, 54<br>CR1-5<br>L21, 22<br>R43-63, 73, 74<br>U41-45 |

DELETED:

1607A-008

7

*Figure 8-11.*
*Schematic 7, Timing Generator, P/O Assembly A1 (Sheet 2 of 2)*

## MEMORY WRITE TIMING DIAGRAM
## SCHEMATIC 8

Set up Model 1607A as follows:

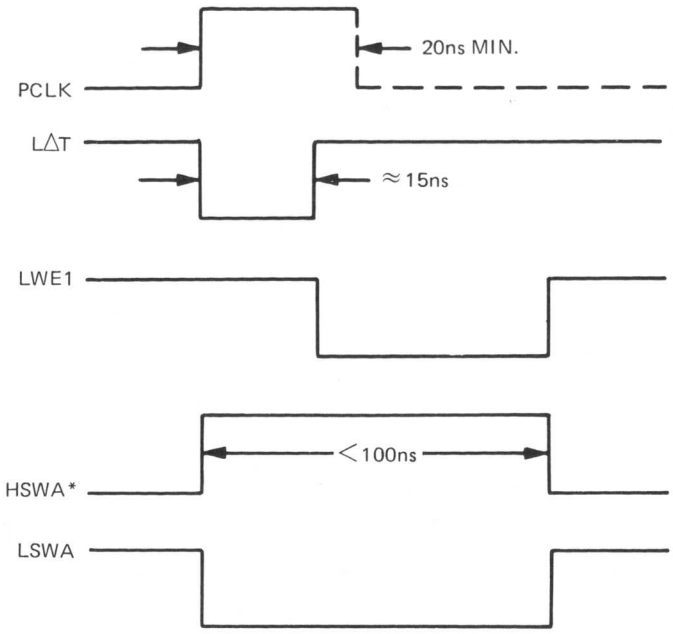
1. Connect Test Equipment as shown for Operational Check Test Setup in Section V.

2. Set Model 1607A controls as follows.

| | |
|---|---|
| CLOCK | ⌐ |
| THLD | TTL |
| QUALIFIER | |
| Q0/Q1 | HI |
| DSPLY/TRIG | TRIG |
| SAMPLE MODE | REPET |
| TRIGGER MODE | |
| START DSPL | ON |
| NORM/ARM | NORM |
| LOCAL/BUS | LOCAL |
| WORD | ON |
| TRIGGER WORD | All Switches HI |

**NOTE**

1. Unused logic not shown for A1U54-A1U57.




**CAUTION**

A1U28 through A1U34, and A1U39 are CMOS devices which are easily damaged if contacted by static voltages.

**NOTE**

See figure 8-7 (Sheet 1 of 2) for Assembly A1 Component Identification.

*Figure 8-12. Schematic 8, Memory/Multiplier, P/O Assembly A1 (Sheet 1 of 2)*

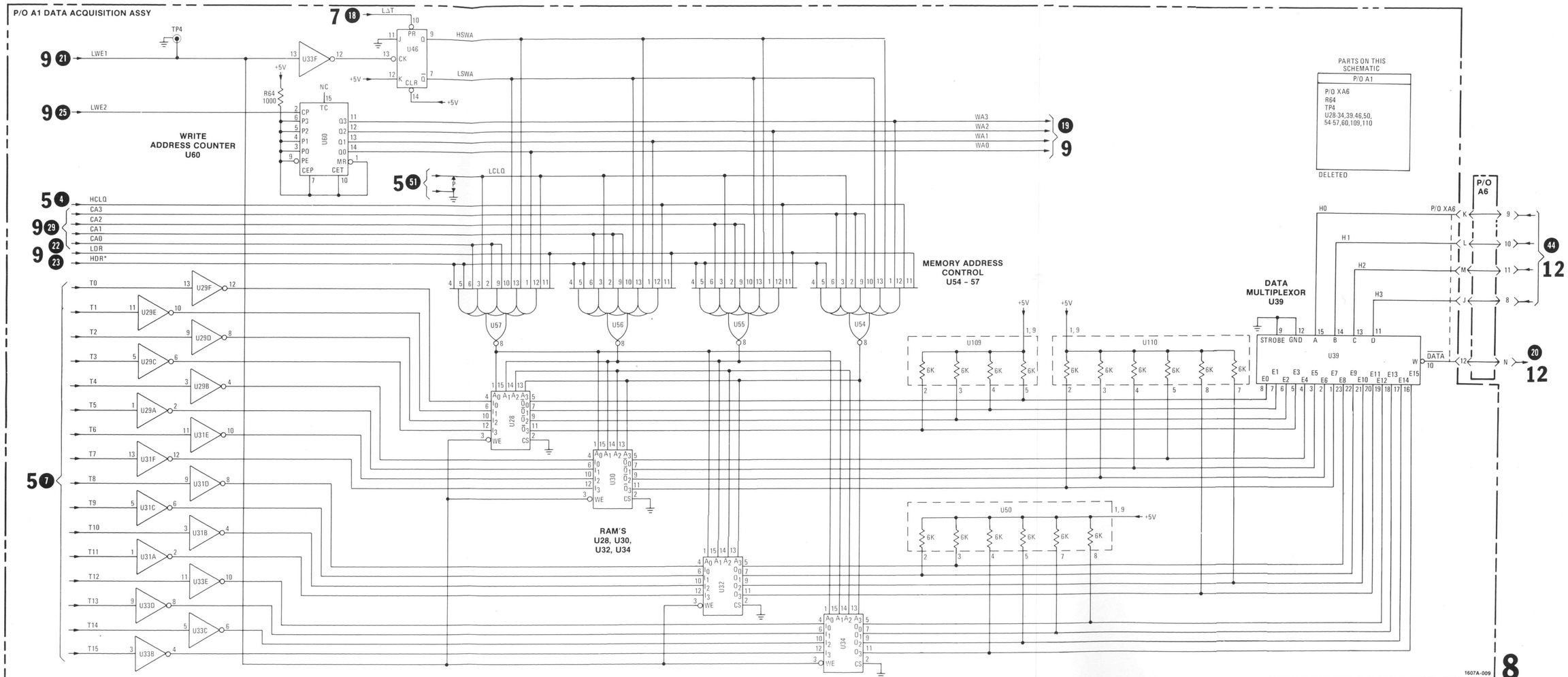



*Figure 8-12.*
*Schematic 8, Memory/Multiplier, P/O Assembly A1 (Sheet 2 of 2)*

**NOTE**

See figure 8-7 (Sheet 1 of 2) for Assembly A1 Component Identification.

*Figure 8-13. Schematic 9, Memory Index and Control, P/O Assembly A1 (Sheet 1 of 2)*

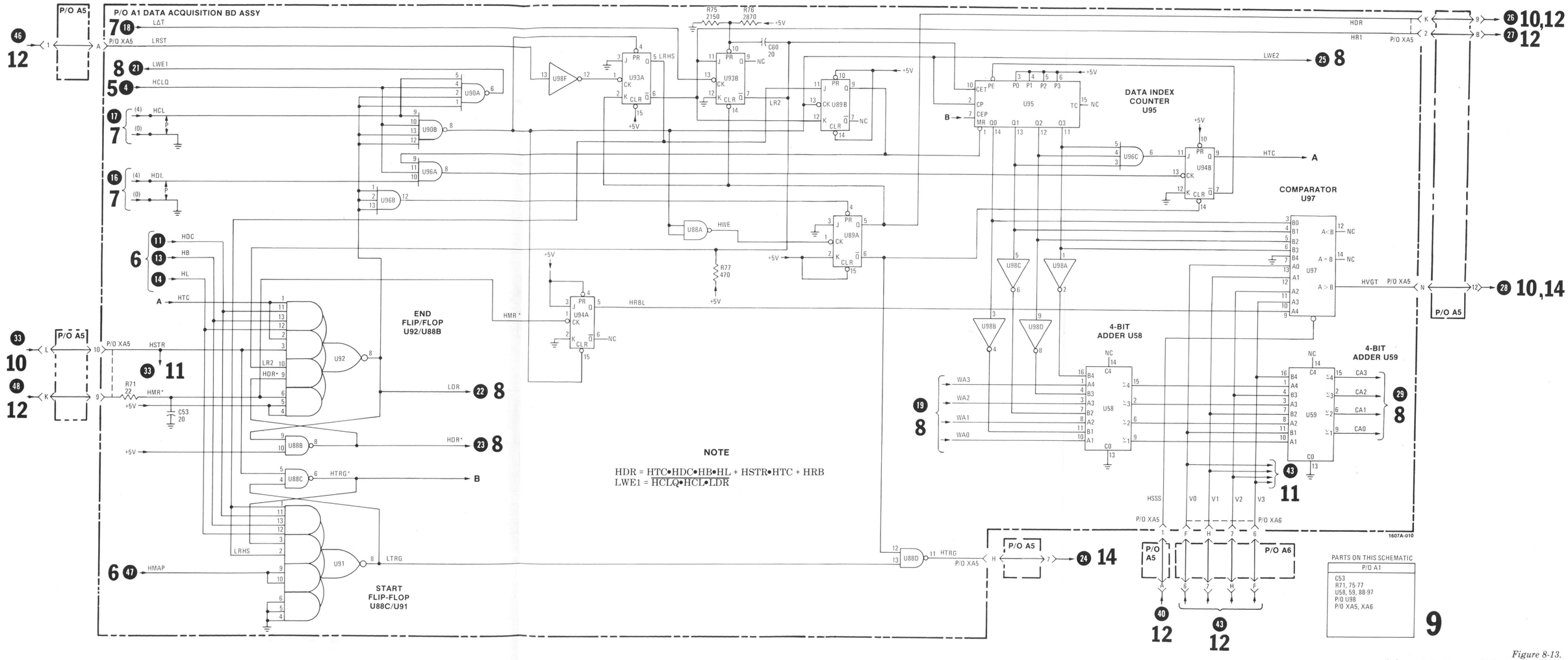
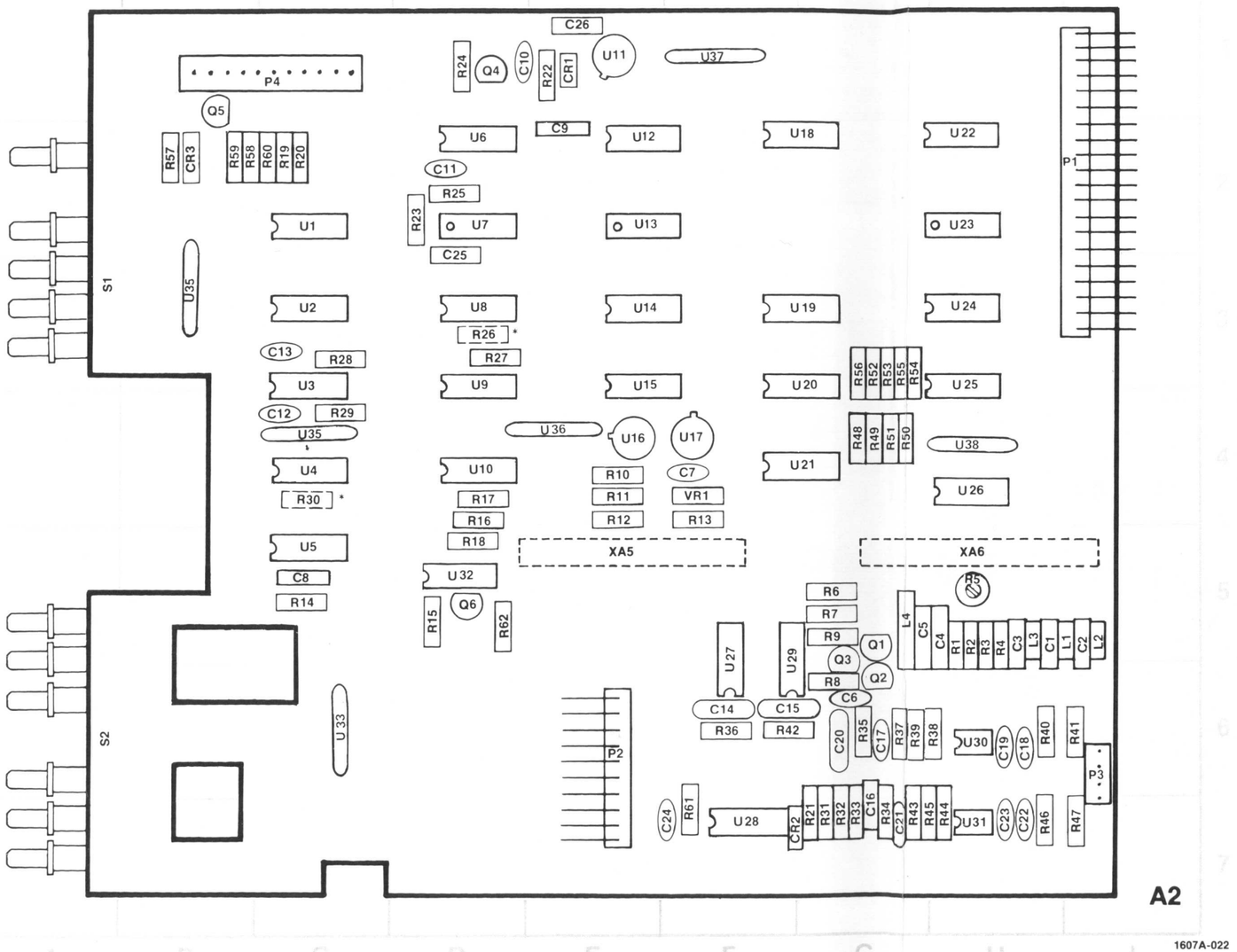



*Figure 8-13.*
*Schematic 9, Memory Index and Control, P/O Assembly A1 (Sheet 2 of 2)*




1607A-022

| REF DESIG | GRID LOC | REF DESIG | GRID LOC | REF DESIG | GRID LOC | REF DESIG | GRID LOC | REF DESIG | GRID LOC |
|---|---|---|---|---|---|---|---|---|---|
| C1 | H-5 | L2 | I-5 | R18 | D-5 | R48 | G-4 | U13 | E-2 |
| C2 | I-5 | L3 | H-5 | R19 | C-2 | R49 | G-4 | U14 | E-3 |
| C3 | H-5 | L4 | G-5 | R20 | C-2 | R50 | G-4 | U15 | E-3 |
| C4 | H-5 | P1 | I-2 | R21 | G-7 | R51 | G-4 | U16 | E-4 |
| C5 | G-5 | P2 | E-6 | R22 | E-1 | R52 | G-3 | U17 | F-4 |
| C6 | G-6 | P3 | I-6 | R23 | D-2 | R53 | C-3 | U18 | G-2 |
| C7 | F-4 | P4 | C-1 | R24 | D-1 | R54 | G-3 | U19 | G-3 |
| C8 | C-5 | Q1 | G-5 | R25 | D-2 | R55 | G-3 | U20 | G-3 |
| C9 | E-2 | Q2 | G-6 | R26* | D-3 | R56 | G-3 | U21 | G-4 |
| C10 | D-1 | Q3 | G-5 | R27 | D-3 | R57 | B-2 | U22 | H-2 |
| C11 | D-2 | Q4 | D-1 | R28 | C-3 | R58 | B-2 | U23 | H-2 |
| C12 | C-4 | Q5 | B-1 | R29 | C-4 | R59 | B-2 | U24 | H-3 |
| C13 | C-3 | Q6 | D-5 | R30* | C-4 | R60 | C-2 | U25 | H-3 |
| C14 | F-6 | R1 | H-5 | R31 | G-7 | R61 | F-7 | U26 | H-4 |
| C15 | F-6 | R2 | H-5 | R32 | G-7 | R62 | D-5 | U27 | F-5 |
| C16 | G-7 | R3 | H-5 | R33 | G-7 | S1 | A-3 | U28 | F-7 |
| C17 | G-6 | R4 | H-5 | R34 | G-7 | S2 | A-6 | U29 | F-5 |
| C18 | H-6 | R5 | H-5 | R35 | G-6 | U1 | C-2 | U30 | H-6 |
| C19 | H-6 | R6 | G-5 | R36 | F-6 | U2 | C-3 | U31 | H-7 |
| C20 | G-6 | R7 | G-5 | R37 | G-6 | U3 | C-3 | U32 | D-5 |
| C21 | G-7 | R8 | G-6 | R38 | H-6 | U4 | C-4 | U33 | C-6 |
| C22 | H-7 | R9 | G-5 | R39 | G-6 | U5 | C-5 | U34 | C-4 |
| C23 | H-7 | R10 | E-4 | R40 | H-6 | U6 | D-2 | U35 | B-3 |
| C24 | F-7 | R11 | E-4 | R41 | I-6 | U7 | D-2 | U36 | E-4 |
| C25 | D-3 | R12 | E-4 | R42 | F-6 | U8 | D-3 | U37 | F-1 |
| C26 | E-1 | R13 | F-4 | R43 | G-7 | U9 | D-3 | U38 | H-4 |
| CR1 | E-1 | R14 | C-5 | R44 | H-7 | U10 | D-4 | VR1 | F-4 |
| CR2 | F-7 | R15 | D-5 | R45 | G-7 | U11 | E-1 | XA5 | E-5 |
| CR3 | B-2 | R16 | D-4 | R46 | H-7 | U12 | E-2 | XA6 | H-5 |
| L1 | H-5 | R17 | D-1 | R47 | I-7 | | | | |

* NOT LOADED AT FACTORY

**NOTE**

See figure 8-7 (Sheet 1 of 2) for Assembly A1 Component Identification.

*Figure 8-14. Schematic 10, Indicator Light Control and Trigger Mode Switches, P/O Assemblies A1 and A2 (Sheet 1 of 2)*

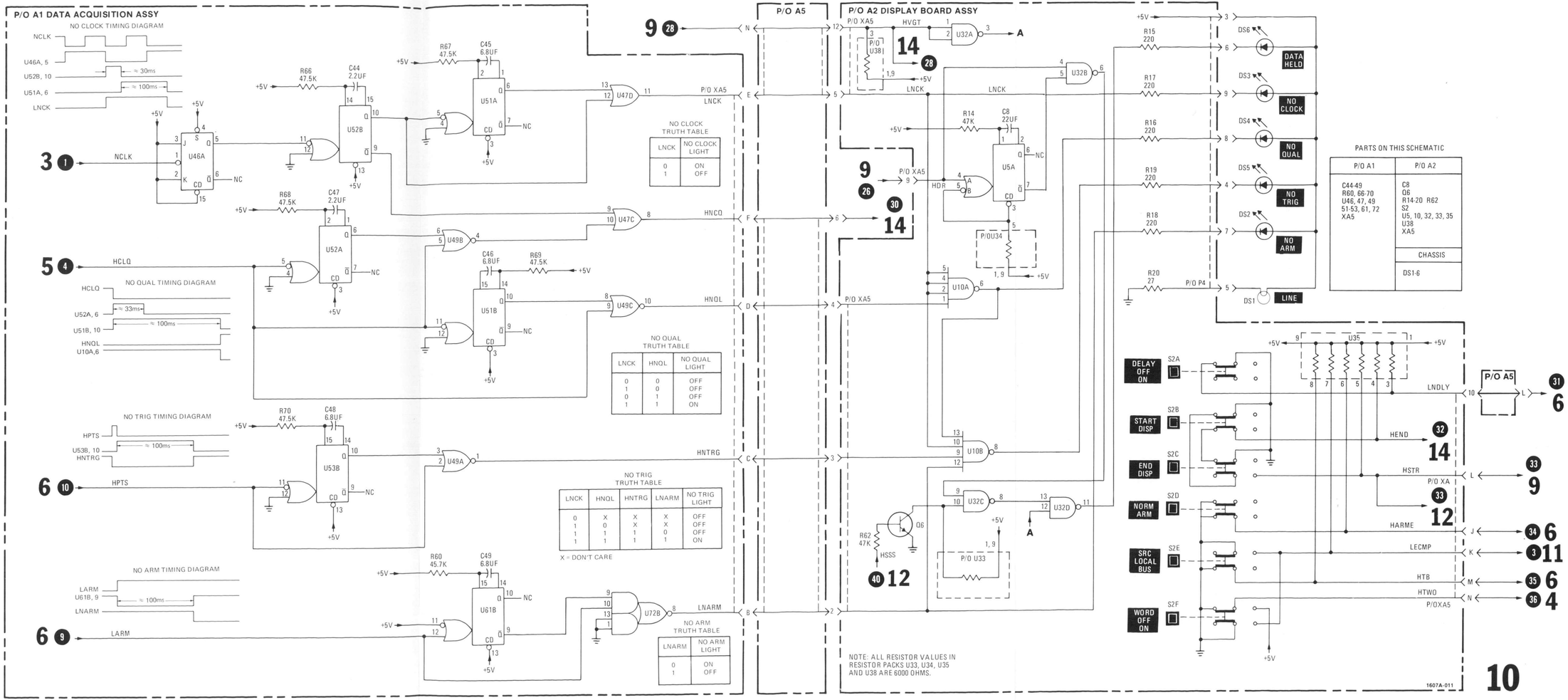



*Figure 8-14.*
*Schematic 10, Indicator Light Control and Trigger Mode Switches, P/O Assemblies A1 and A2 (Sheet 2 of 2)*

TRIGGER WORD INTENSIFY DECODING

| DELAY SETTINGS | TEN'S DECADE 2D3 | 2D2 | 2D1 | 2D0 | UNIT'S DECADE 1D3 | 1D2 | 1D1 | 1D0 | CARRY (A1U79, PIN 14) | MULTIPLEXER U83 OUTPUT CODE Za | Zc | Zd | Zb |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 2 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 3 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 4 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 5 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 6 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 7 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 8 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 9 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 10 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 11 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 12 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 13 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 14 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 15 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 16 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | X | X | X | X |
| 17 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | | | | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | | | | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| | 0 | X | X | X | | | | | | | | | |
| X | X | X | X | X | X | X | X | X | 0 | X | X | X | X |

X = DON'T CARE

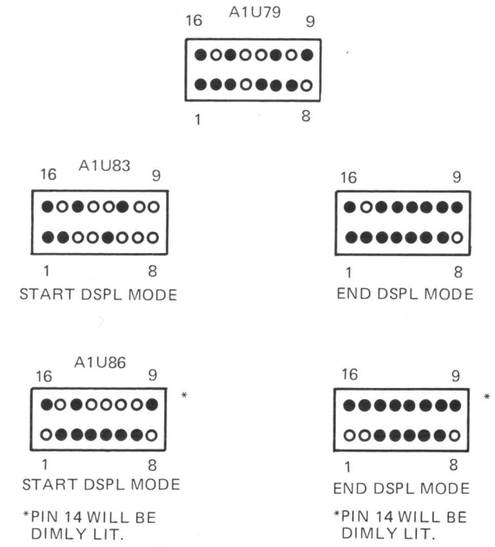


## SCHEMATIC 11 TROUBLESHOOTING

1. Set Model 1607A controls as follows:

| | |
|---|---|
| SAMPLE MODE | SINGLE |
| DISPLAY MODE | START DSPL |
| WORD | ON |
| DELAY | OFF |
| COLUMN BLANKING | FULL CCW |
| LOGIC | POS |
| BYTE | 4 BIT |

2. Monitor A1U79, A1U83 and A1U86, using Model 10528A Logic Clip. The following indications will be observed when the circuit is functioning properly.




LOGIC CLIP INDICATIONS

**NOTE**

See figure 8-7 (Sheet 1 of 2) for Assembly A1 Component Identification.

*Figure 8-15. Schematic 11, Word Intensity, P/O Assembly A1 (Sheet 1 of 2)*

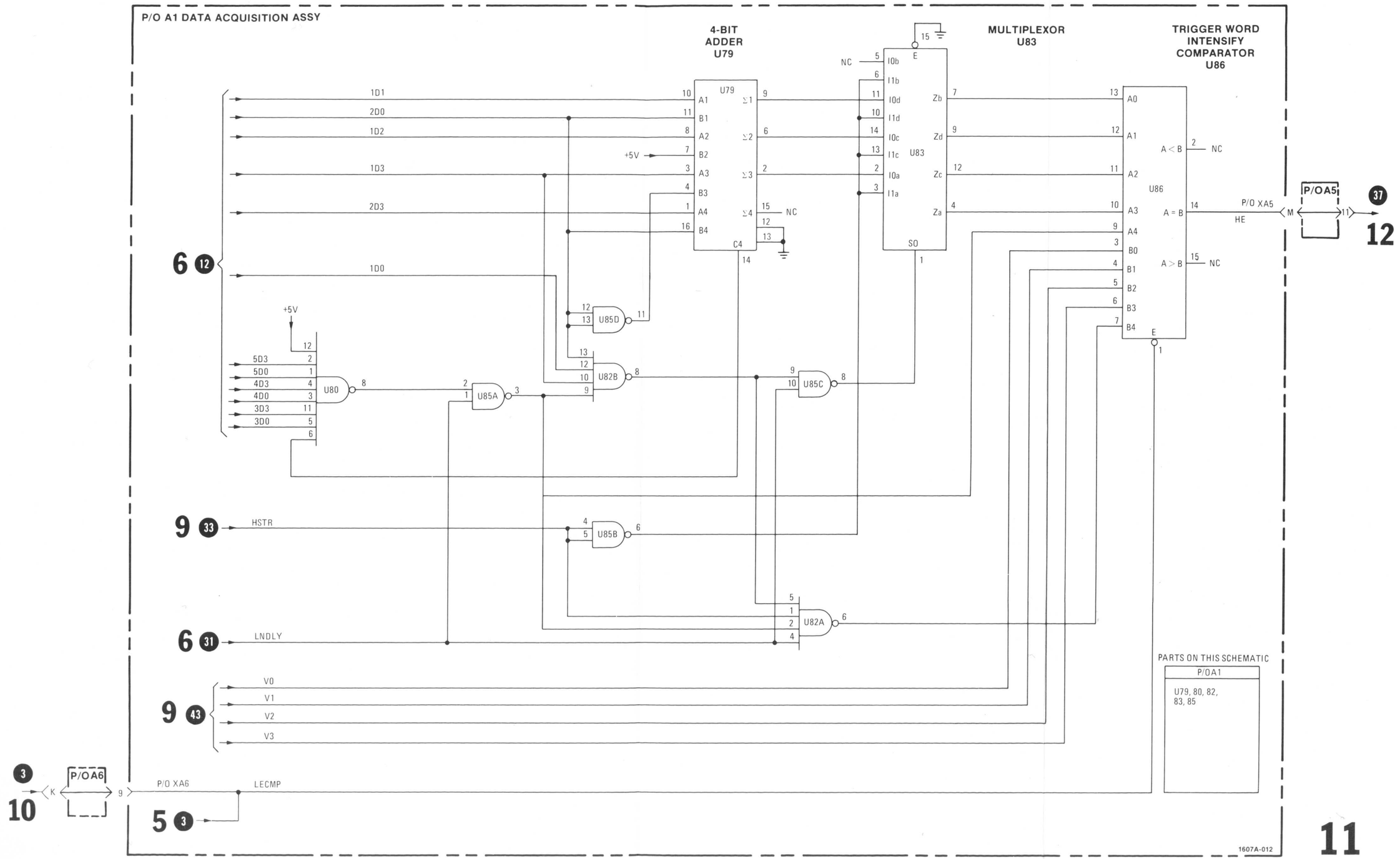



*Figure 8-15.*
*Schematic 11, Word Intensity, P/O Assembly A1 (Sheet 2 of 2)*

LRST LOGIC EQUATIONS

LOCAL MODE

$$LRST = \overline{(HRPR \bullet HRPRB) + HMR}$$

I/O BUS MODE

$$LRST = \overline{(HRPRB \bullet HXRPR \bullet H1600) + (H1600 \bullet HMRXT)^{*} + HMR}$$

*(H1600•HMRXT) is a valid term only in instruments which have modified to accept manual resets from a Model 1600A.

**NOTE**

See figure 8-14 (Sheet 1 of 2) for Assembly A2 Component Identification.

*Figure 8-16. Schematic 12, Display Control and Reset, P/O Assembly A2 (Sheet 1 of 2)*

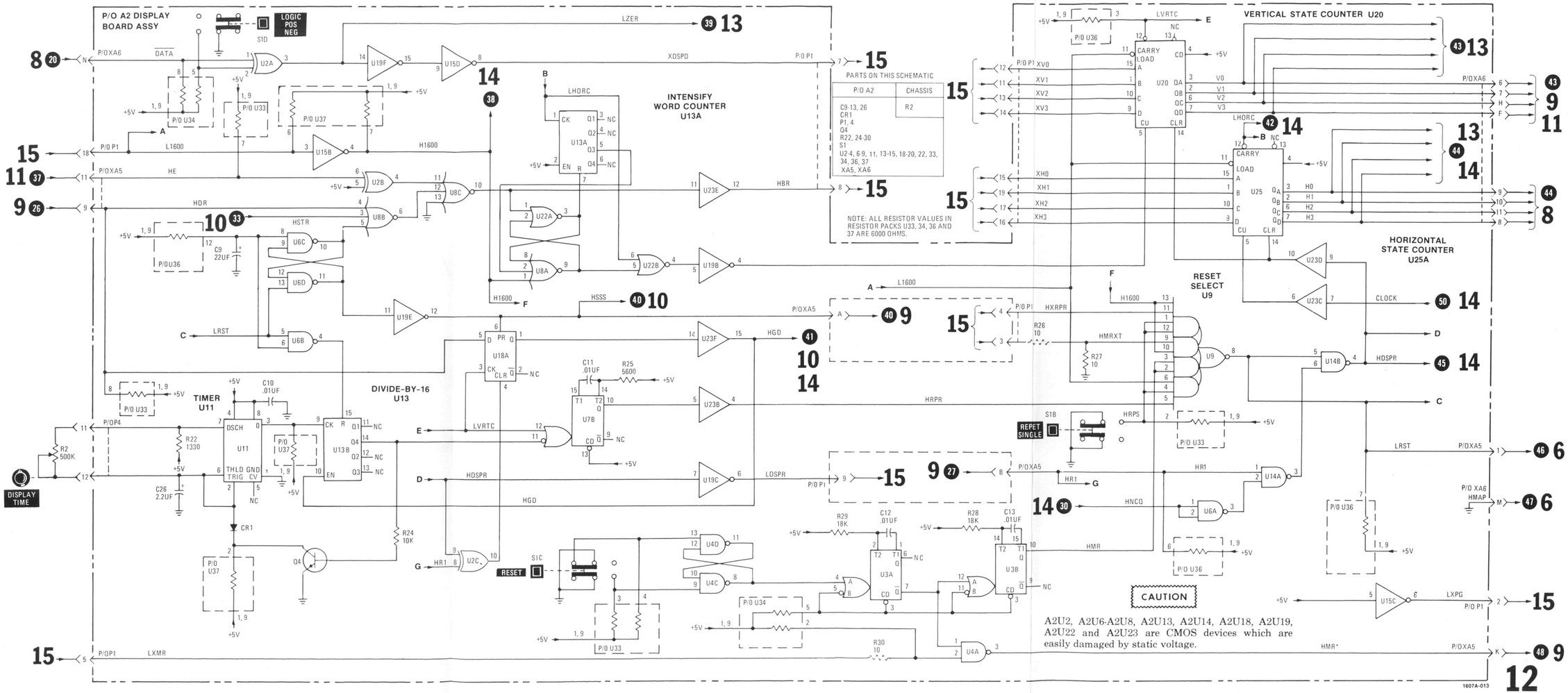



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*Figure 8-16.*
*Schematic 12, Display Control and Reset, P/O Assembly A2 (Sheet 2 of 2)*

## HORIZONTAL AND VERTICAL CODE CONVERTER TRUTH TABLES SCHEMATIC 13

VERTICAL CODE CONVERTER A2U21 TRUTH TABLE

| INPUT | | OUTPUT | | | |
|---|---|---|---|---|---|
| V1 | V0 | ZD | ZC | ZB | ZA |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 |

HORIZONTAL CODE CONVERTER A2U26 TRUTH TABLE

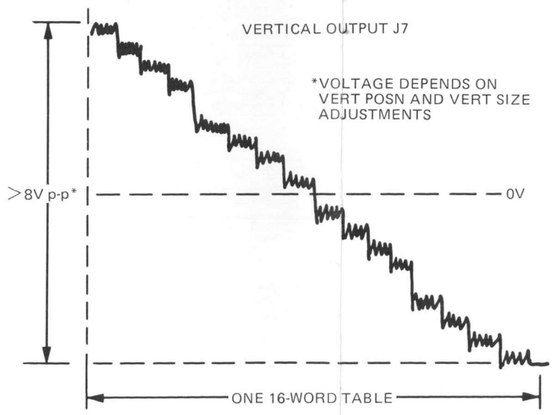
| INPUTS | | | | OUTPUTS (4-BIT BYTES) | | | | OUTPUTS (3-BIT BYTES) | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | B | C | D | Y4 | Y3 | Y2 | Y1 | Y4 | Y3 | Y2 | Y1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |

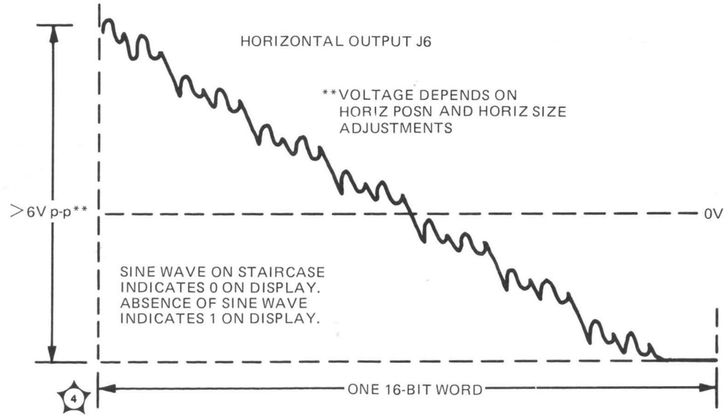
## WAVEFORM MEASUREMENT CONDITIONS SCHEMATIC 13

1. Set Model 1607A controls as follows:

SAMPLE MODE ..... SINGLE
DISPLAY MODE ..... START DSPL
WORD ..... ON
DELAY ..... OFF
COLUMN BLANKING ..... FULL CCW
LOGIC ..... POS
BYTE ..... 4 BIT






**NOTE**

See figure 8-14 (Sheet 1 of 2) for Assembly A2 Component Identification.

*Figure 8-17. Schematic 13, Clock Generator and Analog Output, P/O Assembly A2 (Sheet 1 of 2)*

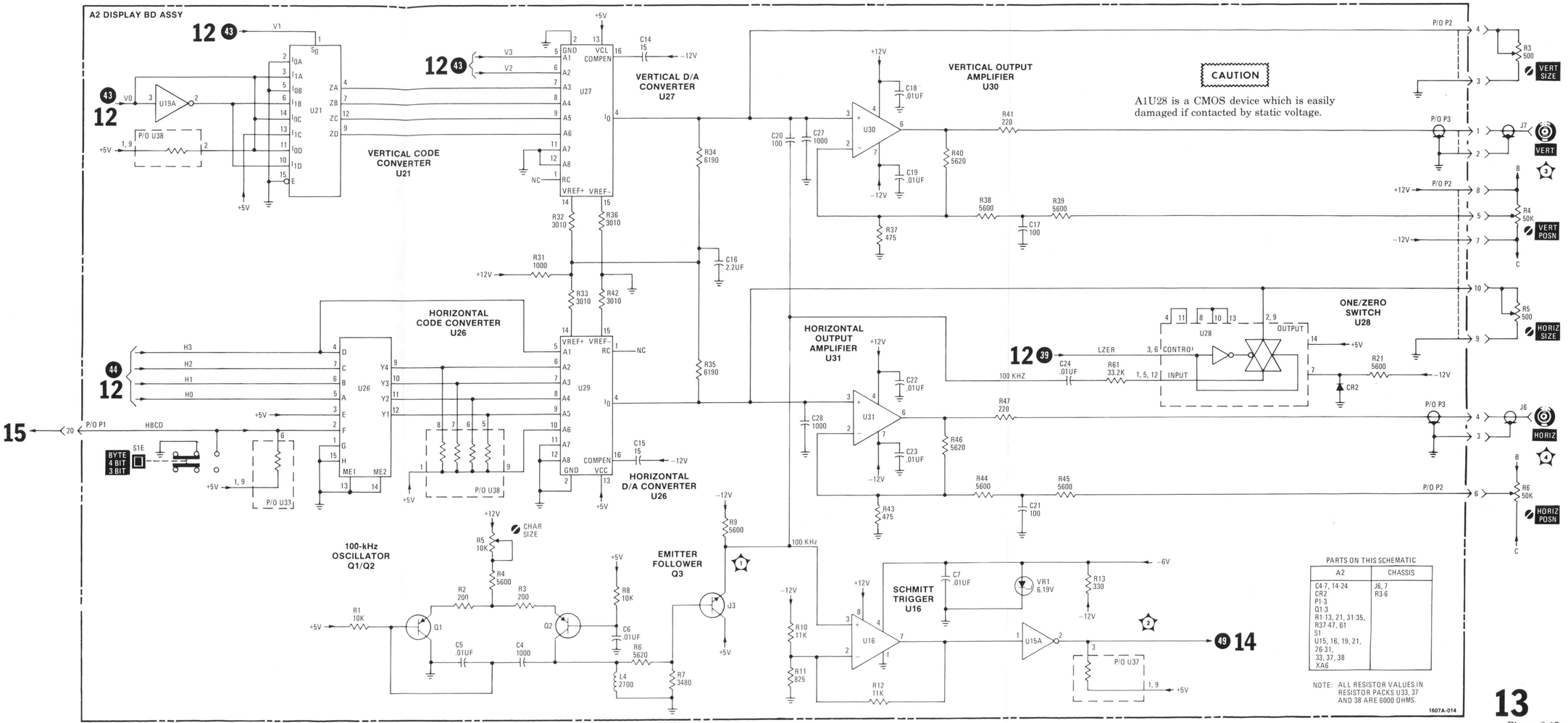



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*Figure 8-17.*
*Schematic 13, Clock Generator and Analog Output, P/O Assembly A2 (Sheet 2 of 2)*

**NOTE**

See figure 8-14 (Sheet 1 of 2) for Assembly A2 Component Identification.

*Figure 8-18. Schematic 14, Blanking, P/O Assembly A2 (Sheet 1 of 2)*

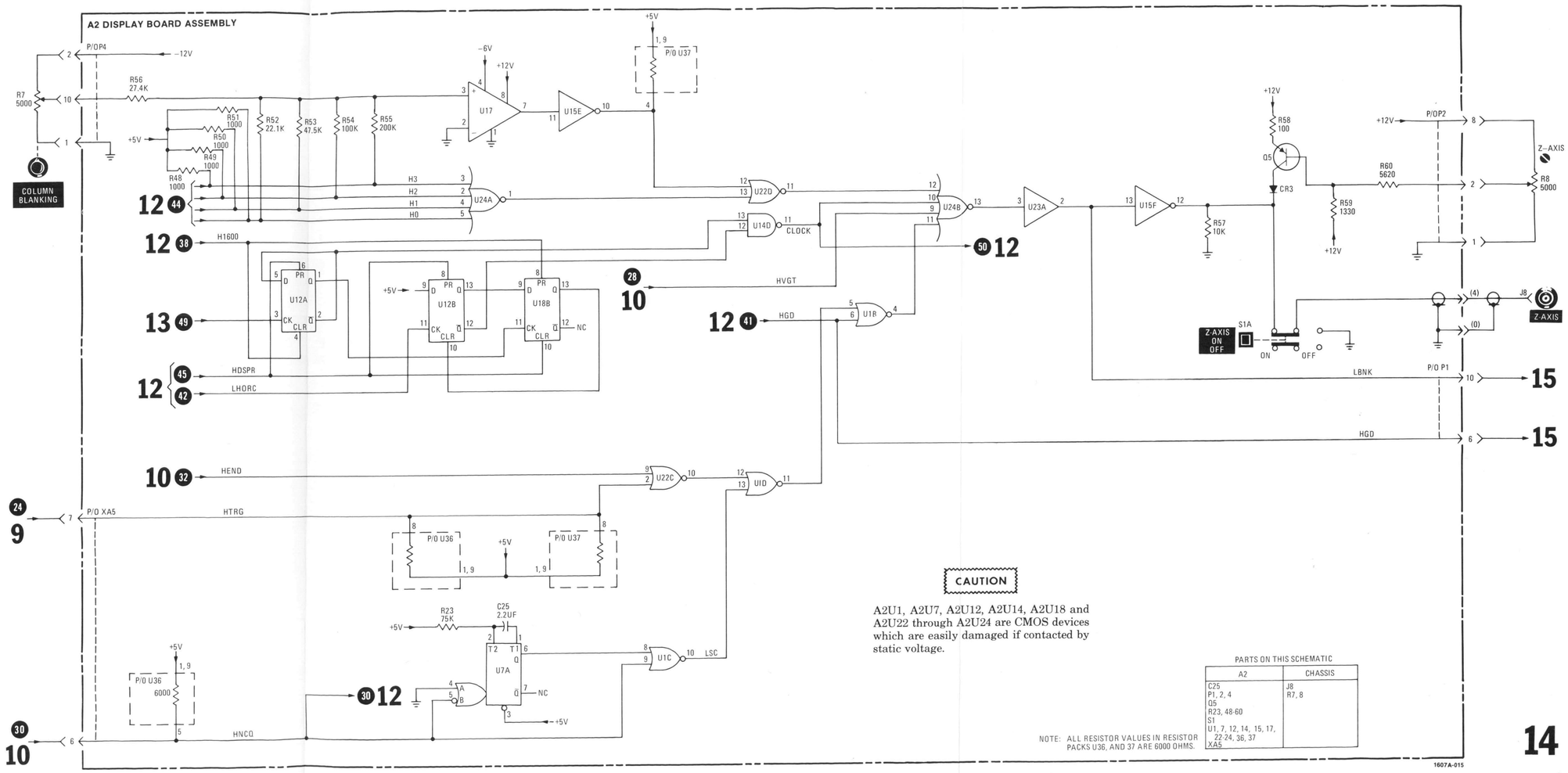



*Figure 8-18.*
*Schematic 14, Blanking, P/O Assembly A2 (Sheet 2 of 2)*

J5 INTERCONNECTION TABLE

| J5 PIN NO. | A2 P1 PIN NO. | SIGNAL |
|---|---|---|
| 6 | 15 | XH0 |
| 7 | 19 | XH1 |
| 8 | 17 | XH2 |
| 9 | 16 | XH3 |
| 10 | 12 | XV0 |
| 11 | 11 | XV1 |
| 12 | 13 | XV2 |
| 13 | 14 | XV3 |
| 14 | 7 | XDSPD |
| 15 | 6 | HGD |
| 16 | 5 | LXMR |
| 17 | 4 | HXRPR |
| 18 | 3 | HMRXT |
| 19 | 8 | HBR |
| 20 | 9 | LDSPR |
| 21 | 10 | LBNK |
| 22 | 20 | HBCD |
| 24 | 2 | LXPG1 |
| 25 | 2 | LXPG2 |
| 35 | 18 | L1600 |
| 36 | 1 | GND |

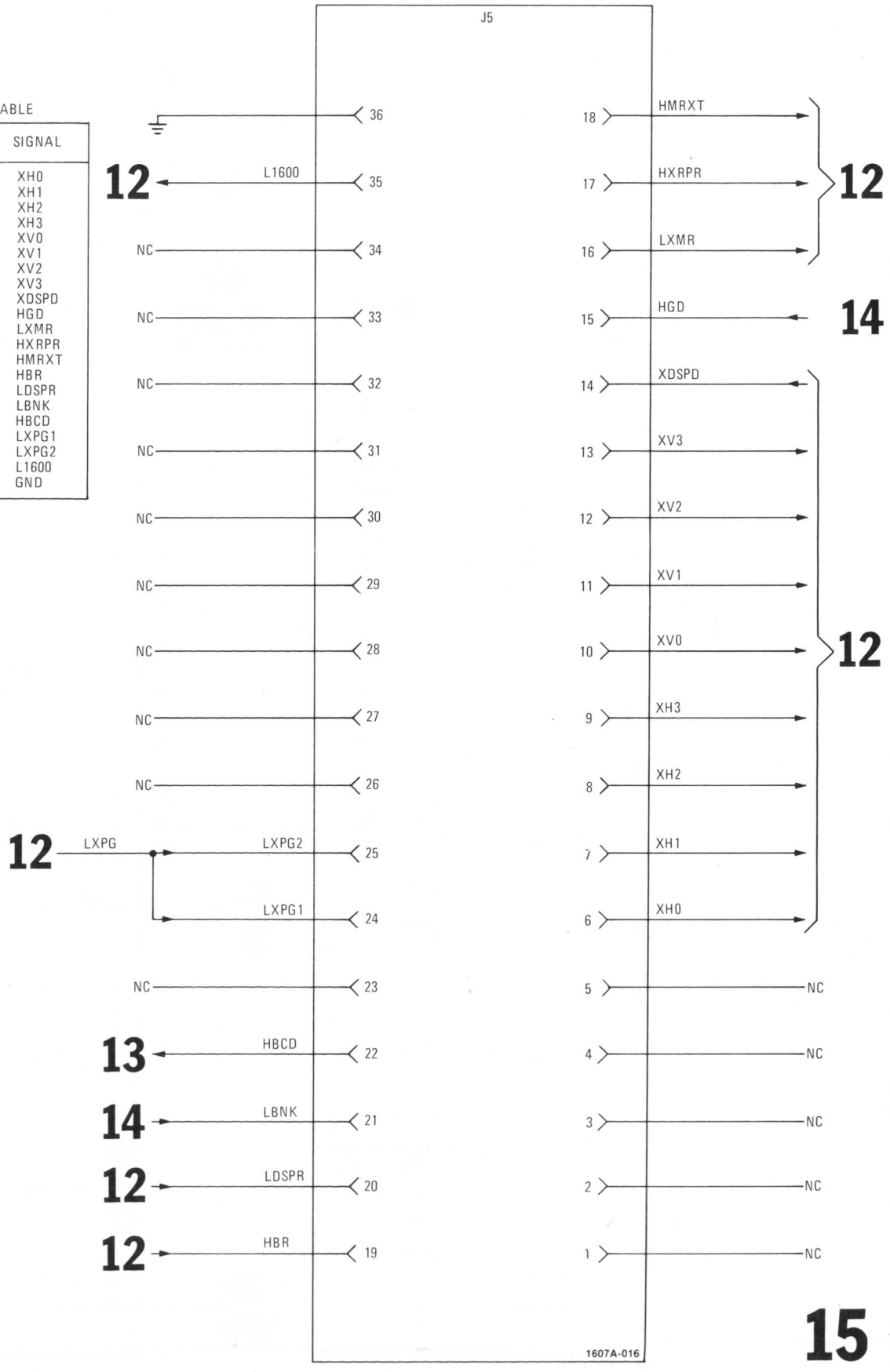
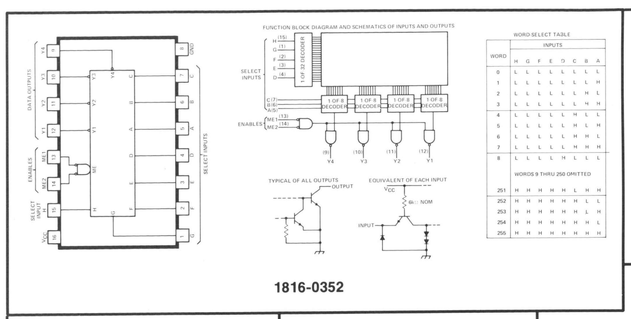



*Figure 8-19. Schematic 15, I/O Port J5*

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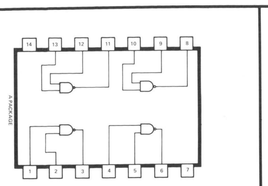

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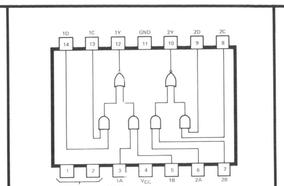


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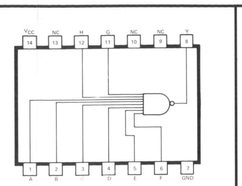

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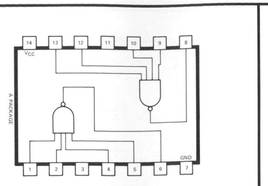

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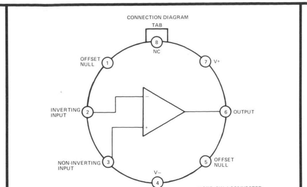


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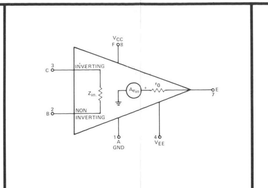


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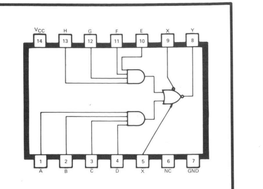

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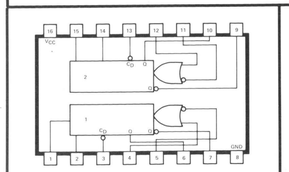

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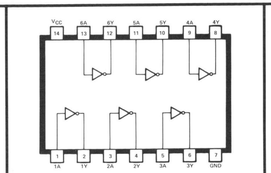

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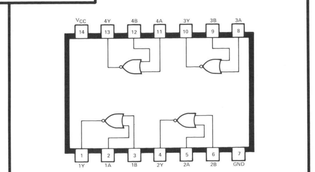

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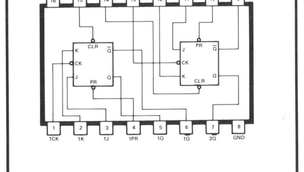

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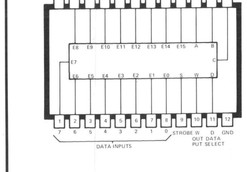


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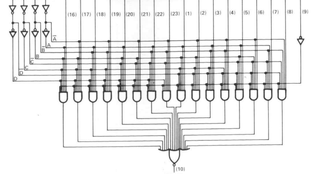


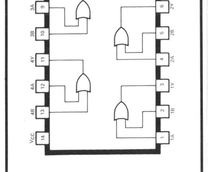

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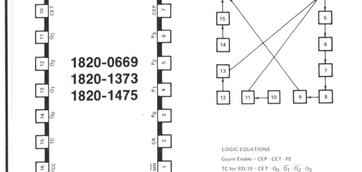


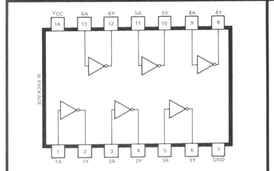

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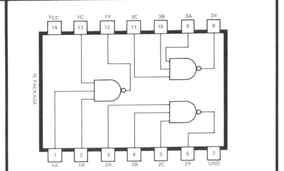

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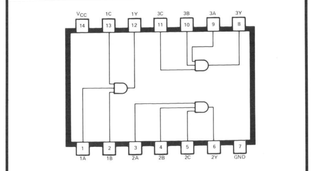

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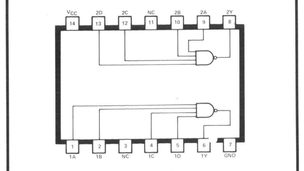

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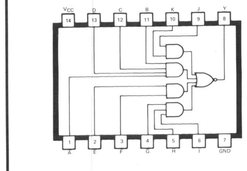

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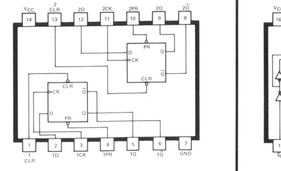

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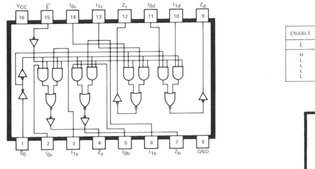

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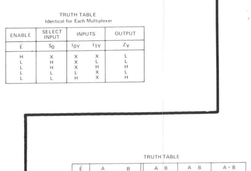
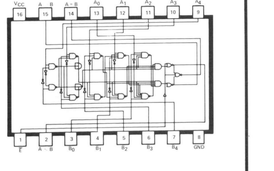
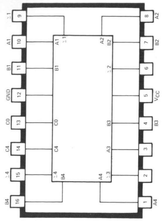


1820-0904

1607A-028

*Figure 8-20.*
*Integrated Circuit (IC) Identification (Sheet 1 of 2)*



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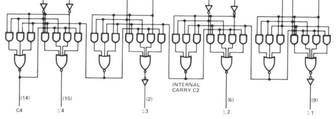
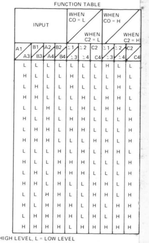
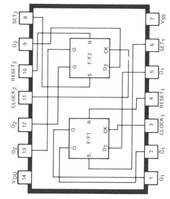




H = HIGH LEVEL, L = LOW LEVEL

NOTE: INPUT CONDITIONS AT A3, A2, B2, AND C0 ARE USED TO DETERMINE OUTPUTS ↑1 AND ↑2 AND THE VALUE OF THE INTERNAL CARRY C2. THE VALUES AT C2, A3, B3, A4, AND B4 ARE THEN USED TO DETERMINE OUTPUTS ↑3, ↑4, AND C4.



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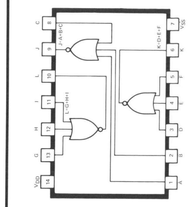

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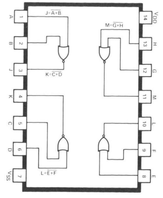

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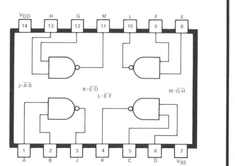

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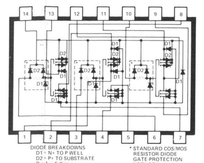
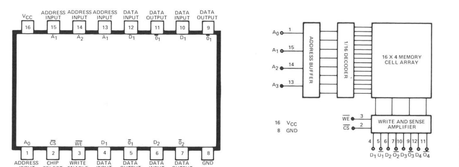


DIODE BRI (ACCIONO)
D1 - N+ TO P WELL
D2 - P+ TO SUBSTRATE
R = 1 - 5 K Ω

STANDARD CONNON RESISTOR DIODE GATE PROTECTION NETWORK

1820-0978



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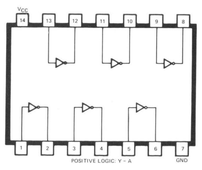
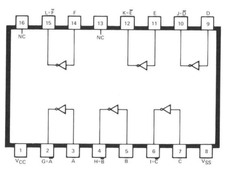


POSITIVE LOGIC: Y = A

1820-1139



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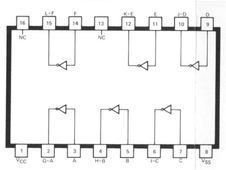

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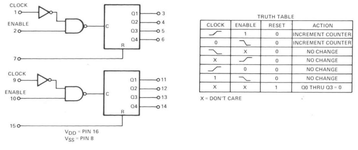
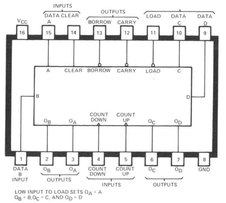


TRUTH TABLE

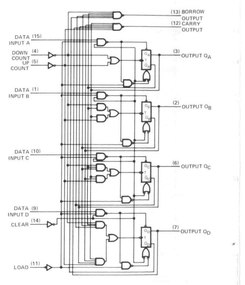
| CLOCK | ENABLE | RESET | ACTION |
|---|---|---|---|
| ↑ | L | 0 | INCREMENT COUNTER |
| 0 | ↑ | 0 | INCREMENT COUNTER |
| ↑ | X | 0 | NO CHANGE |
| X | ↓ | 0 | NO CHANGE |
| ↓ | 0 | 0 | NO CHANGE |
| 1 | ↓ | 0 | NO CHANGE |
| X | X | 1 | Q0 THRU Q3 = 0 |

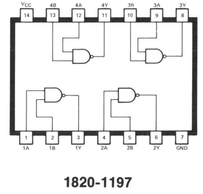
X = DON'T CARE



LOW INPUT TO LOAD SETS $Q_A$ - $Q_D$ = D

1820-1194





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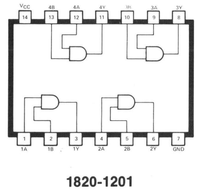

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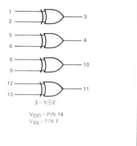
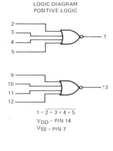


3 = 1◻2

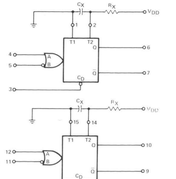
1820-1330



LOGIC DIAGRAM
POSITIVE LOGIC

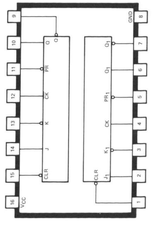
1 = 2 • 3 • 4 • 5

1820-1339



$R_X$ AND $C_X$ ARE EXTERNAL COMPONENTS.

1820-1356



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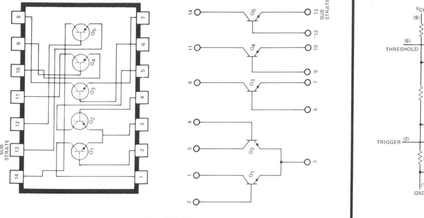

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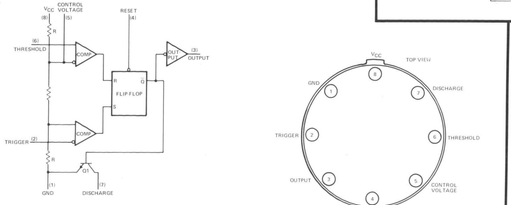

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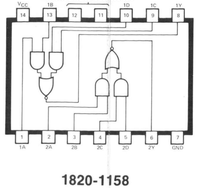

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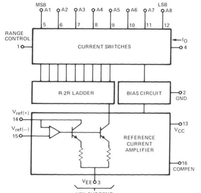

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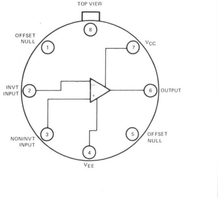

1826-0254

1607A-067

*Figure 8-20. Integrated Circuit (IC) Identification (Sheet 2 of 2)*

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TWX: 710-795-3124

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**King of Prussia** 19406
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TWX: 510-660-2670

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11748 Kingsway Ave.
**Edmonton** T5G 0X5
Tel: (403) 452-3670
TWX: 610-831-2431

Hewlett-Packard (Canada) Ltd.
915-42 Avenue S.E. Suite 102
**Calgary** T2G 1Z1
Tel: (403) 287-1672

**BRITISH COLUMBIA**
Hewlett-Packard (Canada) Ltd.
837 E. Cordova Street
**Vancouver** V6A 3R2
Tel: (604) 254-0531
TWX: 610-922-5059

**MANITOBA**
Hewlett-Packard (Canada) Ltd.
513 Century St.
St. James
**Winnipeg** R3H 0L8
Tel: (204) 786-7581
TWX: 610-671-3531

**NOVA SCOTIA**
Hewlett-Packard (Canada) Ltd.
800 Windmill Road
**Dartmouth** B3C 1L1
Tel: (902) 469-7820

**ONTARIO**
Hewlett-Packard (Canada) Ltd.
1785 Woodward Dr.
**Ottawa** K2C 0P9
Tel: (613) 225-6530
TWX: 610-562-8968

Hewlett-Packard (Canada) Ltd.
6877 Goreway Drive
**Mississauga** L4V 1L9
Tel: (416) 678-9430
TWX: 610-492-4246

**QUEBEC**
Hewlett-Packard (Canada) Ltd.
275 Hymus Blvd.
**Pointe Claire** H9R 1G7
Tel: (514) 697-4232
TWX: 610-422-3022
TLX: 05-821521 HPCL

Hewlett-Packard (Canada) Ltd.
2376 Galvani Street
**Ste-Foy** G1N 4G4
Tel: (418) 688-8710

**FOR CANADIAN AREAS NOT LISTED:**
Contact Hewlett-Packard (Canada) Ltd. in Mississauga.

## CENTRAL AND SOUTH AMERICA

**ARGENTINA**
Hewlett-Packard Argentina S.A.C.e.I.
Lavalle 1171-3° Piso
**Buenos Aires**
Tel: 35-0436, 35-0627, 35-0341
Telex: 012-1009
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**BOLIVIA**
Stambuk & Mark (Bolivia) Ltda.
Av. Mariscal Santa Cruz 1342
**La Paz**
Tel: 40626, 53163, 52421
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Cable: BUKMAR

**BRAZIL**
Hewlett-Packard Do Brasil I.E.C. Ltda.
Rua Frei Caneca, 1.152-Bela Vista
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Praca Dom Feliciano, 78-8° andar (Sala 806/8)
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Hewlett-Packard Do Brasil I.E.C. Ltda.
Rua Siqueira Campos, 53, 4° andar Copacabana
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Instrumentación
Henrik A. Langebaek & Kier S.A.
Carrera 7 No. 48-59
Apartado Aéreo 6287
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Cable: AARIS Bogota
Telex: 44400INSTCO

**COSTA RICA**
Cientifica Costarricense S.A.
Apartado 10159
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GB-**Altrincham**, Cheshire
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Telex: 668068

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S.A./N.V.
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Telex: 13 216 hepa nl

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Telex: 16621 hpnas n

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Warsaw Technical Office
Szpitalna 1
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Telex: 812453

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Equipamentos Eléctricos S.a.r.l.
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P.O. Box 2531
P-**Lisbon** 1
Tel: (19) 68 60 72
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P.O. Box 2761
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Tel: (1) 458 26 00 (10 lines)
Telex: 23515 hpe

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Milanesado 21-23
E-**Barcelona** 17
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E-**Seville**
Tel: 64 44 54/58

Hewlett-Packard Española S.A.
Edificio Albia II 7° B
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Alvaro Bazen, 12
(Edificio Luz)
E - **Valencia** - 10
Tel: 60 42 00

**SWEDEN**
Hewlett-Packard Sverige AB
Enighetsvägen 1-3
Fack
S-161 20 **Bromma** 20
Tel: (08) 730 05 50
Cable: MEASUREMENTS
Stockholm
Telex: 10721

Hewlett-Packard Sverige AB
Hagakersgatan 9C
S-431 41 **Moindal**
Tel: (031) 27 68 00/01
Telex: Via Bromma

**SWITZERLAND**
Hllett-Packard (Schweiz) AG
Zurcherstrasse 20
P.O. Box 64
CH-8952 Schlieren **Zurich**
Tel: (01) 98 18 21
Cable: HPAG CH
Telex: 53933 hpag

Hewlett-Packard (Schweiz) AG
9, chemin Louis-Pictet
CH-1214 Vernier-**Geneva**
Tel: (022) 41 49 50
Cable: HEWPACKSA Geneva
Telex: 27 333 hpsa ch

**TURKEY**
Telekom Engineering Bureau
Saglik Sok. No. 15/1
Ayaspasa-Beyoglu
P.O. Box 437 Beyoglu
TR-**Istanbul**
Tel: 49 40 40
Cable: TELEMATION Istanbul

**UNITED KINGDOM**
Hewlett-Packard Ltd.
King Street Lane
Winnersh, Wokingham
GB-**Berkshire** RG11 5AR
Tel: Wokingham 784774
Telex: 847178/848179

Hewlett-Packard Ltd.
"The Graftons"
Stamford New Road
GB-**Altrincham**, Cheshire
Tel: (061) 928-9021
Telex: 668068

Hewlett-Packard Ltd.
c/o Makro
South Service Wholesale Centre
Amber Way
Halesowen Industrial Estate
GB-**Halesowen**, Worcs
Tel: Birmingham 7860

Hewlett-Packard Ltd.
4th Floor
Wedge House
799, London Road
GB-**Thornton Heath** CR4 6XL,
Surrey
Tel: (01) 684 0105
Telex: 946825

Hewlett-Packard Ltd.
c/o Makro
South Service Wholesale Centre
Wear Industrial Estate
Washington
GB-**New Town**, County Durham
Tel: Washington 464001 ext. 57/58

Hewlett-Packard Ltd.'s registered
address for V.A.T. purposes
only:
70, Finsbury Pavement
**London**, EC2A1SX
Registered No. 690597

**USSR**
Hewlett-Packard USSR
c/o Commercial Office
American Embassy (Box M)
A-1091 **Vienna**, Austria
Tel: 221-79-71
Telex: 7825 hewpak SU

**YUGOSLAVIA**
Iskra-Standard/Hewlett-Packard
Topniska 58/3
61000 **Ljubljana**
Tel: 315-879/321-674
Telex: 31300

**SOCIALIST COUNTRIES PLEASE CONTACT:**
Hewlett-Packard S.A.
7, rue du Bois-du-Lan
P.O. Box 349
CH-1217 Meyrin 1 **Geneva**
Switzerland
Tel: (022) 41 54 00
Cable: HEWPACKSA Geneva
Telex: 2 24 86

# AFRICA, ASIA, AUSTRALIA

**ANGOLA**
Telectra
Empresa Técnica de
Equipamentos
Eléctricos, S.A.R.L.
R. Barbosa Rodrigues, 42-1°DT.°
Caixa Postal, 6487-**Luanda**
Tel: 35515/6
Cable: TELECTRA Luanda

**AUSTRALIA**
Hewlett-Packard Australia
Pty. Ltd.
31-41 Joseph Street
**Blackburn**, Victoria 3130
Tel: 89-6351, 89-6306
Telex: 31-024
Cable: HEWPARD Melbourne

Hewlett-Packard Australia
Pty. Ltd.
31 Bridge Street
**Pymble**,
New South Wales, 2073
Tel: 449-6566
Telex: 21561
Cable: HEWPARD Sydney

Hewlett-Packard Australia
Pty. Ltd.
97 Churchill Road
**Prospect** 5082
South Australia
Tel: 44 8151
Cable: HEWPARD Adelaide

Hewlett-Packard Australia
Pty. Ltd.
141 Stirling Highway
**Claremont**, W.A. 6010
Tel: 86-5455
Telex: 93859
Cable: HEWPARD

Hewlett-Packard Australia
Pty. Ltd.
121 Wollongong Street
**Fyshwick**, A.C.T., 2609
Tel: 95 3733

Hewlett-Packard Australia
Pty. Ltd.
5th Floor
Teachers Union Building
495-499 Boundary Street
**Spring Hill**, 4000 Queensland
Tel: 29-1544
Telex: AA-42133

**CEYLON**
United Electricals Ltd.
P.O. Box 681
60, Park St.
**Colombo** 2
Tel: 26696
Cable: HOTPOINT Colombo

**CYPRUS**
Kypronics
19 Gregorios & Xenopoulos Rd.
P.O. Box 1152
CY-**Nicosia**
Tel: 45628 29
Cable: KYPRONICS PANDEHIS

**HONG KONG**
Schmidt & Co.(Hong Kong) Ltd.
P.O. Box 297
Connalight Centre
39th Floor
Connaught Road, Central
**Hong Kong**
Tel: 240168, 232735
Telex: HX4766
Cable: SCHMIDTCO Hong Kong

**INDIA**
Blue Star Ltd.
Kasturi Buildings
Jamshedji Tata Rd.
**Bombay** 400 020
Tel: 29 50 21
Telex: 3751
Cable: BLUEFROST

Blue Star Ltd.
Sahas
414/2 Vir Savarkar Marg
Prabhadevi
**Bombay** 400 025
Tel: 45 78 87
Telex: 4093
Cable: FROSTBLUE

Blue Star Ltd.
Band Box House
Prabhadevi
**Bombay** 400 025
Tel: 45 73 01
Telex: 3751
Cable: BLUESTAR

Blue Star Ltd.
14/40 Civil Lines
**Kampur** 208 001
Tel: 6 88 82
Cable: BLUESTAR

Blue Star Ltd.
7 Hare Street
P.O. Box 506
**Calcutta** 700 001
Tel: 23-0131
Telex: 655
Cable: BLUESTAR

Blue Star Ltd.
Blue Star House
34 Ring Road
Lajpat Nagar
**New Delhi** 110 024
Tel: 62 32 76
Telex: 2463
Cable: BLUESTAR

Blue Star Ltd.
Blue Star House
11 11A Magarath Road
**Bangalore** 560 025
Tel: 55668
Telex: 430
Cable: BLUESTAR

Blue Star Ltd.
Meeakshi Mandiran
xxx 1678 Mahatma Gandhi Rd.
**Cochin** 682 016 Kerala

Blue Star Ltd.
1-1-117/1
Sarojini Devi Road
**Secunderabad** 500 003
Tel: 7 63 91, 7 73 93
Cable: BLUEFROST
Telex: 459

Blue Star Ltd.
23 24 Second Line Beach
**Madras** 600 001
Tel: 23954
Telex: 379
Cable: BLUESTAR

Blue Star Ltd.
Nathraj Mansions
2nd Floor Bistupur
**Jamshedpur** 831 001
Tel: 38 04
Cable: BLUESTAR
Telex: 240

**INDONESIA**
BERCA Indonesia P.T.
P.O. Box 496
1st Floor JL. Cikini Raya 61
**Jakarta**
Tel: 56038, 40369, 49886
Telex: 2895 Jakarta

**IRAN**
Multi Corp International Ltd.
Avenue Soraya 130
P.O. Box 1212
IR-**Teheran**
Tel: 83 10 35-39
Cable: MULTICORP Tehran
Telex: 2893 mci tn

**ISRAEL**
Electronics & Engineering
Div. of Motorola Israel Ltd.
17 Aminadav Street
**Tel-Aviv**
Tel: 36941 (3 lines)
Cable: BASTEL Tel-Aviv
Telex: 33569

**JAPAN**
Yokogawa-Hewlett-Packard Ltd.
Ohashi Building
1-59-1 Yoyogi
Shibuya-ku, **Tokyo**
Tel: 03-370-2281/92
Telex: 232-2024YHP
Cable: YHPMARKET TOK 23-724

Yokogawa-Hewlett-Packard Ltd.
Nisei Ibaragi Bldg.
2-2-8 Kasuga
Ibaragi-Shi
**Osaka**
Tel: (0726) 23-1641
Telex: 5332-385 YHP OSAKA

Yokogawa-Hewlett-Packard Ltd.
Nakamo Building
No. 24 Kamisasazima-cho
Nakamura-ku, **Nagoya** City
Tel: (052) 571-5171

Yokogawa-Hewlett-Packard Ltd.
Tanigawa Building
2-24-1 Tsuruya-cho
Kanagawa-ku
**Yokohama**, 221
Tel: 045-312-1252
Telex: 382-3204 YHP YOK

Yokogawa-Hewlett-Packard Ltd.
Mito Mitsui Building
1-4-73 San-no-maru
**Mito**, 310
Tel: 0292-25-7470

Yokogawa-Hewlett-Packard Ltd.
Inoue Building
1348-3, Asahi-cho, 1-chome
**Atsugi**, 243
Tel: 0462-24-0452

**KENYA**
Technical Engineering Services
P.O. Box 18311
**Nairobi**, Kenya
Tel: 57726
Cable: PROTON

**KOREA**
American Trading Company
Korea
I.P.O. Box 1103
Dae Kyung Bldg., 8th Floor
107 Sejong-Ro,
Chongro-Ku, **Seoul**
Tel: (4 lines) 73-8924-7
Cable: AMTRACO Seoul

**KUWAIT**
Al-Khaldiya Trading &
Contracting Co.
Al Soor Street
Michaan Bldg. No. 4
**Kuwait**
Tel: 42 99 10
Cable: VISCOUNT

**LEBANON**
Constantin E. Macridis
Clemenceau Street 34
P.O. Box 7213
RL-**Beirut**
Tel: 220846
Telex: 21114 Leb
Cable: ELECTRONUCLEAR Beirut

**MALAYSIA**
MECOMB Malaysia Ltd.
2 Lorong 13/6A
Section 13
Petaling Jaya, **Selangor**
Cable: MECOMB Kuala Lumpur

**MOZAMBIQUE**
A.N. Goncalves, Lta.
162, 1° Apt. 14 Av. D. Luis
Caixa Postal 107
**Lourenco Marques**
Tel: 27091, 27114
Telex: 6-203 Negon Mo
Cable: NEGON

**NEW ZEALAND**
Hewlett-Packard (N.Z.) Ltd.
94-96 Dixon Street
P.O. Box 9443
Courtenay Place,
**Wellington**
Tel: 59-559
Telex: 3898
Cable: HEWPACK Wellington

Hewlett-Packard (N.Z.) Ltd.
Pakuranga Professional Centre
267 Pakuranga Highway
Box 51092
**Pakuranga**
Tel: 569-651
Cable: HEWPACK, Auckland

Analytical/Medical Only
Dental & Medical Supply Co. Ltd.
Scientific Division
79 Carlton Gore Road
Newmarket
P.O. Box 1234
**Auckland**
Tel: 75-289
Cable: DENTAL Auckland

**NIGERIA**
The Electronics
Instrumentatiofns Ltd.
N6B 770 Oyo Road
Oluseun House
P.M.B. 5402
**Ibadan**
Tel: 22325
Cable: THETEIL Ibadan

The Electronics Instrumenta-
tions Ltd. (TEIL)
16th Floor Cocoa House
P.M.B. 5402
**Ibadan**
Tel: 22325
Cable: THETEIL Ibadan

**PAKISTAN**
Mushko & Company, Ltd.
Oosman Chambers
Abdullah Haroon Road
**Karachi** 3
Tel: 511027, 512927
Cable: COOPERATOR Karachi

Mushko & Company, Ltd.
38B, Satellite Town
**Rawalpindi**
Tel: 41924
Cable: FEMUS Rawalpindi

**PHILIPPINES**
Electromex, Inc.
6th Floor, Amalgamated
Development Corp. Bldg.
Ayala Avenue, Makati, Rizal
C.C.P.O. Box 1028
**Makati**, Rizal
Tel: 86-18-87, 87-76-77,
Cable: ELEMEX Manila

**SINGAPORE**
Mechanical & Combustion
Engineering Company Pte.
Ltd.
10/12, Jalan Kilang
Red Hill Industrial Estate
**Singapore**, 3
Tel: 647151 (7 lines)
Cable: MECOMB Singapore

Hewlett-Packard Singapore
(Pte.) Ltd.
Blk. 2, 6th FLOOR, Jalan
Bukit Merah
Redhill Industrial Estate
Alexandra P.O. Box 87,
**Singapore** 3
Tel: 633022
Telex: HPSG RS 21486
Cable: HEWPACK, Singapore

**SOUTH AFRICA**
Hewlett-Packard South Africa
(Pty.), Ltd.
Hewlett-Packard House
Daphne Street, Wendywood
**Sandton**, Transvaal 2001
Tel: 802-1040
Telex: SA43-4782JH
Cable: HEWPACK

Hewlett-Packard South Africa
(Pty.), Ltd.
Breecastle House
Bree Street
**Cape Town**
Tel: 2-6941 2/3
Cable: HEWPACK Cape Town
Telex: 0006 CT

Hewlett-Packard South Africa
(Pty.), Ltd.
641 Ridge Road, Durban
P.O. Box 37099
**Overport**, Durban, 4067
Tel: 88-6102
Telex: 6-7954

**TAIWAN**
Hewlett-Packard Taiwan
39 Chung Shiao West Road
Sec. 1 Overseas Insurance
Corp. Bldg. 7th Floor
**Taipei**
Tel: 389160,1,2,
Telex: TP824 HEWPACK
Cable: HEWPACK Taipei

Hewlett-Packard Taiwan
38, Po-Ai Lane, San Min Chu,
**Kaohsiung**
Tel: 297319

**THAILAND**
UNIMESA Co., Ltd.
Elsom Research Building
Bangjak Sukumvit Ave.
**Bangkok**
Tel: 932387, 930338
Cable: UNIMESA Bangkok

**UGANDA**
Uganda Tele-Electric Co., Ltd.
P.O. Box 4449
**Kampala**
Tel: 57279
Cable: COMCO Kampala

**VIETNAM**
Peninsular Trading Inc.
P.O. Box H-3
216 Hien-Vuong
**Saigon**
Tel: 20-805, 93398
Cable: PENTRA, SAIGON 242

**ZAMBIA**
R.J. Tilbury (Zambia) Ltd.
P.O. Box 2792
**Lusaka**
Zambia, Central Africa
Tel: 73793
Cable: ARJAYTEE, Lusaka

**MEDITERRANEAN AND MIDDLE EAST COUNTRIES NOT SHOWN PLEASE CONTACT:**
Hewlett-Packard S.A.
Mediterranean and Middle
East Operations
35, Kolokotroni Street
Platia Kefallariou
GR-Kifissia-**Athens**
Telex: 21-6588
Cable: HEWPACKSA Athens

**OTHER AREAS NOT LISTED, CONTACT:**
Hewlett-Packard
Export Trade Company
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPACK Palo Alto
Telex: 034-8300, 034-8493


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