



CAPABILITY & FEATURES

- 1) The DT-90 can test 64K x 1, 256K x 1 and 1 MEG x 1 DRAM's or Dynamic Random Access Memory IC's.
- 2) It can test at "read access times" from 60 ns to 200 ns.
- 3) Alternate read/write test patterns of "1010" and "0101" are automatically run to all device addresses.
- 4) Vcc MARGIN tests can be selected, allowing read/write function tests to be run at three voltage levels.
- 5) A "CYCLE" switch allows continuous testing.
- 6) Test immediately stops upon detecting a read error.
- 7) LED indicators are provided to indicate: TEST RUNNING, TEST SUCCESSFULLY COMPLETED, TEST STOPPED ON ERROR, DRAM Vcc level (HI, LO or normal 5V).
- 8) 16 & 18 PIN "ZIF" Zero Insertion Force test sockets are provided for DRAM's being tested.

OPERATION & CONTROLS

POWER ON

The unit is powered ON with 9 VDC from an AC adaptor (200-300 mA output rating). A 2.1 mm DC power jack is located on the right side of the unit. The GREEN/RED, PASS/FAIL indicator will illuminate RED upon initial power up. To maximize accuracy of ACCESS TIME measurements, unit should be powered ON several minutes or longer.

INSERT DRAM TO BE TESTED

A DRAM to be tested may be installed or removed from a test socket with the DT-90 powered ON. Only one DRAM at a time can be tested; insert a 1 MEG DRAM in the 18 PIN ZIF socket on the left or a 64K or 256K DRAM in the ZIF socket on the right. The socket is opened by raising the handle; lower the handle to grip the IC PINS after inserting the device to be tested, position PIN 1 or the notched end to the top.

ACCESS TIME (SPEED) SELECT

Set speed control full clockwise (200 ns). Momentarily press TEST push button to start test. A successful test sequence will run about 5 to 7 seconds and stop with a continuous GREEN indication on the PASS/FAIL indicator LED. To determine the minimum access time or speed of a DRAM being tested, simply reduce the access time until you find the speed at which the device fails and then slightly increase the access time to find the fastest error free operation. NOTE: The tester should be powered ON for a couple minutes or longer to maximize the accuracy of the dial settings.

CYCLE SWITCH

The CYCLE switch will simply repeat the test sequence until an error is detected. Switching the CYCLE switch ON will also start the test sequence.

MARGIN SWITCH

The MARGIN switch will run the first half of the test sequence at LO voltage (Vcc=4.5V), and the last half of the test sequence at HI voltage (Vcc=5.6V). When the MARGIN switch is OFF the DRAM is tested at the normal 5V level.

INDICATORS

HI - 5V - LO Three LED indicators show the Vcc level currently applied to the test sockets.

GREEN/RED, PASS/FAIL LED Flashes GREEN to indicate a test sequence is running, indicates continuous GREEN to indicate a test has successfully completed and indicates continuous RED to indicate an error was detected. Will indicate continuous RED upon initial power ON.

TEST SEQUENCE

When a 1 MEG DRAM is tested, a "0101" data pattern is written to all addresses in the DRAM, then each address is read back and compared for correct data. An error stop will occur immediately during the read test if the data is not correct. After the "0101" pattern test, a "1010" pattern is written to all addresses, read back and compared. Upon successful completion of the two pattern test cycle, the tester stops and a continuous GREEN is indicated on the PASS/FAIL LED. A 256K DRAM receives the same test except each address is written to and read back 4 times in each pattern and a 64K DRAM receives the read/write test 16 times in each pattern.

LIMITED WARRANTY - FACTORY ASSEMBLED MODEL DT-90

STARTEK INTERNATIONAL INC. warrants this hardware product, to the original purchaser, against defects in material or workmanship for a period of 180 days from the date of purchase. Parts and labor costs to repair a defective unit are covered provided the instrument was not modified, did not receive unauthorized repairs or was not subjected to misuse or abuse. This warranty is limited to the value of the instrument and does not cover any incidental or consequential damage or expense. This warranty does not cover transportation costs; all repairs are FOB our factory in Ft. Lauderdale, FL.

THERE ARE NO OTHER WARRANTIES THAT EXTEND BEYOND THE ABOVE DESCRIBED LIMITED WARRANTY.

For questions or service, please contact the factory at
PHONE: (305) 537-5577.



WHAT THE DT-90 DRAM TESTER CAN DO

The DT-90 can test 64K x 1, 256K x 1 or 1MEG x 1 DRAMs and can measure speed or access times from 60 ns to 200 ns. There is a switch to select a HI and LO voltage margin test, three LED indicators that show the current "Device Under Test" or "DUT" voltage and a red/green LED which blinks green to show a test is running, indicates continuous green to show a test has run complete without an error and will indicate continuous red when a test is stopped by detecting an error. An 18 pin ZIF (Zero Insertion Force) test socket is provided for 1 MEG DRAMs and a 16 pin ZIF test socket is used for the 64K and 256K DRAMs. A push button switch starts a test sequence which runs about 5 to 7 seconds depending on the access speed, however, a "CYCLE" switch is provided to continuously recycle the selected test, if desired.

When a 1 MEG DRAM is tested, a "0101" data pattern is written to all addresses in the DRAM, then each address is read back and compared for correct data. An error stop will occur immediately during the read test if the data is not correct. After the "0101" pattern test, a "1010" pattern is written to all locations, read back and compared. Upon successful completion of the two pattern test, the DT-90 will stop and indicate a continuous green on our PASS/FAIL indicator. A 256K DRAM receives the same test except it is written to and read back 4 times in each pattern and a 64K DRAM receives the write/read test 16 times in each pattern.

If the "CYCLE" switch is ON, the test does not stop and will continue until an error is detected. If the "MARGIN" switch is ON, the first test cycle will be run at "LO" margin DUT operating voltage and the second cycle will automatically switch to "HI" margin DUT operating voltage. With both the MARGIN and CYCLE switches ON, the tests will alternate from LO to HI margin voltage. All voltage and test signals are applied to both ZIF test sockets simultaneously but only one DRAM at a time can be tested. DRAMs to be tested can safely be inserted or removed from the ZIF test sockets with the tester power on.

THE DYNAMIC RAM MEMORY

The DRAMs use multiplexed row and column address inputs, the 64K DRAM requires only 7 address lines, the 256K DRAM requires 9 and the 1MEG requires 10. Address decoding and address latches are incorporated in the DRAM. To address the DRAM, row address data is put on all address lines and clocked by the "RAS" (Row Address Strobe) signal, then the column address data is put on the address lines and clocked by the "CAS" (Column Address Strobe) signal. There is a

READ/WRITE input pin "W" to determine the type of operation, a DATA IN pin "D", and a DATA OUT pin "Q". The DRAM uses a capacitor storage charge for every bit in the array which degrades with time. To retain the data stored in the DRAM, the bits need to be "refreshed" or "row addressed" at minimum cycle intervals, depending on the specific part. This is typically done by a RAS only cycle thru the row addresses or a normal read or write cycle will accomplish the refresh as well.

There is critical signal timing involved with the address and strobe inputs. When that timing is within spec for a given part, the "access time" or "speed" is the time from "RAS", which is the start of the addressing, to the time at which there is "VALID DATA" at the output pin "D" (DOUT).

CIRCUIT DESCRIPTION

The DT-90 DRAM TESTER uses two voltage regulator ICs and only 6 logic ICs, thanks to the two PLDs (Programmable Logic Devices) which displace about ten TTL (74XX series) parts for an equivalent circuit. Parts are installed on both sides of a double sided, PTH, PC board measuring 3.35" x 3.8".

An AC power adaptor is used to provide 9VDC at 150 mA to a full wave bridge input, D5-D8, which performs an auto polarity function from the adaptor wiring. U7 is a 5 volt regulator which supplies power to everything but the DUT (Device Under Test). DUT power is regulated by U8, an LM317LZ adjustable regulator which is controlled by logic in the PLD, U5. U8 will output to the DUT a regulated 5.0V for normal test, "MARGIN" test "LO" output is 4.5V, "MARGIN" test "HI" output is 5.6V.

U5 and U6 are TTL PAL (Programmable Array Logic) devices. U5 is an MMI/AMD PAL16L8B-2CN which is a low power, 25ns part. The 25ns propagation delay of U5 and U6 is an integral part of the system timing. U5 generates a continuous running clock oscillator consisting of the logic in U5 with the feed back circuit of R15, R16, C12 and C5. The additional circuitry of R14, "Access time" selection pot R5, "calibration" trimpot R19 and "dial spread" trim pot R17 form the speed test circuit which varies the basic system clock.

The clock output at U5, pin 15 runs continuously and is fed into U6 at pins 1 and 6. When the "START TEST" switch, SW1 is pressed, a "START/RESET" signal is generated thru R7, C2 and R8 which resets U2 and U3 at pin 11 and is also applied as an input to the PAL at U6, pin 8. Logic in U6 will gate an output clock signal, designated CK1, at pin 14. CK1 drives a 24 stage, ripple-carry, binary counter consisting of two 74HCT4040's (or CD4040B's), at locations U2 and U3 (clock input at pin 10, U2). As the clock increments the U2/U3 ripple counter, Q0 thru Q7 and Q10 thru Q17 outputs drive U1 and U4 which are the 74HCT257, quad 2-input multiplexers. U1 and U4 each select four bits of data from two different sources under the control of a common select input at pin 1.

Logic in U6 generates the "RAS" (Row Address Strobe) signal which is used as a basic timing signal in the tester circuit as well as DRAM addressing. RAS is a logic input at pin 3 of the PAL at U5, a strobe signal at pin 3 of test socket ZIF1, and pin 4 of ZIF2 and is also the input select signal at pin 1 of U1 and U4, DRAM address multiplexers. The outputs of U1 drive address lines A0 thru A3 and the outputs of U2 drive address lines A4 thru A7 of the DUT at test sockets ZIF1 and ZIF2.

A 256K DRAM requires an additional address line A8 and a 1 MEG DRAM requires two additional address lines, A8 and A9. To generate the A8 and A9 address lines, Q8, Q9, Q18 and Q19 from our 24 stage counter, U2 and U3, are logic inputs to the PAL at U6 which generates the A8 output at pin 19 and the A9 output at pin 12.

Both the 16R4 type PAL at U6 and the 16L8 type PAL at U5 are rated at 25 ns internal gate propagation delay. As mentioned earlier this delay is an integral part of the system timing. These internal propagation delays are used to determine the timing of the low "CAS" (Column Address Strobe) signal at pin 12 of U5 about 40 ns after "RAS" goes low. The CAS signal is applied to the DUT which gates the column address data after the row address data has been gated. At the intersection of the row address and column address, we have the selected bit location. Q20 from the 24 stage ripple counter will determine if the operation will be a write or read cycle in the DRAM. From the start of the test Q20 (U3, pin 12) applies a low to the DUT READ/WRITE inputs at ZIF1, pin 2 and ZIF2, pin 3. The low signal selects a WRITE cycle in the DRAM; as we cycle thru all of the address locations the first time, WRITE mode is selected.

As the ripple counter gets to Q20, it has cycled thru all address locations in a 1MEG DRAM once but will have cycled thru all address locations in a 256K DRAM four times and sixteen times for a 64K DRAM, depending on what type part is under test (only one DRAM at a time can be tested). Q20 is also a logic input to PAL U5 at pin 6. U5 will generate a "DIN" signal, which will determine the data bit, high=1, low=0, applied to the DUT at ZIF1, pin 1 and ZIF2, pin 2. Q0 and Q21 are also applied to the logic input of PAL U5 at pins 1 and 7 respectively. Q0 is used to alternate the bit pattern every other location as it is triggered every cycle or clock time. Q21 will be the term used to change the pattern from "010101, to "101010" during the second write cycle. Every DRAM location will have a "1" bit written to it and read back and a "0" bit written to it and read back 1 to 16 times per test, depending on the type of DRAM, 64K, 256K or 1MEG.

During the read cycle, the access time of the DRAM is the time from RAS to DOUT (VALID DATA OUT) or the time from the first address strobe until valid data is at the output pin "Q". The Q output is a tri-state signal, which will switch to a high impedance, mid logic level when the CAS signal goes inactive. As each address is cycled thru during the read portion of the test, the data bit read out is applied at pin 11 of the PAL U5 and compared with the expected bit, if the data does not compare an "ERROR" signal is generated at output pin 19 which goes to pin 9 of the PAL U6 where the "FAIL" output will go high and the CK1 output will stop. This will stop advancing the ripple counter and illuminate the red/green LED continuous red.

The margin switch, SW2 is "ON" when the contacts are open removing a ground from pin 5 of PAL U5, allowing pull up resistor R4 to switch the input high. The logic in U5 will then switch the low output from pin 17, which selected a normal DUT operating voltage of 5.0V, to pin 16, which selects a low margin voltage of 4.5V. LEDs D1, D2 and D3 indicate which DUT operating voltage is currently selected and will remain illuminated after an error stop to indicate what operating voltage was selected at the time of a failure.

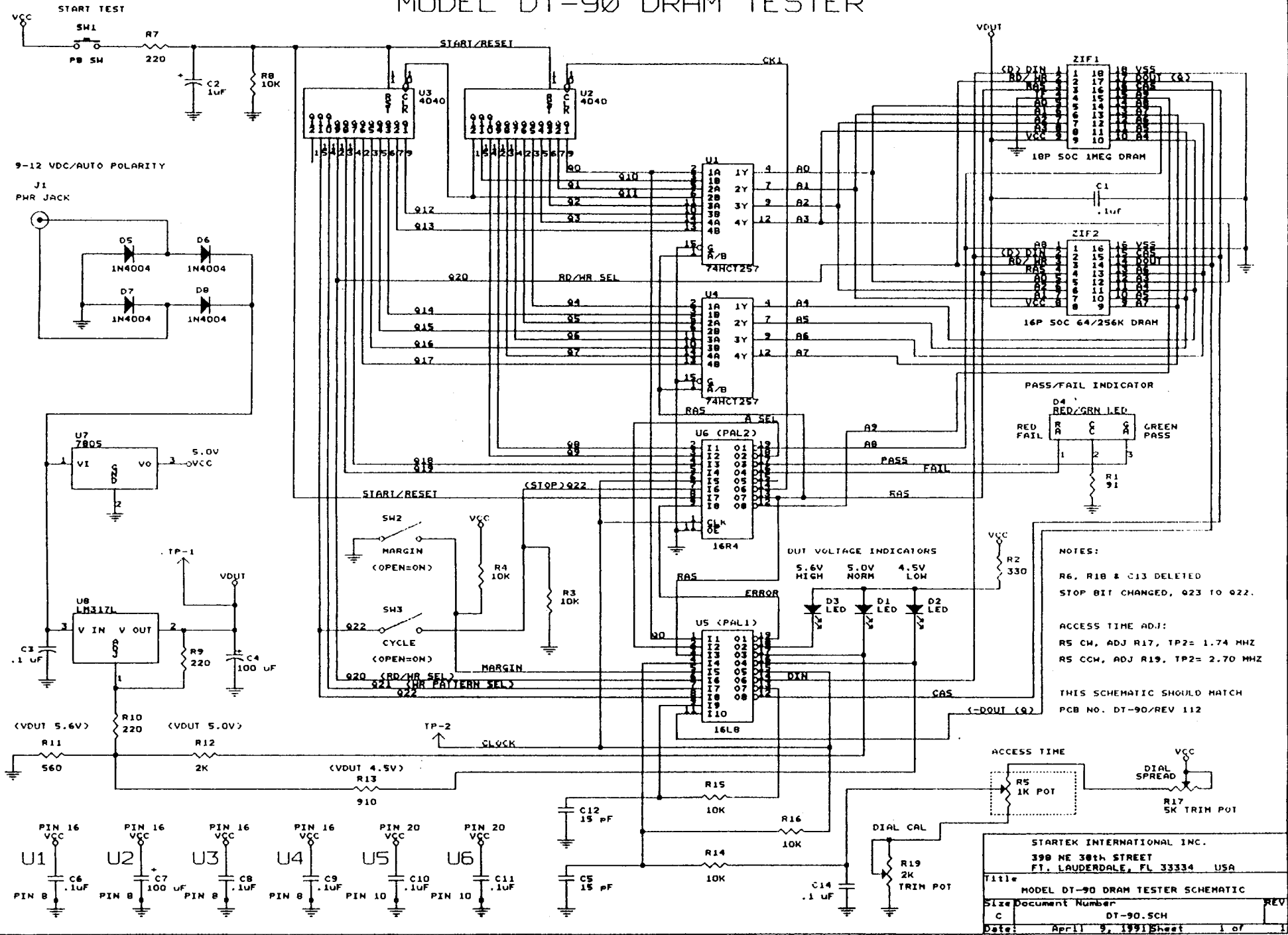
Q21 & Q22 are the PAL U5 input terms at pins 7 & 8 that will be used by the U5 logic to switch the "LO" margin test to "HI" and select U5 output pin 18, illuminating D3 to indicate the DUT is at a HI margin operating voltage of 5.6V. The U5 output pins selecting the appropriate LED voltage indicator also directly control the DUT voltage by applying a ground to R12 via output pin 17 or R13 via output pin 16 or a ground to neither when pin 18, HI margin is selected. This affects the adjustment pin on the adjustable regulator U8 which produces "VDUT", the operating voltage for the DRAM being tested.

The "CYCLE" switch, SW3 is "ON" when the contacts are open, allowing the pull-down resistor R3 to hold pin 7 of PAL U6 low. Q22 is the "STOP BIT". When Q22 goes high, the two pattern test has finished. The SW3 CYCLE switch simply prevents the Q22 high output from reaching the logic input of PAL U6.

C1, C3, C6 and C8 thru C11 are power by-pass capacitors, R1 is used to limit the current flow thru the red/green LED, D4. R2 limits the current thru D1, D2 and D3, which are red discrete LEDs.



MODEL DT-90 DRAM TESTER

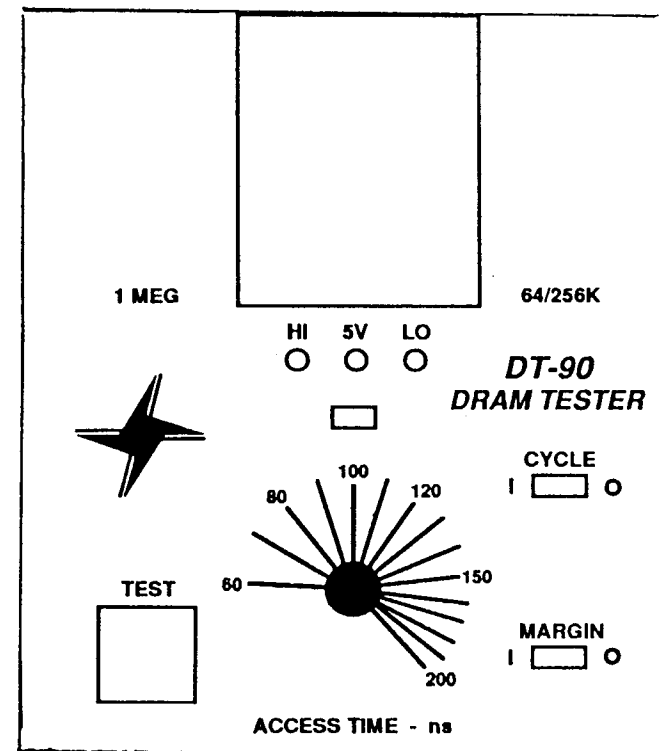
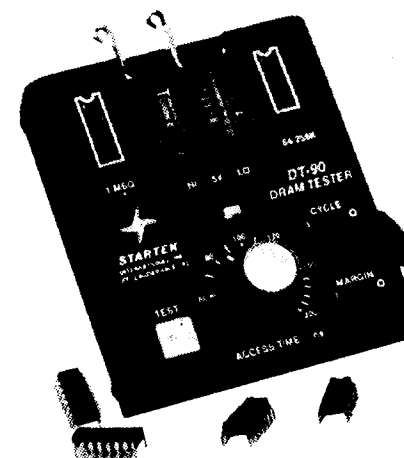


DT-90 PARTS LIST

QTY	TYPE	DESCRIPTION	REF	PR EA
1	PC BOARD	DBL SIDED, PTH	DT-90	\$18.00
3	LED	RED, 1/8 IN. DIA.	D1-D3	.25
1	LED	RED/GREEN, 3 LEAD	D4	2.00
4	DIODE	1N4001-7, 1A RECT	D5-D8	.15
8	CAP	.1 uF, MONO (104)	C1,C3,C6,C8-C11,C14	.20
2	CAP	15 pF, MONO (150)	C5,C12	.25
1	CAP	1 uF, DIP TANT	C2	.25
2	CAP	100 uF, FILTER	C4,C7	.25
6	RES	10K, 1/4 W, 5%	R3,R4,R8,R14-R16	.10
3	RES	220 OHM, 1/4 W, 1% (or pretested 5%)	R7,R9,R10	.30
1	RES	560 OHM, 1/4 W, 5%	R11	.10
1	RES	2K, 1/4 W, 1%	R12	.20
1	RES	910 OHM, 1/4 W, 5%	R13	.10
1	RES	330 OHM, 1/4 W, 5%	R2	.10
1	RES	91 OHM, 1/4 W, 5%	R1	.10
1	POT	1K, LINEAR TAPER	R5	1.50
1	POT	2K TRIMMER	R19	.50
1	POT	5K, 4 TURN TRIMMER	R17	2.50
2	IC	74HCT257	U1,U4	.75
2	IC	74HCT4040 / CD4040B	U2,U3	.75
1	IC	PAL 16R4A-4 (PROG)	U6	7.50
1	IC	PAL 16L8B-2 (PROG)	U5	7.50
1	IC	7805, TO-220	U7	.75
1	IC	LM317LZ, TO-92	U8	.75
1	SWITCH	PUSH BUTTON, NO	SW1	.75
2	SWITCH	SLIDE, SPDT, MINI	SW2,SW3	.50
1	JACK	2.1 mm, DC INPUT	J1	.75
4	IC SOC	16 PIN, ST	U1-U4	.25
2	IC SOC	20 PIN, ST	U5,U6	.25
1	ZIF SOC	16 PIN, TEST	ZIF2	8.50
1	ZIF SOC	18 PIN, TEST	ZIF1	9.50
1	KNOB	ACCESS TIME	FOR R5	1.50
1	CABINET	"STAR-CAB"™, ALUMINUM, 2 PC		22.50
1	AC ADP	9VDC @ 300 mA, 110 VAC PRI		7.50



STARTEK INTERNATIONAL, INC.



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DT-90-CK KIT ASSEMBLY

RECOMMENDED TOOLS & SUPPLIES

Soldering iron or station with small tip

Electrical solder, small diameter

Small wire cutters

Small needlenose pliers

Small regular screwdriver

#2 phillips screwdriver

Volt/Ohm meter

NOTE: A 100 MHZ Oscilloscope or a Frequency counter that can measure 1 to 3 MHZ (such as the STARTEK model 1500 series) is ideal for "access time" calibration, however, this adjustment can be approximated.

ASSEMBLY STEPS

1) Check parts against parts list to verify nothing is missing and ensure you can identify the parts for assembly. For each assembly step, reference the PARTS LIST and the parts placement legend printed on each side of the PC BOARD.

2) Install six 10K resistors, R3, R4, R8, R14, R15 & R16. All resistors will be installed on SIDE B or the bottom of the PCB. After soldering the resistors, trim excess lead length.

3) Install three 220 Ohm resistors R7, R9 & R10 on SIDE B, as in the previous step. These resistors may be marked either 1% or 5% tol. If 5% resistors are supplied, they are pretested. (The 220 Ohm- 1% look similar in coloring to the 2K- 1%, do not confuse)

4) Install the remaining resistors, R1, R2, R11, R12 & R13 on SIDE B of the PC board where indicated, check the parts list for proper values. After soldering, trim excess lead length. This should complete the installation of all fixed value resistors.

5) Install four 16 pin IC SOCKETS at locations U1-U4 and two 20 pin IC SOCKETS at U5 & U6, all on SIDE B.

6) Install four rectifier DIODES at D5-D8 on SIDE A. These diodes may be any number from 1N4001 to 1N4007. NOTE POLARITY

7) Install eight .1 uF (104) monolithic by-pass capacitors at C1, C3, C6, C8, C9, C10, C11 & C14, all on SIDE B.

8) Install two 15 pF (150) capacitors at C5 & C12, SIDE B.

9) Install C2, a 1 uF dipped tantalum capacitor, SIDE B. OBSERVE POLARITY.

10) Install two 100 uF ELECTROLYTIC capacitors at C4 & C7, SIDE B, OBSERVE POLARITY.

11) Install POT R5. Bend the leads upward, parallel to the shaft and place shaft through PCB from SIDE B. First secure with washer and nut, then solder the three leads.

12) Install U7 & U8 voltage regulators on SIDE B. Install U7, the TAB type 7805, face up with the leads bent down through the holes on the PCB .

13) Install SW1, PUSH BUTTON SWITCH, SIDE A. Install flush to board with the plastic guide pins in the PCB holes.

14) Install two slide switches at SW2 & SW3, SIDE A. BE SURE THESE SWITCHES ARE STRAIGHT to avoid cabinet fit problems. Solder the 3 center leads first, the 2 bracket leads can be soldered after the cabinet fit is checked.

15) Install J1 POWER JACK, SIDE B.

16) Install 2K trimmer at R19, SIDE B. The back of this trimmer can rest against R5 as it is insulated.

17) Install the 5K, 4 turn trimmer (small, round, blue pot), at R17 on SIDE B.

18) Install the three small RED LEDs at D1, D2 & D3, SIDE A. NOTE POLARITY, the LEDs have a flat side which should be toward the top of the PC board. Mount in a straight line with leads extending 3/16 inch above the PC Board.

19) Next install D4, the RED/GREEN LED. Observe polarity, the slightly shorter lead is the red anode (+) and the center lead is the common cathode (-), the remaining lead is the green anode. Holding the LED (leads pointing down) with the shorter lead on your left, bend the center lead at a 90 degree angle, snug to the component body, toward yourself and likewise bend the other two leads in the opposite direction, spreading them slightly. Align the LED over the D4 location on SIDE A and bend the three leads down to fit the holes.



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20) Install the two ZIF test sockets at ZIF1 & ZIF2, SIDE A. Be sure to fit them snug to the PCB. Solder a corner pin and then the diagonal corner pin, check alignment, make correction if necessary and solder remaining pins if you are sure sockets are straight and flush to PCB.

21) Reference the parts list and install the six ICs, U1-U6 in the proper sockets, NOTE POLARITY.

22) The PC Board assembly should now be complete. NOTE: C13, R6 & R18 HAVE BEEN ELIMINATED. Carefully recheck all of the solder connections and parts requiring specific polarity installation. When you are sure your assembly is complete and correct, proceed to the POWER-ON check out.

POWER-ON CHECK & ADJUSTMENT

First set R17 and R19 to midpoint adjustment. the Power supply should be rated 9 VDC at 200 mA or more (actual current will be about 150 mA), plug wiring polarity does not matter as we have a diode bridge input circuit.

Apply power to the circuit with no device in either test socket, a continuous RED on the PASS/FAIL indicator should be displayed.

Using a DC Voltmeter, make the following measurements. A pad and hole is located in each corner of the PC board as a ground test point.

The following voltages should be +/- .1 volt.

- 1) Vcc, U7, pin 3 should be 5.0V (pin 3 is next to C11)
- 2) With MARGIN switch, SW2, OFF (slider to right), measure VDUT, TP1. Should be 5.0V. (LED D1 should be ON)
- 3) With MARGIN switch ON, "LO" DUT voltage indicator (D2 LED) should be ON and TP1 should measure 4.5V.
- 4) Place a DRAM IC in the appropriate ZIF test socket, turn the ACCESS TIME pot, R5, fully clockwise and press the test push button switch, SW1. If the device under test is good and the tester is working properly, the PASS/FAIL LED will blink green and if the MARGIN and CYCLE switches are ON, the tester should alternate between HI and LO margin voltages.

If you do not get a correct indication, try a power off and on reset. Turn ON the CYCLE switch SW3 (slider to the left) and the tester should repeat the test without having to press the TEST button.

5) When the HI margin voltage indicator, D3 is ON, the voltage at TP1 should be 5.6V.

6) When all of the above steps check out properly, only the SPEED or ACCESS TIME calibration remains. This can be done with either a frequency counter or a 100 MHZ oscilloscope.

OSCILLOSCOPE METHOD: Connect a probe to TP2 with NO IC in either test socket. This is the master clock and it should run continuously. Allow the unit to operate a few minutes or longer for maximum stability. Turn R5 fully CCW and adjust R19 for a low clock pulse of 150 ns. Measure this pulse at the 1.0 VDC level. Next turn R5 fully CW and adjust the low clock pulse for 300 ns. Go back and forth repeating these two adjustments until they are correct, this usually takes 3 to 5 times.

FREQUENCY COUNTER METHOD: Probe TP2 for counter input, turn R5 fully CCW and adjust R19 for a frequency of 2.70 MHZ. Next turn R5 fully CW and adjust R17 for a frequency of 1.74 MHZ. Go back and forth between these adjustments until they are correct, this usually takes 3 to 5 times. This adjustment is usually easy to make; both pots should end up somewhere near midrange.

NOTE: If you are using a 50 OHM counter input, use a resistor about 470 OHMS in series with your probe.

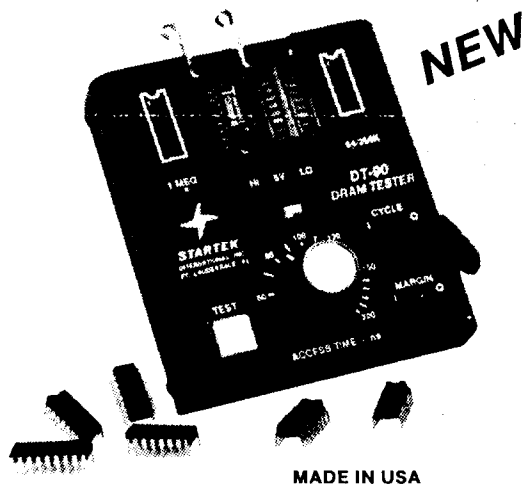
If you do not have a scope or counter immediately available to calibrate the ACCESS TIME control, set R17 and R19 to midrange, which should be near calibration, and use the speed test for a relative indication, and of course the function and voltage margin tests should work fine.

PROBLEMS WITH PARTS OR ASSEMBLY

Should you have questions or problems you can not resolve, technical telephone assistance is available at (305) 537-5577

There is a \$40.00 flat rate repair service for the DT-90 KIT. This covers all troubleshooting and repair labor, parts, test, calibration and return charges.

In the rare event you receive a defective part in your kit, you may return it within 90 days for a free replacement.



MODEL DT-90 DRAM TESTER

The DT-90 is a new, compact memory IC tester that can READ/WRITE FUNCTION TEST, VOLTAGE TEST and MEASURE THE SPEED of 1 MEG x 1, 256K x 1 and 64K x 1 Dynamic RAMS. LED indicators show 3 Vcc TEST VOLTAGES and a RED/GREEN LED flashes when test is running then indicates PASS or FAIL. A switch is provided to continuously cycle a test if desired. The DT-90 is housed in a rugged aluminum cabinet 3.4" W x 3.8" H x 1" D. Two ZIF TEST SOCKETS are provided for the IC under test. The unit is powered by a 110 VAC to 9 VDC @ 300 mA adaptor which is included. The DT-90 is sold in KIT FORM with complete assembly instructions or FACTORY ASSEMBLED, calibrated and tested.

MODEL DT-90-CK

\$89⁹⁵ Kit
Form

MODEL DT-90

\$119⁰⁰ Factory
Assembled

TOLL FREE ORDER LINE

800-638-8050

FOR INFO PLEASE CALL (305) 561-2211

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